SECTION 5
HARDWARE DESCRIPTION

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SYSTEM DESCRIPTION

501. The sounder control software must be intimately integrated with the analog and digital hardware required to operate the sounder. The system configuration is shown in Figure 5-1 with the layout of the Main Chassis major components shown in Figure 5-2. The major sub-assemblies include:

a. A 10 MHz frequency source (the Master Oscillator, 10 MHz Rubidium Oscillator, optional).

b. The MAIN Computer, an embedded 80486 single board computer with an eight-slot passive backplane. Computer sub-system components are:

   1) Intel 486 DX processor
   2) 32 Mbytes RAM
   3) 4 Mbyte disk emulator card (flash ROM)
   4) SVGA graphics interface
   5) Ethernet adapter
   6) Multi I/O card (2 x 16550 UART serial ports, parallel port)
   7) 16 channel Data Acquisition Card
   7) 2 Msample/sec 4 channel Digitizer Card
   8) TMS320C40 Digital signal processor card
   9) 1.4 Mbyte 3½ inch floppy drive

c. The Auxiliary Computer, a single board computer including:

   1) Intel Pentium processor
   2) 64Mbytes RAM
   3) SVGA graphics interface
   4) PC-104 10base2 Ethernet port
   5) IDE hard disk
   6) IDE disk controller
   7) 1.4 Mbyte 3½ inch floppy drive
   8) Floppy disk controller
   9) PC-104 SCSI-2 interface
   10) 2 x serial ports
   11) Parallel port
   12) Keyboard interface

d. Two x 150 W solid state RF power amplifiers operating over a range of 1 MHz to 40 MHz.

e. Electronically switchable right or left hand circularly polarized active receiving antennas, powered and controlled by the Antenna Switch.

f. Digital signal processor (DSP) with direct computer interface and 3 Mbytes of independent memory (i.e., does not require use of memory in the MAIN computer).

g. Modular chassis mountable power board to convert the 24 V DC to 28 V DC primary power or battery power to the precise +15, –15, +12, –12, +5, and –5 volts needed by various components in the system. The RF power amplifier circuitry can utilize the 24 V DC to 28 V DC directly.

h. Analog and digital cards for signal generation and reception.

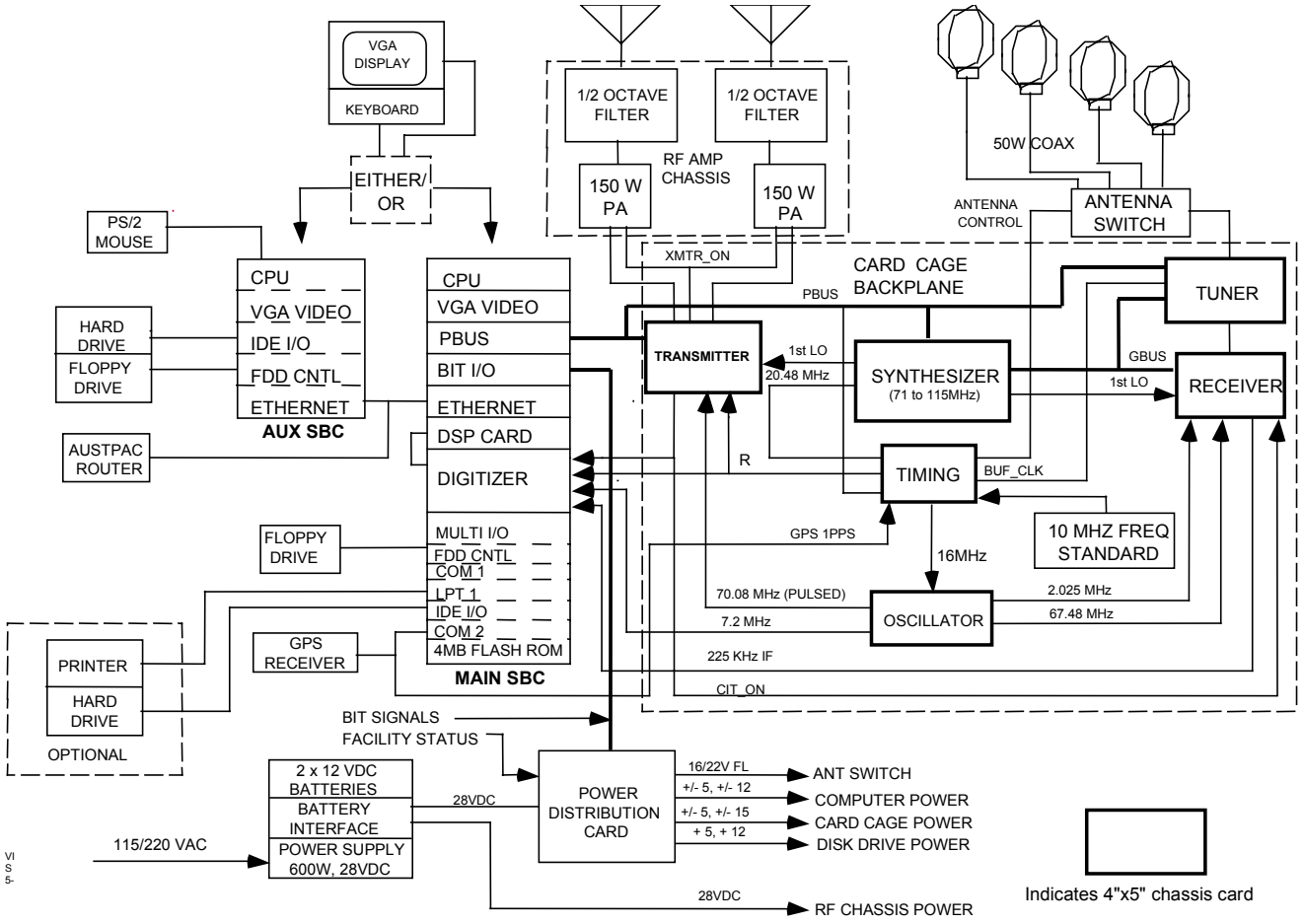

Figure 5-1 System Diagram

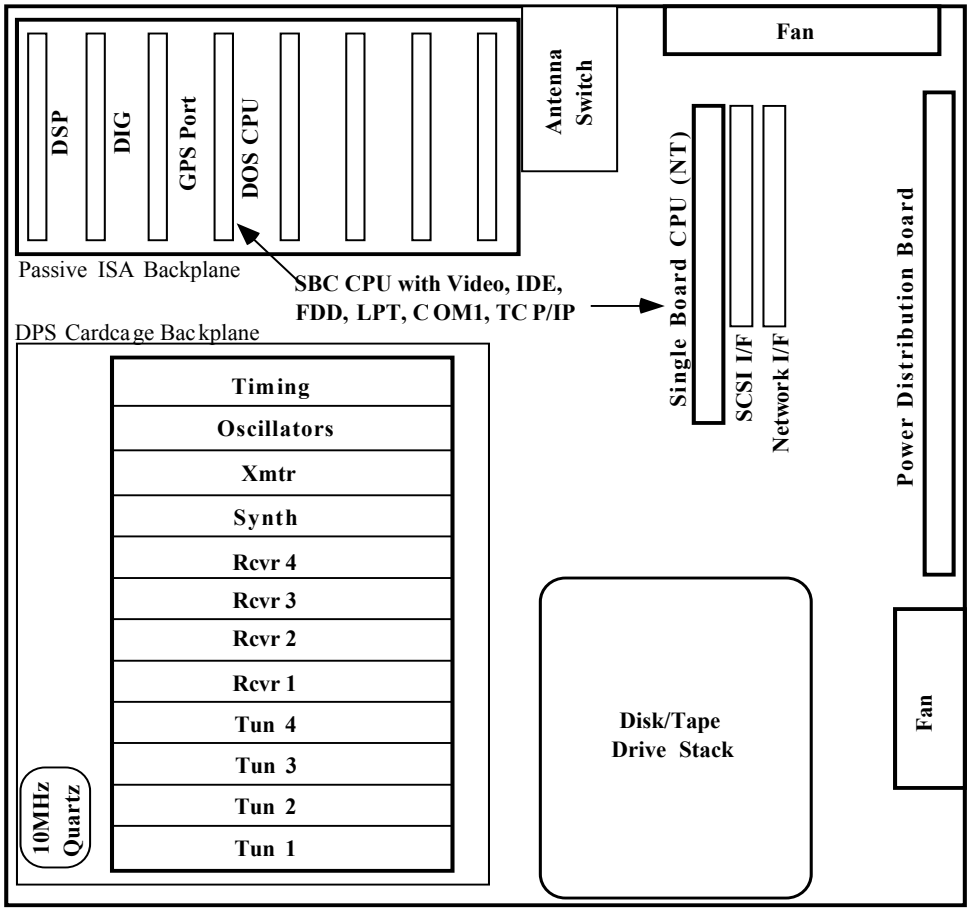

Figure 5-2 Main Chassis Major Components

SOUNDER PROPRIETARY CIRCUIT BOARDS

Timing Card

502. The Timing (TIM) Card generates digital clocks and timing sequences slaved to the 10 MHz system frequency standard. The Timing Card can automatically be synchronized with an external 1-pps time reference and can offset all system timing signals ±0.5 sec in 50 μsec steps from this reference signal under program control. In conjunction with the GPS receiver and the computer's battery backed-up real time clock, an assembly language function (GET_EXT_SYS_TIME) has been developed to provide real time (including year, day, hour, min, sec and msec) to the system program with 5 msec resolution (but μsec accuracy).

503. Another function, TIMEX, will correct the computer's on-board battery powered clock whenever it has drifted by 1 second (the cumulative error in the free-running system computer clock is tracked and the measured offset is corrected for whenever time is requested by GET_EXT_SYS_TIME). This technique provides time stability equal to that of the system frequency standard (either quartz or rubidium standard) not the system

clock. The optional GPS receiver will keep all system timing to microsecond accuracy by means of proprietary software and by interfacing the GPS receiver's 1-pps signal to the Timing Card.

Functional Description of the Timing Card (Refer to Figure 5-3)

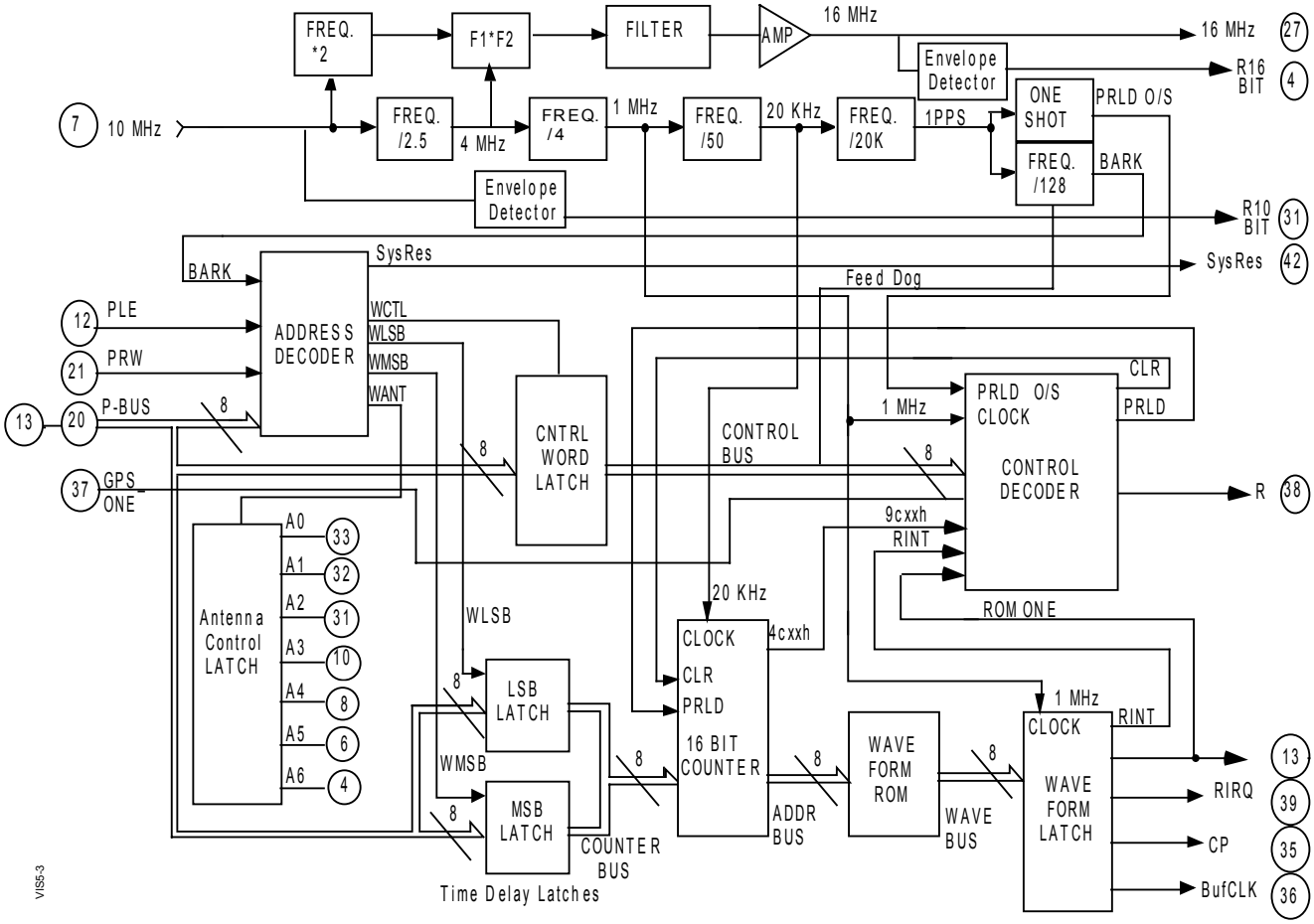

Figure 5-3 Timing Card Block Diagram

504. **Timing Operation.** The Timing Card converts the 10 MHz frequency standard into the 16 MHz system reference frequency and generates the 20 kHz timing clock. The 10 MHz signal from the master oscillator is input on pin 7. It then goes through a matching transformer circuit, doubled to 20 MHz and divided down to 4 MHz. The 20 MHz and 4 MHz frequencies are digitally mixed to produce 16 MHz which is crystal filtered, and is amplified by Q2. The signal, as the output of pin 27, is fed to the Oscillator Card which generates more clock signals and all of the fixed frequency LO signals. U4 divides the 10 MHz down to 1 MHz and U5 reduces it further to 20 kHz which clocks out (via counters U28 & U29) all of the timing waveforms stored in U30.

505. **P-Bus (Pins 13 to 20)**. The P-bus is an 8-bit bus which via the address decoder (U20) writes control bytes from the MAIN computer into four latches: antenna latch (U19); control word latch (U21); timing offset-

counter LSB latch (U27); and timing offset-counter MSB latch (U26). It is a unidirectional bus, from computer to card, and is asynchronous (no handshaking).

506. **Address Decoder (U20)**. The address decoder has two inputs in addition to the P-bus data lines; they are: 1) program latch enable (PLE) and 2) program write (PRW). In operation, the P-bus sets the address for one of the four latches, then the PLE is strobed, and the latch-address is decoded. At this point, depending on the address, WGAIN, WCTL, WLSB, or WMSB is buffered and held waiting for the data to be placed on the bus. When the data is on the P-bus the PRW is strobed enabling the selected-latch and loading the data from the P-bus.

507. **Control Word Latch (U21)**. There are four signals presently implemented in the control-word for the sounder:

a. **ENPRLD.** Enable presetting of the offset-timing counter.

b. **ENCLR.** Enable CLR for external 1-pps system synchronization ().

c. **ENR.** Enable R, transmitter pulse ().

d. **FEED WATCHDOG.** This signal is to be refreshed to block the system-reset. If this is not refreshed by the time of the next BARK signal every 128 seconds, the system is assumed to be hung, and the system-reset line will be activated, causing a hard-boot on the 486 motherboard via the reset circuit on the motherboard.

508. **MSB (U26) and LSB Latches (U27).** These two latches are programmed to hold the offset-time for use in synchronizing remote systems. The configuration allows for 50 μsec resolution, based on the 20 kHz (1/50 μsec) clock of the 16-bit counter.

509. **16-Bit Counter (U28, U29).** Driven by the 20 kHz clock signal from U5, these two programmable logic devices (PLD) count from the timing-offset as held by U26 and U27 and roll-over via a reset at the end of the stored timing waveforms (i.e., 20 000 counts). The output of these counters create the address for the timing waveform ROM (U30). At the direction of the control word latch (U21), the ENPRLD will allow a preset load (PRLD) to load the offset-timing data from U26 and U27 into the counters synchronously with the system's 1-pps, generated by U14 in the time-base count-down circuit.

510. **Timing Waveform ROM (U30).** This EPROM contains the various waveforms which are used by the system for control during CIT. The outputs are buffered through the waveform latch (U31), which is clocked with the 1 MHz from U2. Six signals are used:

a. **RINT.** Internal R-pulse used for generation of system R-pulse.

b. **ROMONE.** A ROM generated one-second pulse.

c. **RIRQ.** A 5 msec interrupt request. This causes IRQ7 for the system computer to be asserted every 5 msec.

d. **CP.** A 10 Hz precision timing signal read by the computer to synchronize transmissions with other sites.

e. **BUFCLK.** BUFCLK is created to allow for double-buffered latching of hardware control bytes. It writes the antenna control latch 150 μsec before transmission of a pulse.

f. **RBONE.** A separately buffered version of ROMONE.

Unless the "leash", switch S1, is closed (toward the rear of the chassis) the watchdog timer will force a hardware reset of the 80486 computer whenever 128 seconds pass without toggling bit 6 of the control byte stored in U21 on the Timing Card.

Oscillator Card

511. The Oscillator (OSC) Card generates coherent local oscillator frequencies and clock signals derived from the master oscillator. A direct synthesis technique is employed, creating a set of coherent oscillators generated by patterns stored in a high speed CMOS ROM and clocked by the master oscillator. The specific frequencies generated are:

a. A pulsed 49.6 and 20.48 MHz, which are on only during transmission.

b. 67.48 MHz, the receiver's second LO.

c. 20.48 MHz, the frequency synthesizer clock frequency.

d. 7.2 MHz, the digitizer clock frequency.

e. 2.375 MHz, the receiver's third LO.

f. A pulsed 60 kHz, the transmitter's phase code chip clock.

Functional Description of the Oscillator Card (Refer to Figure 5-4 on the following page)

512. The Oscillator Card is fed by the 16 MHz system reference oscillator (from the Timing Card) signal on pin 28, and outputs several coherent clock and oscillator waveforms which are derived from the one master reference. These outputs include:

a. On pin 25, a continuous 67.48 MHz signal which is the second LO and is used only in the Receiver Card.

b. On pin 30, a continuous 2.375 MHz which is the third LO and is used only in the Receiver Card.

c. On the rightmost SMC connector, a pulsed (gated off during signal reception) 49.6 MHz IF signal, used only by the Transmitter Card during signal transmission.

d. On the middle SMC, the phase coded first transmitter IF (C20,48) is output to the Transmitter Card.

e. On pin 37, a pulsed (gated off during signal reception) 60 kHz clock signal, which counts out the phase modulation code (stored on the ROM on the Transmitter Card) which applies the bi-phase modulation to the transmitter's 70.08 MHz 1st IF. The 30 kHz clock is used only by the Transmitter Card.

f. On pin 43, a continuous 7.2 MHz sinusoidal frequency reference which provides the master clock function (after conversion to a TTL clock signal on the Digitizer Card) to the Digitizer Card which performs the sampled data acquisition.

g. On pin 35, a continuous 20.48 MHz filtered sine wave which is doubled on the Synthesizer Card to make the master clock for the Qualcomm frequency synthesizer IC. This synthesizer provides the 71 to 110 MHz first LO to the Transmitter and Receiver Cards.

h. Rectified (i.e., DC) levels of the RF envelope signals are output to the BIT Card on pins 37, 20, 18, 32, 4 and 11.

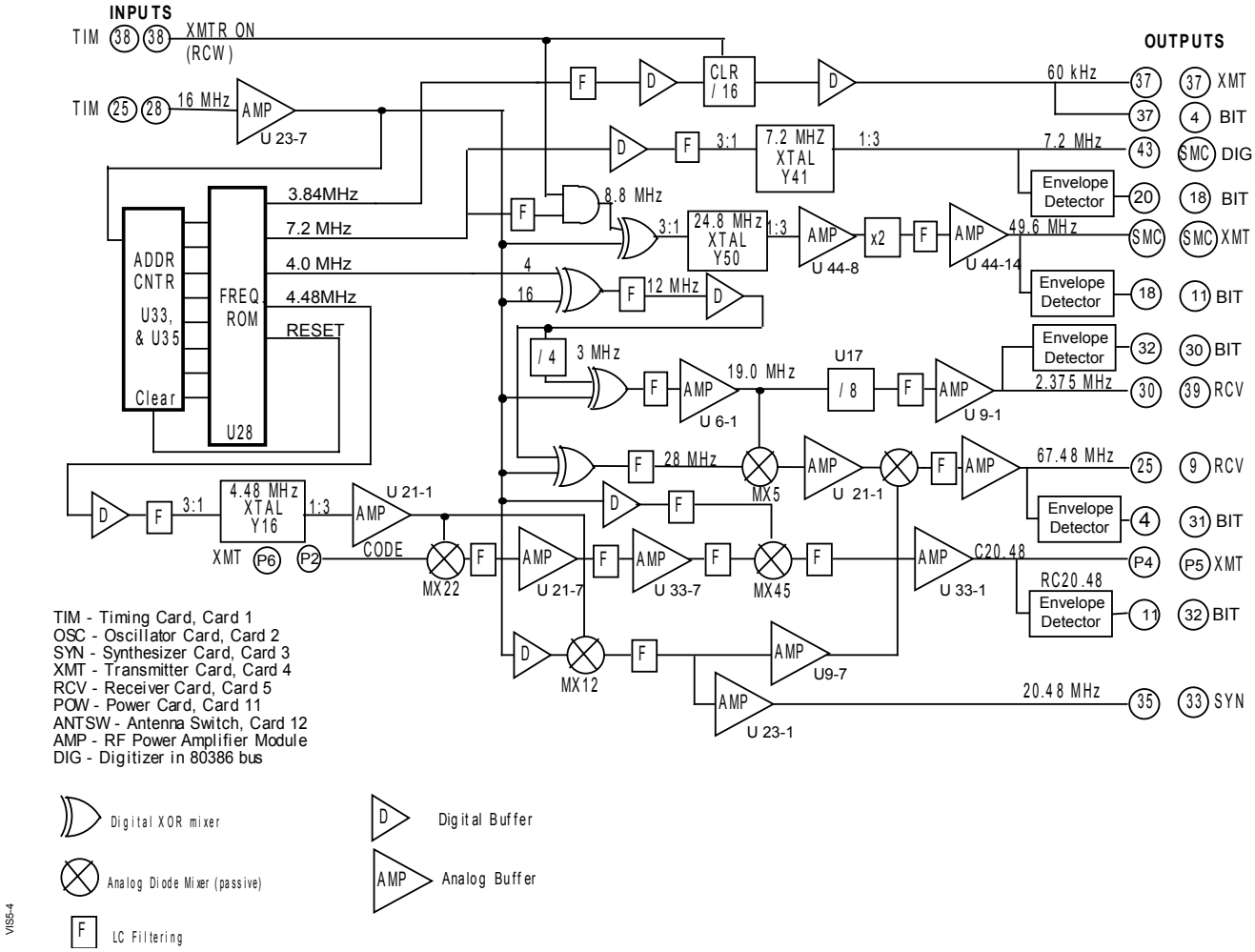

Figure 5-4 Oscillator Card Block Diagram

513. The coherent signal generation is realized by clocking the frequency ROM (U24) with the address counter (U29 and U30) at 16 MHz. The ROM outputs are TTL functions which are used to resonate the crystals at precisely their tuned frequency (referenced to the master oscillator). To obtain frequencies which cannot be realized directly out of the ROM, digital mixing provides either a sum or difference with 16 MHz to generate the desired frequency which is then crystal filtered. Frequency doubling and mixing are performed by diode mixers, while frequency dividing is implemented with binary counters. See the schematic drawings for more details concerning the implementation of these frequency generation circuits.

Transmitter Card

514. The function of the Transmitter (XMT) Card is to produce a phase coded pulsed RF output, of variable duty cycle up to 100%, that is suitable for transmission by the power amplifier.

Functional Description of Transmitter Card (Refer to Figure 5-5)

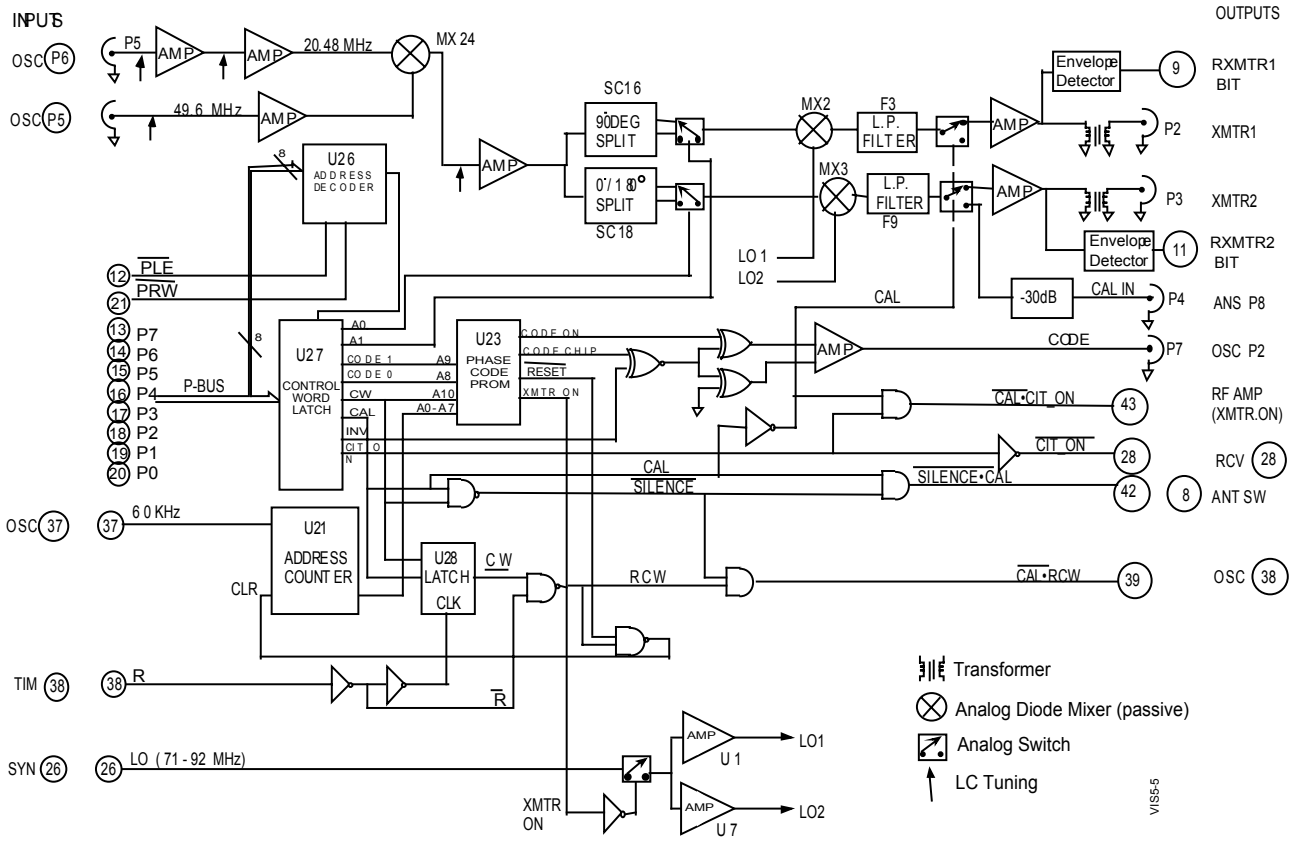

Figure 5-5 Transmitter Card Block Diagram

515. It can be seen that there may be a maximum of eight phase codes, each up to 128 bits long located in the ROM. Currently these codes are defined as two 16-bit Complementary codes, a "1-bit" simple unmodulated pulse and a 127 bit maximal length code for CW transmissions.

516. All logic control to the card is written from the host via the system's P-bus. User controllable features on the Transmitter Card are:

- Antenna polarization; right or left circular transmitter polarization (requires use of two antennas with orthogonal radiating elements)
- Code selection via the code 0 and code 1 selection lines
- Code invert or non-invert (180° phase inversion)
- CIT_ON means transmissions are currently underway
- CW Selection
- CAL

- Invert (shifts RF phase by 180°)

CAL activates software controlled switches to loopback an attenuated version of the transmitter signal and inject it into the receiver(s).

517. To write data to the Transmitter Card, the card address 0Eh is first written to the P-bus selecting this card, then the appropriate data is written to the control word latch (see the description for the Timing Card above).

NOTE

Activating CW and CAL sets the system into a radio silent mode, where it runs through the receiver functions but does not transmit. This allows it to bi-staticly receive remotely transmitted oblique incidence signals.

518. To illustrate the operation of the hardware consider one pulsed transmission cycle. A code is selected, (e.g., for the first Complementary code the program sets the control bits, code0 = 0, code1 = 0). During the next transmitted pulse the R pulse enables the address counter which clocks out the selected complementary phase code at 60 kHz (stored such that they produce 30 kbps). The resulting digital code is DC offset and used to modulate the 4.48 MHz IF on the Oscillator Card.

519. The phase modulated 20.48 MHz signal is mixed with the pulsed 49.6 MHz LO and is filtered by the SAW filter amplified and converted into four outputs by the power splitter. These quadrature signals may now be selected for output by the polarization switches (U14 and U15).

520. The two outputs from the Polarization Switch are mixed with the local oscillator signal (from the Synthesizer Card) filtered and amplified to their final output values. The output signals exit the top of the card on SMC connectors and are carried by miniature coaxial cable to the output amplifier.

521. CW transmission proceeds as above with two exceptions. The CW mode may be selected in software but will not be initiated until the next R pulse, thus synchronizing the transmission. Subsequent R pulses will have no effect until the hardware has been reset by clearing the CW bit. The CW code has been written in ROM in such a way that the code is automatically reset at the end of each sequence with no break occurring before the start of the next code repetition.

Synthesizer (SYN) Card

Functional Description of the Synthesizer Card (Refer to Figure 5-6 on the following page)

522. The 20.48 MHz oscillator frequency from the Oscillator Card is doubled to create the main clock frequency for the direct digital synthesizer (DDS) chip. The DDS outputs a new sine wave sample as a 12-bit binary number each 24.41 nsec which is converted to a 8.8 to 15.75 MHz analog signal in the D/A converter. A fixed low-pass filter cleans up this signal, which is then doubled. An electronically tuned filter selects the 17.75 to 28.75 MHz upper sideband which is doubled and tuned twice more to create 71 to 115 MHz. The four 8-bit wide frequency control bytes are latched internally in the DDS (according to the address sent to the synthesizer address latch). A separate control byte is also latched by the tuning latch (a LS374) to select the correct tuning value stored in the Tune PROM. This byte tunes the electronically tuned filters to the proper center frequency via a D/A converter. These latch interfaces are the standard P-bus interface described for the Timing Card above.

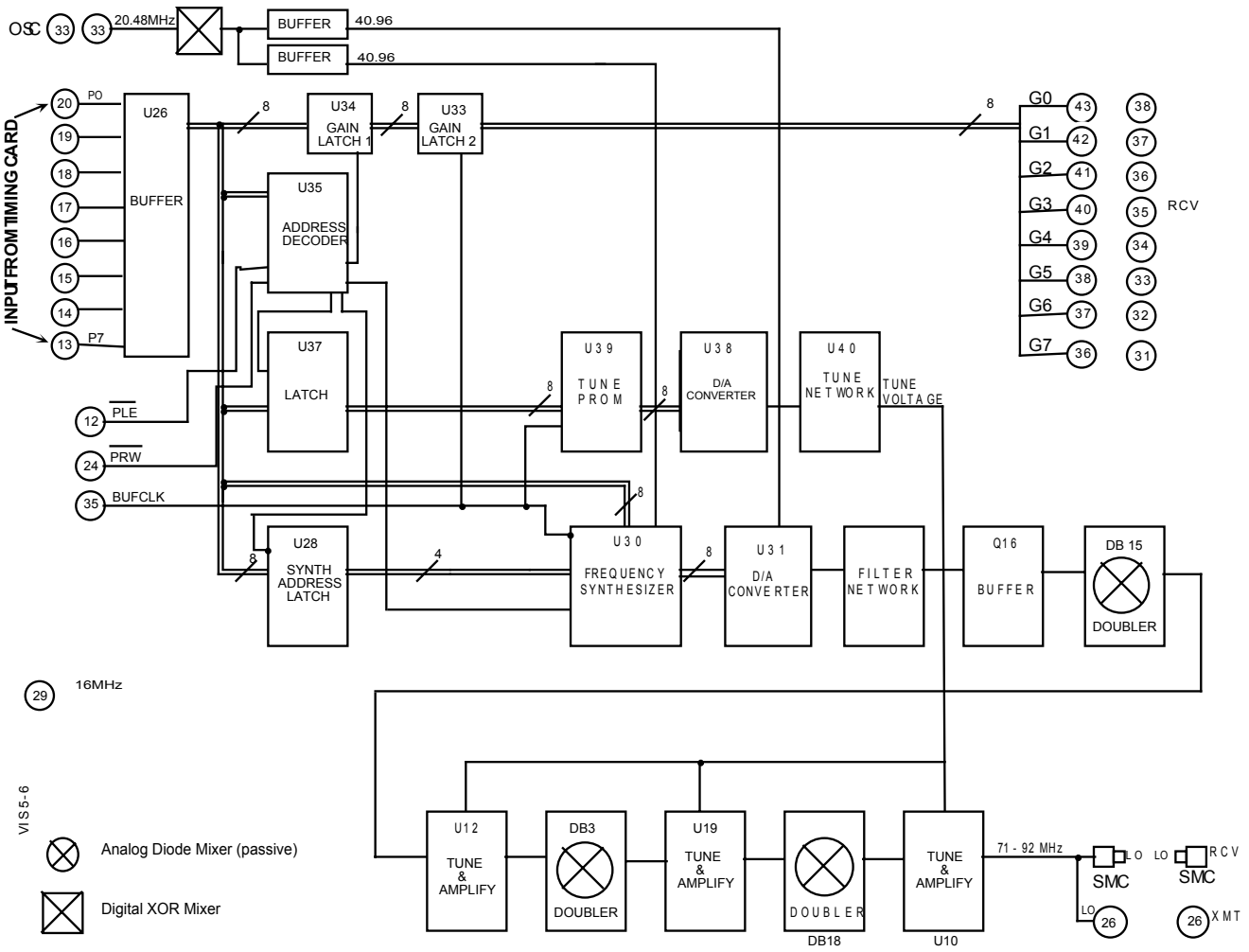

Figure 5-6 Synthesizer Card Block Diagram

523. An auxiliary function of the Synthesizer Card is to latch the gain control byte for the receiver(s). This keeps the noisy P-bus separated from the receiver(s).

Receiver Card

524. Some of the key features of the Receiver (RCV) Card are:

a. Triple conversion to a final IF at 225 kHz, no baseband (the sounder does not use a two channel quadrature scheme but digitally samples the one IF in quadrature).

b. Gain control of the first stage amplifier before the first mixer.

c. A high dynamic range first mixer (+23 dBm LO) handles input signals up to 6 Vp-p.

d. A 250 kHz bandwidth linear phase SAW filter in the first IF of 70 MHz.

e. Distributed gain control by means of variable gain amplifiers, not attenuation.

f. Frequency selectivity is distributed through the receiver as eight single stage 2-pole filters of approximately 100 kHz bandwidth resulting in an overall 34 kHz bandwidth.

g. High level output ±5 Vp-p into 150 Ω, as well as high level RF input levels, maintains a large dynamic range even in a modular chassis with proximity to high speed computer busses and a high power RF amplifier.

h. A buffered output of the RF and first IF envelope is sent to the computer (via the BIT Card) to allow a gain setting which prevents saturation of these stages.

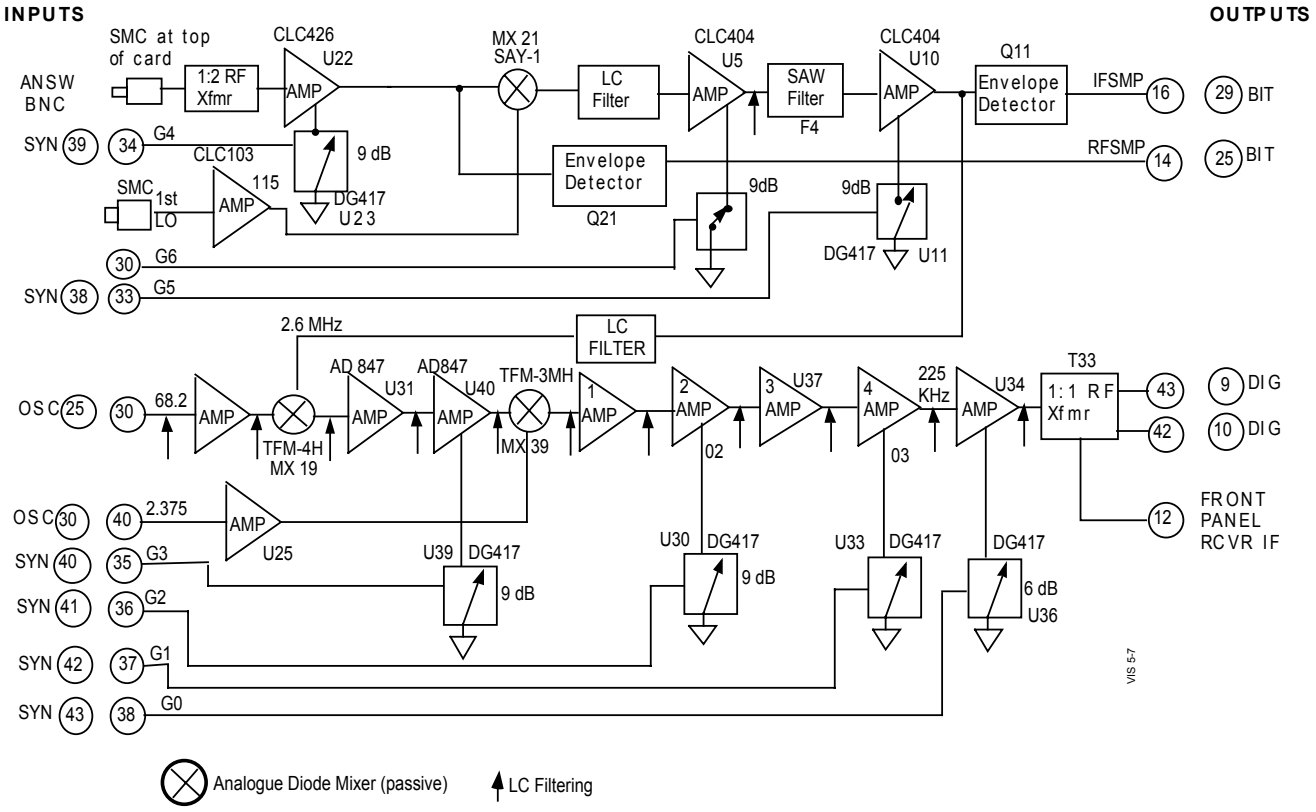

Figure 5-7 Receiver Card Block Diagram

Functional Description of the Receiver Card (Refer to Figure 5-7 above)

525. The input signal from the Antenna Switch enters the card through the SMC female connector at the top of the card. It has already been buffered and over voltage limited such that the maximum input signal level would be ±1.5 Vp-p. This input is stepped up in T24 to match the U22's input impedance. The output of U22 is envelope detected by Q21 to allow the computer to decide what gain to set in U22. U22's output goes to the high level mixer MX21. There it is mixed with the LO input which has been amplified to +23 dBm. The output of MX21 may be as high as 6 Vp-p due to the presence of both the sum and difference frequencies. Therefore, the LC filter here selects only the difference component of 70 MHz to avoid overloading the next ampli-

fier, even if a low gain is selected and to also provide image rejection. Although the signal may experience a 17 dB loss through the SAW filter a variable gain amplifier is provided because the next mixer allows only 6 dB less amplitude than the SAW. Thus the signal is envelope detected again by Q11 to allow the computer to sample the signal level here and decide what gain to apply to U5 and U10. The reason for sampling signal levels at the RF and first IF is that out of band interference could saturate the components here, distorting the amplitude measurement, but go undetected since subsequent tuned stages would filter it out. Most of the signal present after T3 and T20, however, will be seen by the digitizer and computer at the final IF output.

526. MX19 is driven by a +17 dBm 67.48 MHz LO. The output passes through T20 which removes the sum frequency (at 138.2 MHz), provides the first 70 kHz bandwidth filter stage and steps up 50 Ω to 450 Ω. U31 applies a fixed gain to restore the signal level, then U40 is a 9 dB variable gain stage. T40 steps down to 50 Ω to match to MX39, a +13 dB level mixer. MX39's 225 kHz output goes through a series of four independent gain stages in U37, each separated by a 70 kHz bandwidth tuned circuit; two of the four stages are gain controlled. U34, the output amplifier, is gain controlled and T33 provides the final frequency selective filtering as well as providing a differential output. Since this IF signal must travel over 12 inches on ribbon cable to the Digitizer Card it is quite powerful (10 Vp-p into 150 Ω) in order to reduce the impact of inductively or capacitively coupled chassis noise.

Tuner Card

Functional Description of the Tuner Card (Refer to Figure 5-8 on the following page)

527. For stations with strong local interference the Tuner (TUN) Card, located between the Antenna Switch and the Receiver Card(s), improves the performance of the sounder significantly. At the input of the Tuner Card is a 2:1 step-down transformer that distributes the signal from the Antenna Switch to one of the four channels of the card. No switch is necessary at this location because the impedance of the channels that are not tuned to the desired frequency is very high. Thus the noise is not increased at this location. This is the advantage of serial tuning at the input.

528. Serial tuning provides an almost constant bandwidth for each band. The bandwidth is given by the serial resistor and the inductor, i.e.:

$$\Delta f = \frac{Rs}{2\pi \bullet L}$$

For a small bandwidth Rs has to be small which is achieved by a step-down at the input and a step-up at the output of the tuned circuit.

529. After modest amplification with a low noise amplifier a parallel absorption circuit shorts the amplifier's output signal after a 100Ω resistor except for frequencies to which the parallel circuit is tuned. Since parallel tuning is applied, the bandwidth of this circuit is approximately proportional to the square of the frequency, i.e.:

$$\Delta f = \frac{1}{2\pi C}$$

This gives a small bandwidth at the low frequencies of each band. Thus the total bandwidth of the input and the output tuned circuits is approximately proportional to the frequency, this is the goal.

530. To make the parallel output absorption circuit effective without unreasonably large capacities, the inductor is built as a step-up transformer with a turn ratio of approximately four. To minimize noise from any leakage frequency only one channel output is selected by a switch. For BIT purposes another switch allows the Tuner Card to be bypassed with 30 dB attenuation.

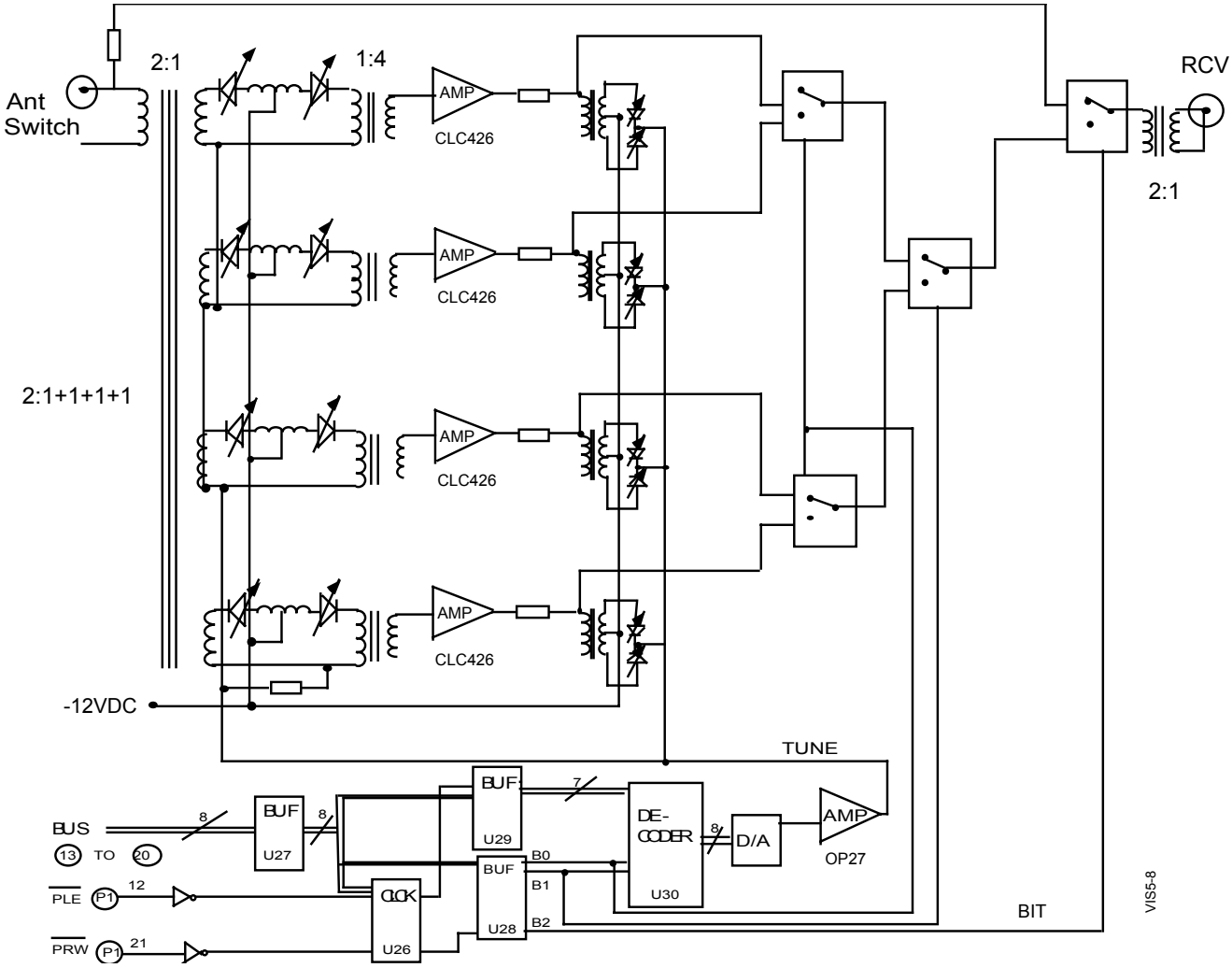

Figure 5-8 Tuner Card Block Diagram

Digitizer Card

NOTE

The DPS-4 Digitizer Card described below may be used in a single- or four-channel sounder without reconfiguration. In a single channel application, only one receiver channel is used.

531. The Digitizer (DIG) Card converts analog signals from the Receiver Card IF outputs to 12-bit digital words. The converted samples are then stored on the Digitizer Card in FIFO memories until the DSP program is ready to upload the samples for processing. The Digitizer Card interfaces directly to the DSP Card via a 50-pin ribbon cable and *does not* communicate directly with the MAIN computer.

Functional Description of the Digitizer Card (Refer to Figure 5-9)

532. For IC Numbers [Unn] refer to the schematic entitled DPS-4 Digitizer - Rev C, Drawing Numbers 6021301-1, 2, 3 contained in the technical data package shipped with the sounder.

533. Four receiver IF signals (225 KHz) are transformer-coupled to the Digitizer Card where they are connected through DG419 analog multiplexers (U5 - U8) to a pair of AD684 quad sample-and-hold (S/H) amplifiers (U9 and U10). The S/H amplifiers sample the analog signals and hold them constant for conversion by the A/D converter. The two S/H amplifiers are clocked 1.11 μsec apart (90° out of phase at 225 KHz). The top S/H (U9) is clocked by the control signal "ReClk" to capture 4 simultaneous samples first (called the real samples), and then the other S/H (U10) is clocked by the control signal "ImClk" to capture 4 simultaneous samples 90 degrees later (the imaginary samples). This process, called quadrature sampling, allows relative phase shifts of the analog signals to be obtained. A total of 8 sampled signals are obtained repeatedly at intervals of 16.67 μsec or 2.5 km height spacing.

534. The S/H output signals are connected one-at-a-time to the A/D converter via an ADG408 8-to-1 analog multiplexer (U11). The multiplexer address is selected by the 3 control signals CH0, CH1, and CH2 (grouped together as "A" on the block diagram).

535. The ADC511 A/D converter (U13) converts each of the 8 analog samples to a 12-bit digital word. Conversion is triggered by the control signal "Start". The A/D output word is sign-extended to 16-bits and connected via a common data bus to four FIFO memories. Control signals "W1", "W2", "W3" and "W4" are asserted accordingly to write the samples into the FIFO corresponding to the receiver on which the sample originated.

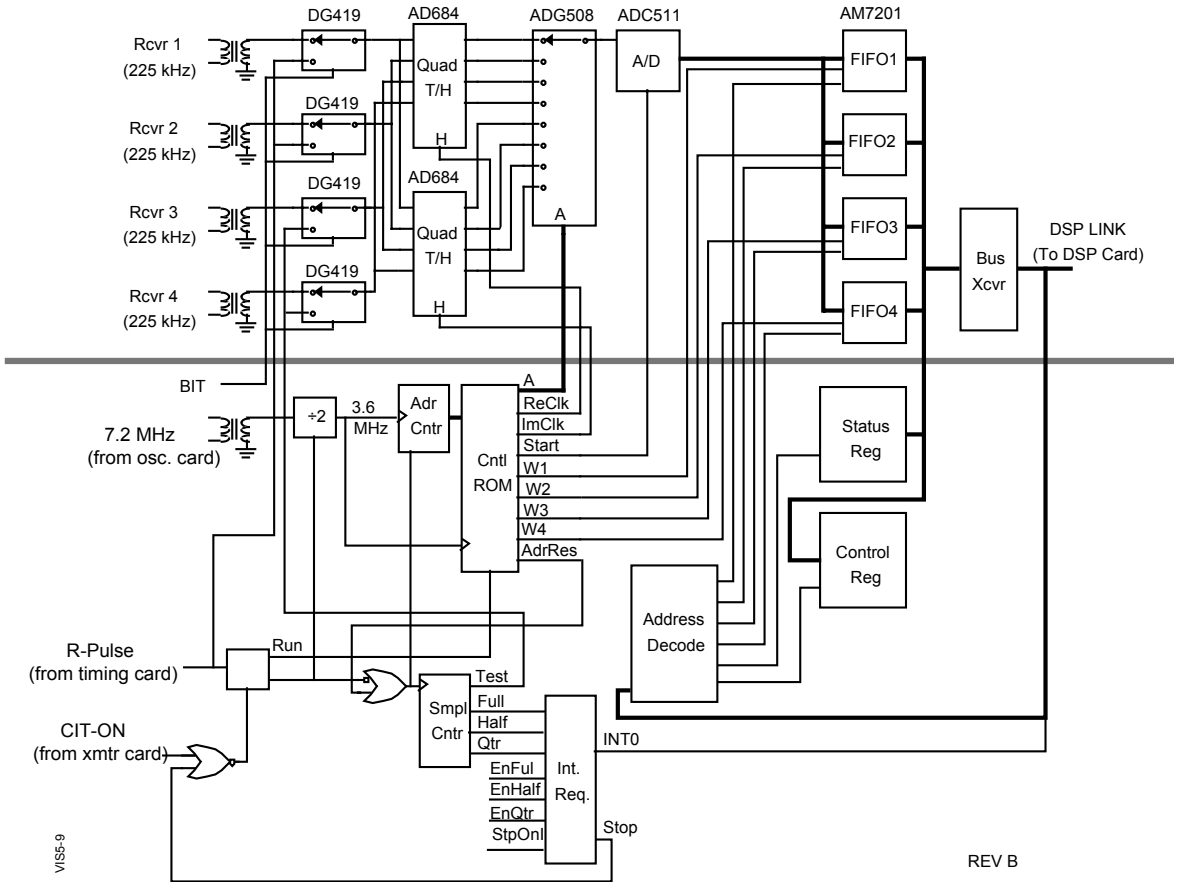

Figure 5-9 Digitizer Card

536. Each of the FIFO memories shown in Figure 5-9 stores up to 512 16-bit samples obtained from one of the four receiver IF signals. Each FIFO channel consists of a pair of AM7201 512 nine bit FIFO chips. The first FIFO (U40 and U44) stores samples from receiver 1, the second FIFO (U39 and U43) stores receiver 2 samples, the third FIFO (U38 and U42) stores receiver 3 samples, and the fourth FIFO U37 and U41) stores receiver 4 samples (in a 4-channel receiver sounder). In a single-channel system, only the first FIFO is used.

537. Samples stored in the FIFOs are read by the DSP Card via the DSP I/O bus. The FIFO outputs are interfaced to the DSP bus via bus transceiver chips (U49 and U50). Samples are read out of the FIFOs when the DSP Card reads from DSP I/O address 5. The specific FIFO is selected by bits in the Digitizer Card control register and is clocked when the address decode circuitry (U48 and U52) detects a read request for address 5.

538. Control signals for generating the various digitizer clock signals are all derived from a 7.2 MHz synchronous clock signal originating on the Oscillator Card. This 7.2 MHz signal is transformer-coupled onto the Digitizer Card and then divided by two by U21 to generate a 3.6 MHz clock. This 3.6 MHz clock is used to drive both an 8-bit address counter (U18) and a registered PROM (U24 and U26). The timing waveforms for the Digitizer Card clock signals are stored in this control ROM. The address counter increments the ROM address until the AdrRes control signal is asserted by the ROM. When this happens, the ROM address resets and the clock waveforms repeat.

539. The Digitizer Card is armed to begin sampling by the signal CIT-ON which originates on the Transmitter Card. Once armed, the digitizer is triggered to begin sampling by the falling edge of the R-Pulse (from the Timing Card) which coincides with the end of the transmit pulse. That is, the digitizer starts sampling only after transmission ends, since the receiver outputs would be saturated during transmission. The falling edge of the R-Pulse sets the Run Flip-Flop (U21) which remains on until the end of sampling.

540. During sampling, the digitizer's sample counter (U34 and U33) counts how many samples have been acquired. When enough samples have been taken, the interrupt request circuitry (U29, U30, and U34) generates an interrupt request to the DSP Card. The DSP Card responds to the interrupt request by reading the samples out of the FIFOs.

541. Generally it may be necessary for the DSP Card to empty the FIFOs several times for each transmit pulse. When the DSP Card determines that 512 complex height samples have been taken it will signal the digitizer to stop sampling by asserting the control register bit STPONI (stop on interrupt). If STPONI is asserted, then U21 will be reset on the next digitizer interrupt, causing the sampling process to terminate.

542. For purposes of testing the Digitizer Card operation, a pair of BIT signals may be sampled in place of the receiver outputs. The R-pulse is applied to two of the digitizer channels, and a special test signal generated on the Digitizer Card is applied to the other two.

Antenna Switch

Functional Descriptions of Antenna Switch Variants (Refer to Figures 10A and 10B on the following pages)

543. Four identical input stages (T1, 2, 3, 4 and U1, 2, 3, and 4) receive signals from each of four receive antennas. The block diagram is shown in Figure 5-10A. The input Jx1, Jx2 (x denoting the antenna number) comes via short wires from BNC connectors mounted on the side of the Antenna Switch's RF shielded enclosure. These connectors are connected to lightning suppressers to isolate the chassis from current surges (induced by lightning or power faults) picked up on the 160 to 320 m RF coaxial cables coming in from the antenna field. Also, the DC voltage to power the receive antennas pre-amplifiers is applied to these cables: +16.5 V or +22.5 V switched voltage (O/X from J7.5) is applied to the center conductor (+16.5 V signals the pre-amplifier to use left-hand circular polarization while the 22.5 V indicates right-hand polarization). O/X enters from the Power Distribution Card through J7.5. T1, 2, 3 and 4 match the 50 Ω signal from the coaxial cables to input impedances of U1, U2, U3, and U4. DX1 and DX2 limit saturation from the transmitter pulse to ±0.7V. J7.2, J7.10 and J7.12 bring in the antenna selection bits (A_0, A_1, and A_2) written to the latch on the Timing Card. These lines are inverted in U7 which is a four-channel inverting buffer.

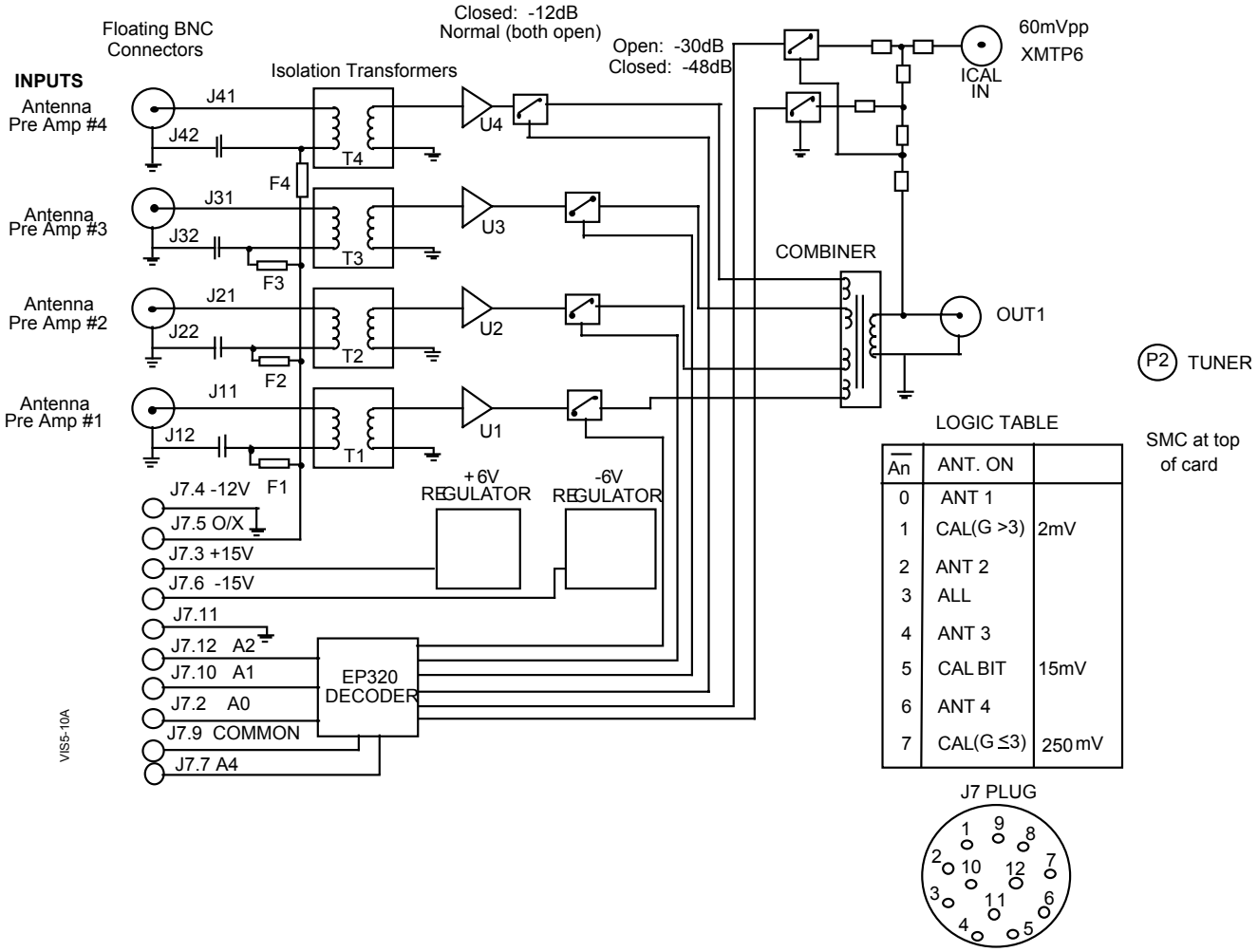

Figure 5-10A Antenna Switch Block Diagram

Alternate Design #1

544. U5 is configured as an eight-channel wideband multiplexer. Based on A_0, A_1, and A_2 inputs U5 selects either the CAL RF signal, the sum of the four antennas (formed by the resistor network R18, R28, R38, and R48) or one antenna only. All voltages for the IC's are derived from +15 V (from J7.3) and –15V (from J7.6) while the card ground and common pin (J7.11) is grounded to chassis ground.

Alternate Design #2

545. The outputs of the four amplifiers U1-U4 are switched by U9, U10, U11 and U12 to either apply or disconnect their outputs from a 4-way power combiner, U5. When disconnected the analog switches present a 50 Ω resistance, therefore the output of U5 is either a single antenna or the in-phase beam of the four antennas.

Antenna Switch [4-Channel Sounder]

546. The above Antenna Switch description for the sounder, regarding input, isolation, and O/X switching is identical for the 4-channel sounder variant. The one exception is the deletion of switches U10, U20, U30, and U40 which are not needed in the 4-channel variant since the switchbox inputs are not multiplexed to a single output.

547. The four inputs are fed through transformers T1-T4, then through op amps U1-U4 into analog switches U11, U21, U31, and U41. The second input to the switches is a calibration signal generated on the Transmitter Card. The choice of switching between the antenna inputs and calibration signal is software controlled by the CAL signal on the J7 plug to the switchbox. The calibration signal level is dependent on the gain setting selected by the user in the DPSControl menu. The software configures switches U5 and U6 to attenuate the level to 75mV, 2.5mV, 650uV, or 160uV. The four outputs of the antenna switch, either antenna signals or calibration signals, are fed out of the switchbox on SMB connectors, into the top of the (four) Receiver Card(s).

Polarization Switch

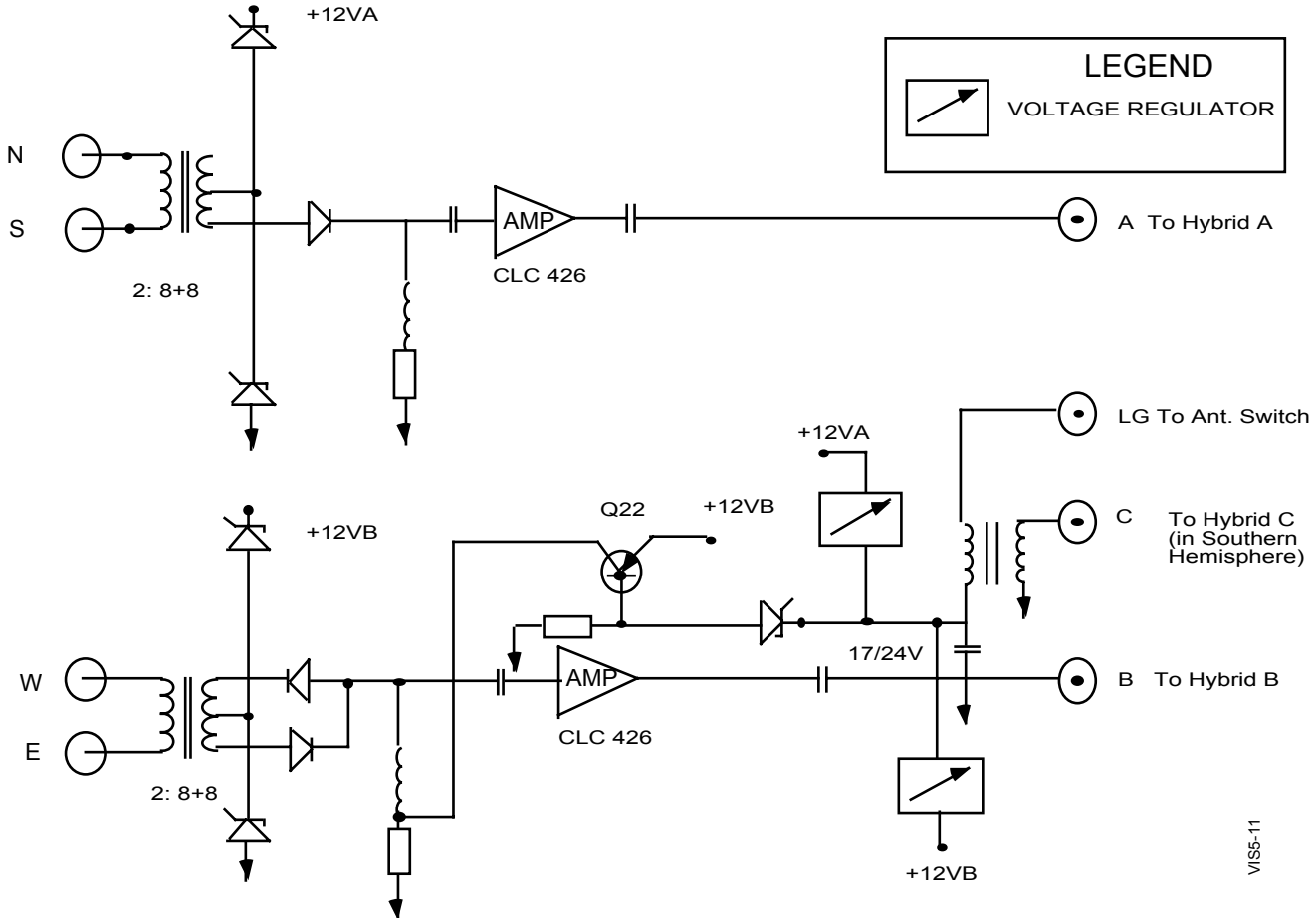

Figure 5-11 Polarization Switch Block Diagram

Functional Description of the Polarization Switch
(Refer to Figure 5-11)

548. With two channels, one for the North (N) – South (S) loop and another for the West (W) – East (E) loop, the Polarization Switch (Fig 5-11) allows the receiver to receive circularly polarized signals arriving from overhead (i.e., small zenith angles) and to change the desired sense of rotation of the polarization vector.

549. For that purpose a 90° phase shifter is attached to the two outputs of the low-noise amplifiers which are equal to within 1 dB in amplification for the whole frequency band used. Thus the two channels are almost equal in design although only the W–E channel is switched.

550. Polarization switching is accomplished by switching the DC power fed through the same cable that brings the RF signal to the Antenna Switch. Two voltage regulators make the voltage (12 VDC) applied to the amplifier independent of the supply power, which changes between 17 and 24 VDC. This change is sensed by a transistor, the base of which feeds this voltage to a Zener diode.

551. The transistor current or the current to ground make one of the two diodes conduct which connects one or the opposite output of the input transformer to the W–E amplifier. This 180° change in one of the two channels provides the polarization change of the turnstile loop antenna with the help of a 90° wideband hybrid adder.

552. For signals arriving from remote stations with larger than 45° zenith angles the suppression of unwanted polarization depends strongly on the orientation of the turnstile antennas. An optimum configuration would be for the loop planes to be ±45° off the direction toward the remote sounder.

Power Distribution Card

Functional Description of the Power Distribution Card (Refer to Figures 12A and 12B)

553. Power distribution within the sounder chassis is centralized in the Power Distribution (PWR) Card (shown in Figures 5-12A and 5-12B). Fusing (with self-resetting overload devices), voltage regulation and current limiting are applied as necessary. Along the top of the card are LED's to indicate the presence of various voltages. Red LED's indicate a positive voltage, green indicate negative voltages and amber indicate the 24 V – 28 V input power for each DC/DC converter. An auxiliary function of this card is to switch the voltage level of the power sent to the magnetic loop preamplifiers to switch received polarization sensitivity (left-hand and right-hand circular). The card also provides a mounting for the DC/DC converters and collects several BIT signals into connector P8 to output them to the BIT Card. Figure 5-13 on Page 24 shows the overall power distribution within the sounder system.

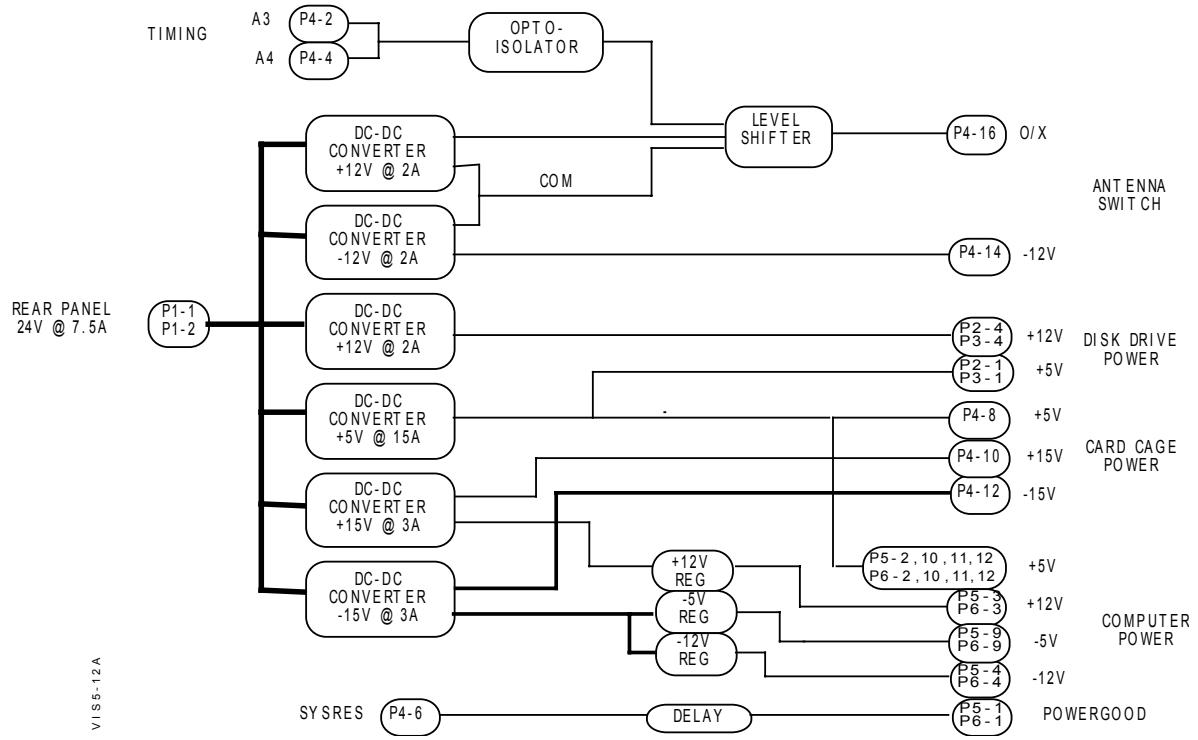

Figure 5-12A Power Distribution Card Block Diagram (System Power)

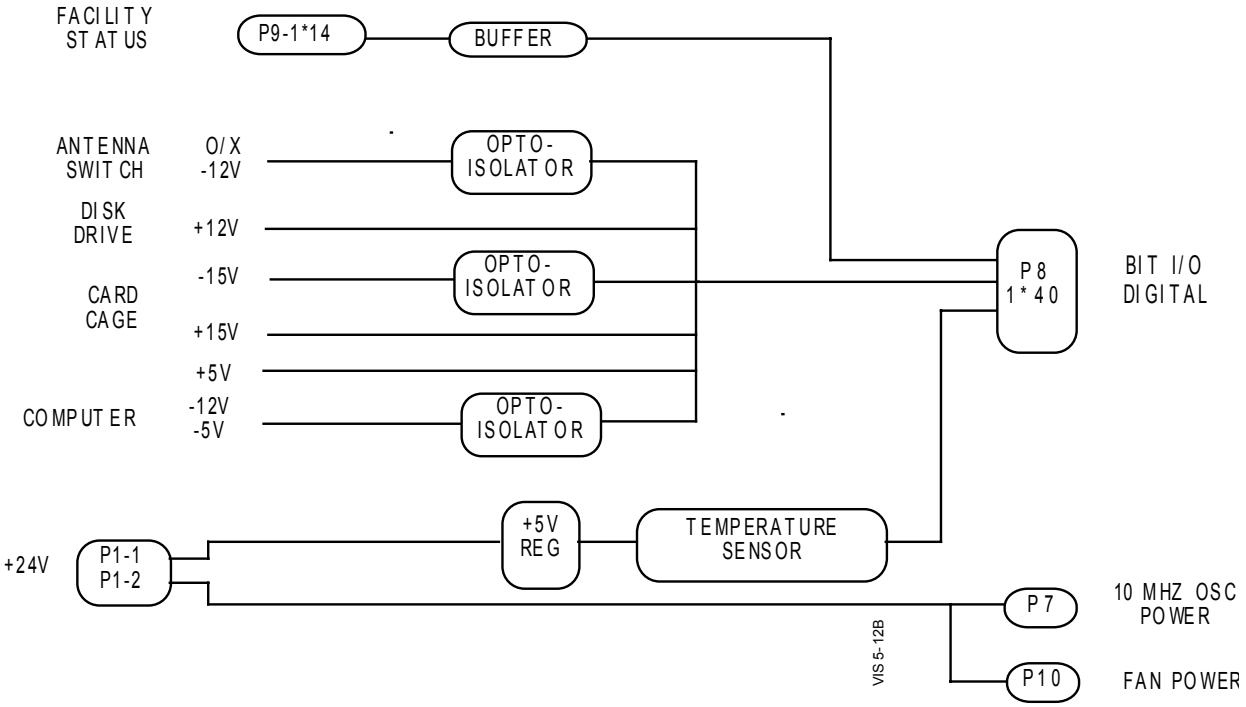

Figure 5-12B Power Distribution Card Block Diagram (BIT Card Interface)

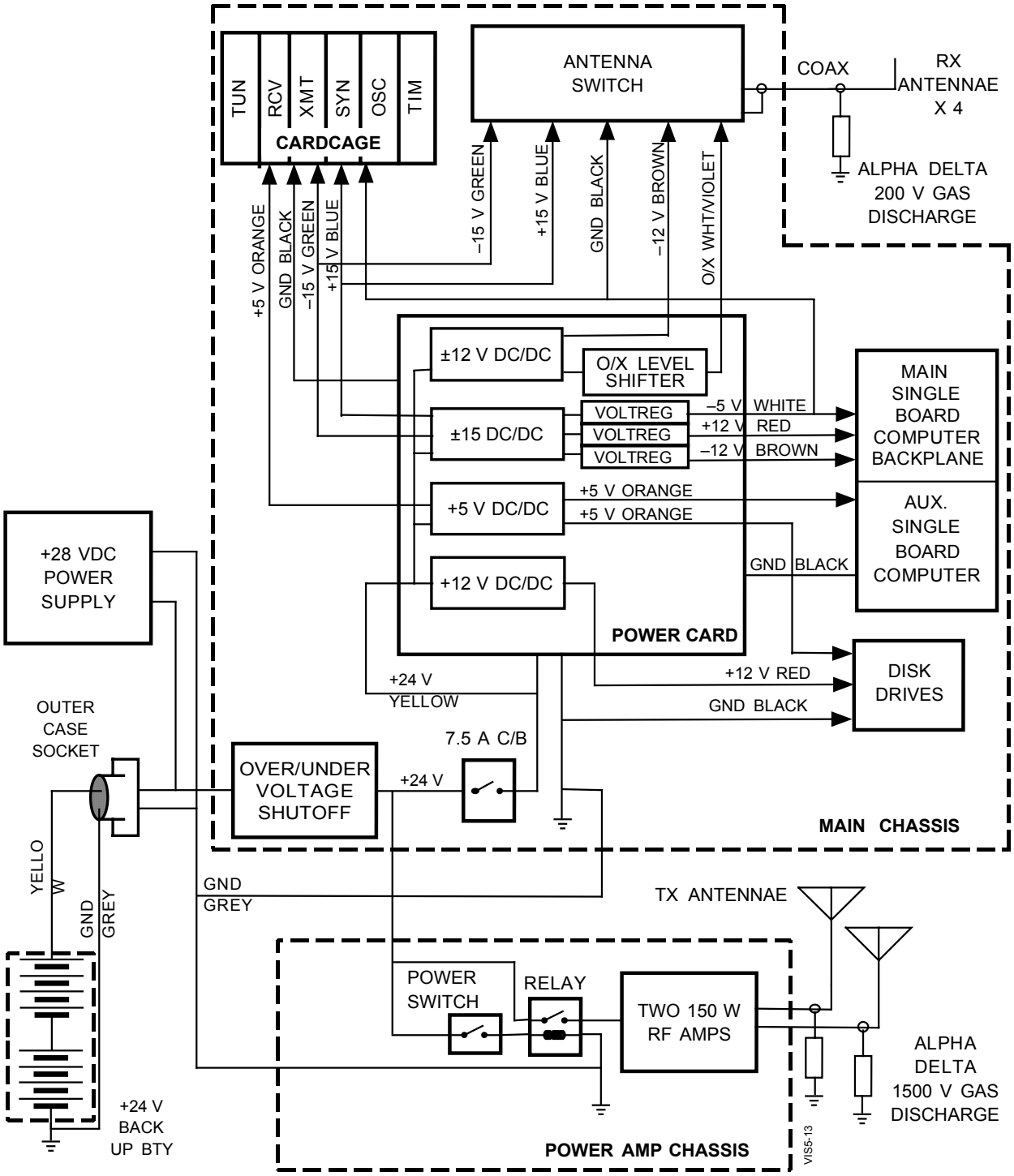

Figure 5-13 DC Power Distribution Block Diagram

Battery Interface Box

Functional Description of the Battery Interface Box

(Due to Simplicity, Refer to schematic SC6010101-01)

554. The functions of the battery interface are to provide:

a) current to the VIS chassis, the RF Amp, and the cooling fans

b) overvoltage protection

c) an undervoltage shutdown

d) overcurrent protection

e) a timer to re-attempt powerup if a shutdown occurs

f) a meter to observe the batttery/+28V power supply voltage.

555. After an initial delay of 10 seconds by the 555 timer (U6), the two parallel P-channel power MOSFETS (Q4 and Q5) are turned on, and current is provided to the RF Amp, VIS chassis, and cooling fans through the terminal strip connections on top of the Battery Interface Box housing.

556. Overvoltage is monitored by the voltage divider R35, R39, and R30 and the comparator U3. If there is an overvoltage condition, the comparator changes state and the power FETs and LED shut off.

557. Undervoltage is similarly monitored by the divider formed by R31 and R34. If the voltage drops below the set threshold, shutdown occurs.

558. Overcurrent is sensed by the voltage drop across the drain and source of the power FETs Q4 and Q5 by the voltage divider consisting of R51, R52, R53, and R54 in conjunction with the divider used by the overvoltage circuit.

559. If any of the failure conditions shut the interface down, the 555 timer will re-attempt powerup. If the cause of shutdown is no longer present, it will powerup successfully. Shorting J8 and J9 is a means of externally disabling the timer interface.

RF Power Amplifier Chassis

560. The RF Amplifier consists of the aluminum chassis drawer, a power relay (24V solenoid) for switching the +26.5V input from the battery/power supply. The power relay is controlled by the front panel switch and by an FET on the RF Amp card which is commanded by input from the upper chassis via the RF Amp IO connector. The chassis also houses the dual channel RF Power Amplifier card, with two independent amplifiers both capable of 150-200W output, and the two Half-Octave Filter (HOF) cards. The chassis front panel green LED displays the presence of primary power to the cards, and the two amber LED's indicate the presence of transmitted power being output to the antennas from each of the two independent amplifiers located on the RF Amplifier card.

RF Amplifier Card

561. The RF Amplifier is comprised of two independent wideband amplifiers (referred to below as the two channels) consisting of three stages, two drivers and a final (see Figure 5-14). The input signal to each amplifier channel is 1.4Vp-p, falling off slightly at the higher frequencies. The input cable is terminated in a PI attenuator made up of a 68, 330, and 68 ohm resistors where the 220 ohm is bypassed by a 68p capacitor to boost up the high frequency output. Each input stage (comprised of a Motorola hybrid module) amplifies 10mW up to 0.5W. The output of the second stage is 20W (40Vp-p across 22 ohms at the input to the final) and the output

of the final stage is 200W. The entire 10 inch x 6 inch board is mounted to a 10 inch by 6 inch heat sink. The input voltage is the system's primary power of 25 to 28VDC, from the power supply and the batteries in parallel, via the battery interface box. This input voltage is protected through a 15A fuse (not shown on the block diagram) at the input of the 25 to 28V DC to the board. The primary power is applied at the output end of the amp board where it feeds power, via the center tap on the primary of the 1:6 wideband transformers, to the 300V output stages. It is also routed back off the board to a twisted pair which runs down the underside (the fin side) of the heatsink to feed power to the small signal end of the board. Keeping this twisted pair on the back side of the AMP heat sink reduces coupling between output RF and input power, thus reducing the danger of a positive feedback situation (i.e. oscillation).

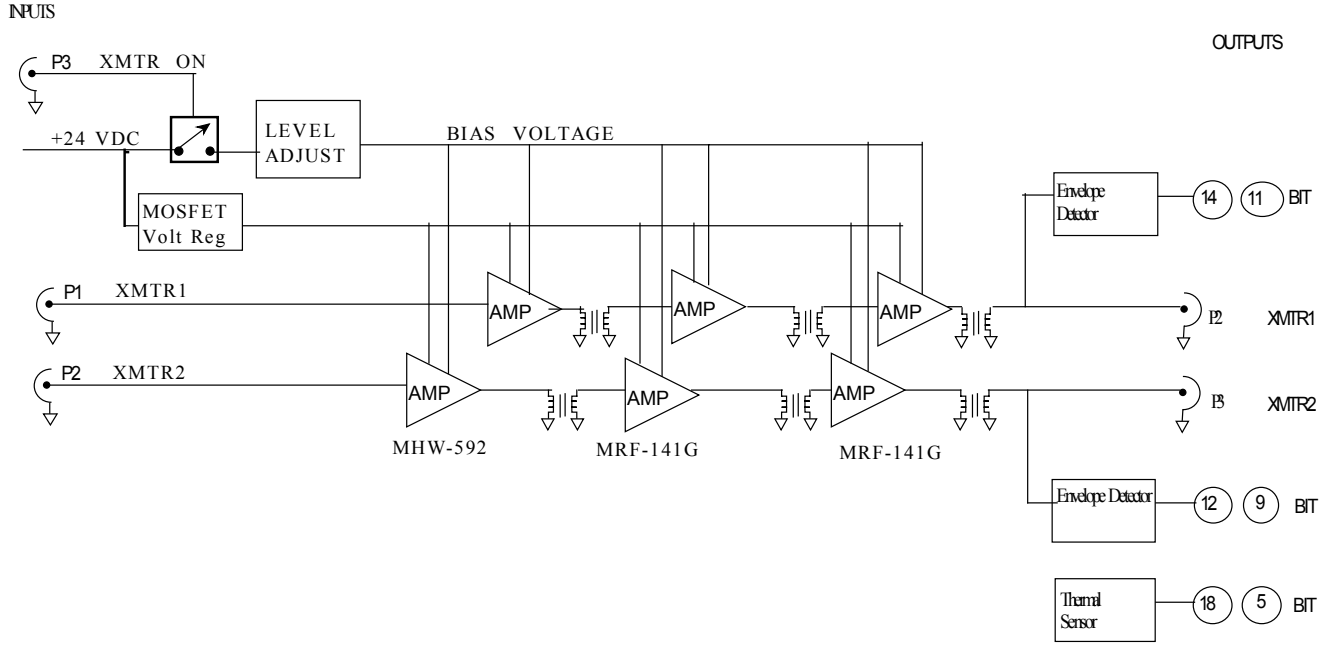

Figure 5-14 RF Power Amplifier Card

562. The critical setting in the RF AMP is the bias voltage set by R67/147 for the input stages and R107/187 for the output stages. The bias voltage is pulsed, rising when the R BNC signal (Xmtr On from the regulated front panel input from the upper chassis) rises. The R BNC, via U41 and Q52/53 also applies the regulated +18V to amplifiers A1 and A2. The turn-on voltage for various batches of MRF-141G MOSFET transistors varies widely, but the bias voltage needed to set an idle current of about 2A is usually in the range of 2-4V. When the negative swing of an input sine wave exceeds 1V below the bias level, the FET is in its non-linear cutoff range, thus causing harmonic distortion in the output signal. The input and feedback resistors linearize these amplifiers greatly since the gate voltage becomes a virtual ground (i.e. the signal should theoretically approach zero since the output is inverted compared to the input and is larger by the same ratio as the feedback resistance–to-input resistance).

563. The design of the wideband transformers is crucial. A transmission line transformer needs to be constructed with a transmission line which has an impedance which is the geometric mean of the input and output

impedances. For instance, matching a MOSFET output impedance of 2 ohms (1.5 ohms augmented with the 0.5 ohm resistors) to a 50 ohm output impedance requires a 10 ohm transmission line.

Half-Octave Filter (HOF) Cards (2 per system):

564. Since the harmonic content of the RF Amplifier is too high for most frequency allocation agencies to authorize, the final output is passed through one of eight low-pass filters, depending on output frequency. The switch points are controlled by software in the Armenu.dps file. The upper cutoff frequency in MHz for each band is given as (parenthesis show default Armenu switch points for systems operating over a 1-40MHz band):

1. 1.74 (1.74)
2. 2.45 (2.45)
3. 3.85 (3.85)
4. 6.55 (6.55)
5. 10.95 (10.95)
6. 16.15 (16.15)
7. 28.1 (28.10)
8. 42.0

The filter channel is selected by 3 digital bits F0-F2 from the upper chassis (originating in the SYN card, and fed through the 25-pin AMP IO connector) which activate reed relay switches which conduct the RF signal to the selected filter. Two more bits F3 & F4 command the two output switches (also RF reed relays), directing the power to one of two antennas. Nominally one antenna is oriented for vertical incidence (thus VIS) and the other is oriented for oblique incidence (thus OIS). The LS138 logic IC's decode the F0-F2 bits and the high voltage (+18V is connected through the solenoid winding to the IC's output pin) open-collector non-inverting buffer (7407) provides the drive to pull down the solenoids of the appropriate switches (see Figure 5-15).

Cards and Assemblies Supplied from other Manufacturers

565. There are cards and assemblies provided by external manufacturers that are integrated into the digisonde. For simplicity, reference is directed to the applicable literature provided with each of these cards and assemblies. Copies of these documents are shipped with each VIS. For additional copies please contact:

University of Massachusetts Lowell

Center for Atmospheric Research

600 Suffolk St.

Lowell, MA 01854

Reinisch@cae.uml.edu or http://ulcar.uml.edu

A listing of these card assemblies and applicable commercial documentation is provided in Table 5-1.

Table 5-1 Listing of Commercial Peripheral Literature

Board/Assembly Description	Manufacturer	Document Title
GPS Receiver	Trimble Navigation	Smart Antenna Devoloper's Guide, Acutis, Acutime, Acutime II

		Acutis, Acutime, Acutime II
BIT I/O Board	Cyber Research	CYRDAS 1200 User's Guide
PC Flash Disk Board	Industrial Computer Source	Model PCFD, TFD Series Product Manual
Digital Signal Processor Board	Bridgenorth Signal Processing, Inc.	DSP Development and Data Acquisition User's Guide