HF RADAR MANUAL

VOLUME 1

General Description
System Internal Interfaces, Timing,
and Operation Sequence; Housekeeping ADC;
Temperature Monitors

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1. INTRODUCTION

1.1 General

The Space Environment Laboratory HF Radar is a new general purpose radio frequency pulse sounding system intended for research purposes. It covers the frequency range 0.1-30 MHz and with suitable antennas is capable of making nearly all of the remote sensing measurements of the ionosphere which can be made by coherently receiving pulsed signals reflected from the ionosphere either monstatically or bistatically. This flexibility is achieved by the incorporation of a general purpose computer as the heart of the system. In this respect, the system is a logical development of the Dynasonde (Wright 1969; Wright and Pitteway, 1978). The primary objectives are:

1. To provide a system with the minimum of hardware-bound restraints to the characterization of signals returned from the ionosphere. This implies digital data processing techniques and requires the modes of operation to be defined and controlled almost completely by software.

2. To provide a system which is capable of self-contained real-time data analysis and display to an extent permitting the geophysical significance of the measurements or their required resolution to be used in the manual or automatic control of data acquisition.

The basic measurements to be made on signal returns are:

1. The complex (vector) numerical description of signal returns versus range and frequency, to permit the amplitude, phase, envelope group delay, $\Delta\emptyset/\Delta f$ group delay, and doppler spectrum to be obtained.

2. The comparison of echo data from an array of receiving antennas to permit a measure of the direction of arrival, wave polarization, and other diffraction pattern information.

3. The comparison of echo data at closely-spaced times for doppler, group-rate, and other time-dependent information.

The system is also well adapted to increasing the range resolution by transforming a set of closely spaced frequency samples (Devlin, et al 1977).

Secondary objectives of the system are to function cooperatively with other sounders in a network to provide information on oblique propagation paths, to function in a spectrum surveillance mode to provide information on oblique propagation from known transmitters, and to accommodate data from other geophysical sensors.

1.2 System Philosophy

One of the first decisions is the choice of the form of the transmitted signal. Ionospheric sounding systems have developed in two different directions since the early 1960's from the basic pulse sounder developed in the 1930's. In one, pulse sounding has been retained and combined with numerical data recording techniques. Signal enhancement by averaging or the use of coded pulses has been used where necessary to improve numerical accuracy and sensitivity (Bibl 1978). In the other direction, a completely different form of coding, FMCW, uses a linear frequency swept transmitted signal, in which the time domain dispersed signal returns are transformed to frequency dispersed returns; spectrum analysis is required to express the signal return in the ionogram form (Barry 1971). This permits the use of essentially CW transmission giving high average power without the complication of producing high peak powers. It is very effective in rejecting interference from fixed frequency communication signals. Most of the applications have used analog presentation of the output data but high quality numerical data can be obtained by Fourier Transform analysis. In general, and particularly where crossmodulation in nearby systems is a problem, FMCW produces less interference to the normal uses of the spectrum than does a pulse sounding system.

In research applications of ionospheric sounding, it is important to trade frequency resolution and time resolution, depending on the electron distribution and the dynamics of the ionosphere. Indeed, it may be desirable to interleave frequency sweeps and high time resolution sounding at a few selected frequencies. This would be much more complex to achieve with an FMCW system than with a pulse sounder. Another requirement is the sampling of multiple receiving antennas. A single channel receiver can be time shared between antennas with FMCW provided the switching rate is chosen to place the side bands generated outside

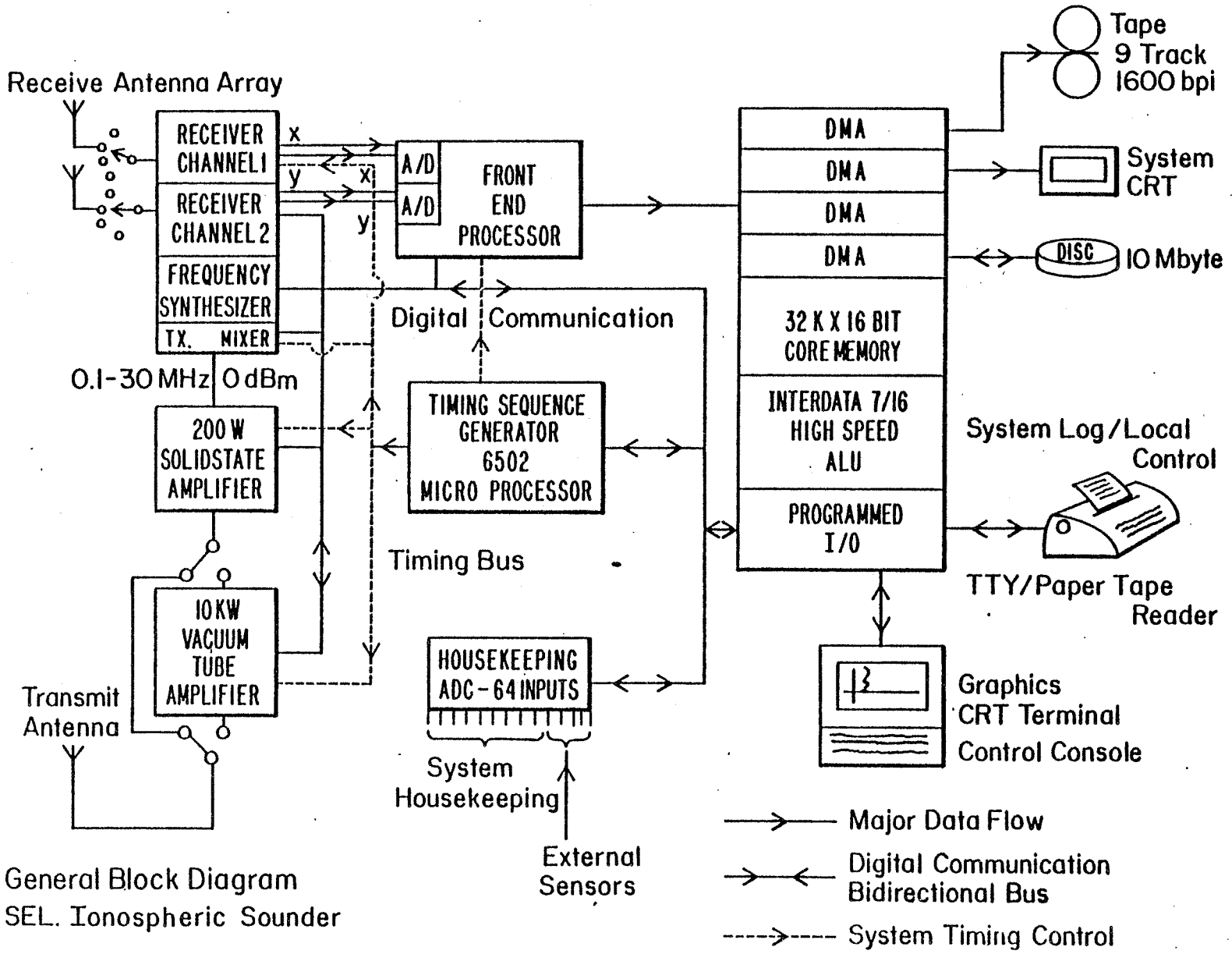
the final analysis range. Multichannel receivers are more usually used. In the pulse system, any combination of sequential sampling or parallel sampling using multiple receiver channels is easy to implement. Although these problems with FMCW could be overcome and might be considered a reasonable counterbalance to the advantages, the major problem is in the increased complexity of the data processing. To obtain the simple virtual height information, if it is to be done numerically, requires one Fourier transform, and if the doppler spectrum of a time series of returns is needed, two transforms are required. This considerably increases the complexity and power needed in the data processing system and also its cost.

The foregoing factors lead to the choice of a basic pulse sounding system with software controlled options for signal enhancement using pulse-to-pulse integration and/or pulse coding. The latter can be implemented using the complementary codes which are used in pairs and, unlike Barker codes, have theoretically zero side lobes in their autocorrelation function (Golay 1961). Two receiver channels are provided so that a single phase comparison can be made between receiving antennas without any restriction on the phase rate of the process being observed, and to double the potential data acquisition rate of the system.

1.3 System Design

A simplified block diagram of the system is shown in Figure 1.

The main processor is a 16-bit Interdata model 7/16 or an 8/16 with 32 K words of 1 μs core memory. Hardware multiply and divide, and hardware floating point registers are incorporated. Typical instruction execution times are 1 μs for a register to register addition, 10 μs for a fixed point 16-bit divide and 48 μs for a 32-bit floating point divide. The processor instruction set is implemented through microcode and is very comprehensive. Input/Output (I/O) communication is carried out through a separately multiplexed bus structure which permits both programmed I/O and Direct Memory Access for block data transfers. Standard peripherals are a 1600 bpi, 9-track, 35 ips tape transport for program loading and data recording, a 10 Megabyte disc memory, one half of which is a removable cartridge disc. A Tektronix graphics display console and hard copy unit form the primary operator interaction point and can in principle be located remotely from the rest of the system; a Model 33 TTY and paper tape reader/punch are used for system logging and initial bootstrap if required. An automatic bootstrap loader permits easy restart under most conditions. Special purpose peripherals are the interfaces to the two other processors described below and to the local system graphics display.



General Block Diagram
SEL. Ionospheric Sounder

FIGURE 1

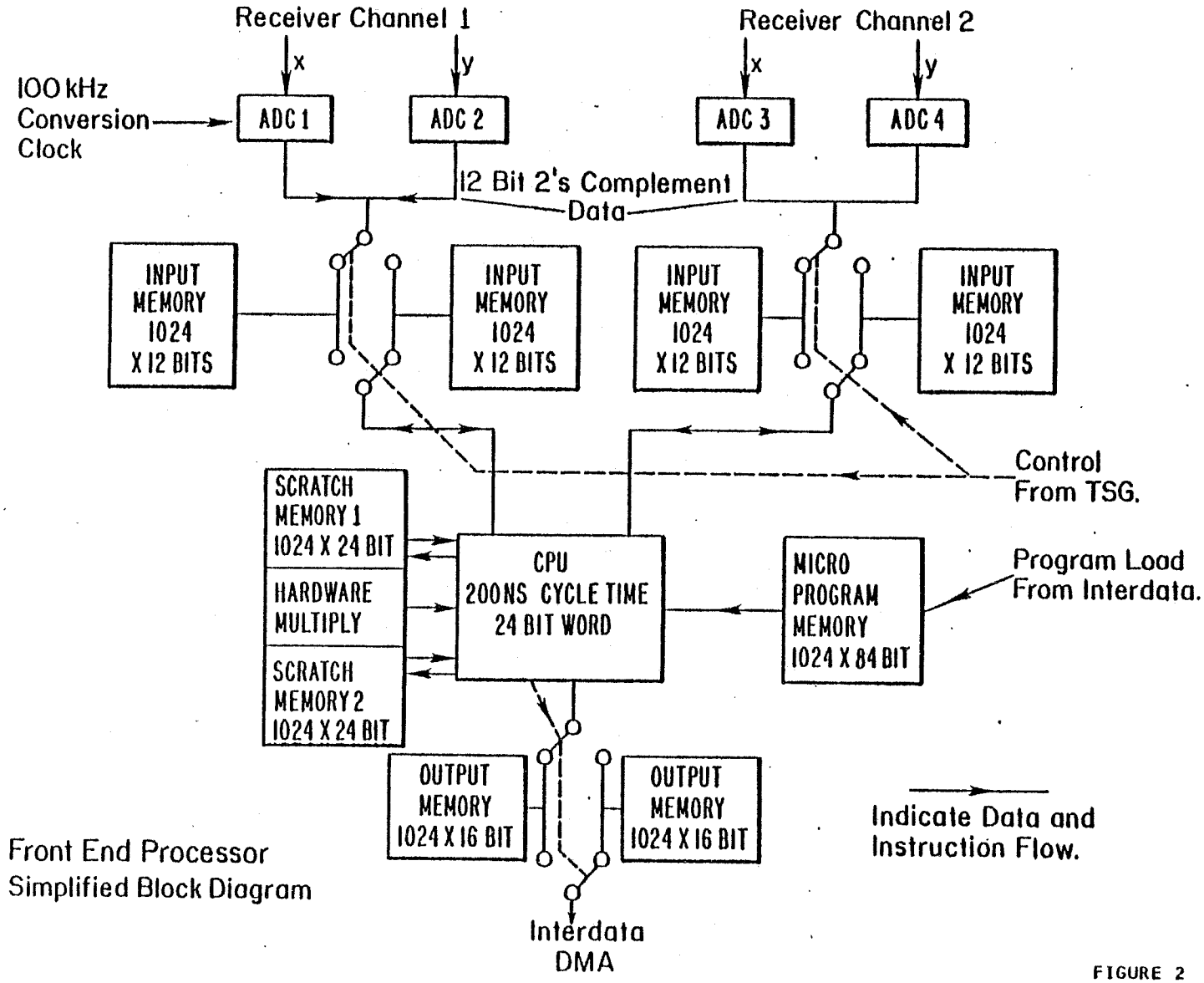
A separate 15 cm XY CRT display with 1024 x 1024 addressable points is intended as the primary local operator graphics display and for local photographic data recording. Both point addressing, vector, and alphanumeric modes are provided. The display is refreshed by direct memory access to the Interdata computer core memory making possible rapid changes in the display for time sequence presentation of the data. The display formats are entirely determined by software and are not predetermined by hardware. The capability also exists for light pen interaction with the data displayed. In addition, the CRT can also be used in standard XY and YT modes to display system timing lines and signal returns in an A-scan mode.

It is not practical to carry out all of the programmable functions needed to meet the system objectives directly with one central processor, particularly since it is desired to have software for general purpose interaction, data processing, and program development coexist with the sounder operating software. The two most time-consuming and routine functions are the generation of the precise timing sequences needed to initiate a transmitted pulse and in the processing of the returning echo data. In the latter operation, a large amount of data must be processed at comparatively high speed to perform initial signal processing, which is needed to reduce the volume of data before it is passed to the main processor. One approach to this problem would have been to build special purpose digital and analog interfaces directly controlled by the main processor. This would have restricted the modes of operation of the system to those which had been foreseen as needed in the original design. The alternative which we have adopted, and which has been made practical by the advances in microprocessor technology, is to use a distributed processing system in which the timing functions and the "front end" signal processing are handled by separate program-controlled processors. These are slaves to the main processor in that they rely entirely on it for nonvolatile program storage and user interaction. Programs for both are loaded from the Interdata 7/16 via a general purpose 8-bit digital I/O bus (DIO) which is used to communicate with the system for control and status monitoring purposes.

The Timing Sequence Generator (TSG) uses a 6502 8-bit microprocessor. This executes a program which provides control interaction with the other parts of the system and exercises 8 general purpose timing lines allocated to various control functions such as transmitter keying and receiver data acquisition gating. The timing is controlled by a sequential state look-up table which contains the states required and the time

intervals between them. The time intervals are restricted to integer multiples of 10 μs with a minimum of 30 μs between state changes. This is not generally restrictive considering the bandwidth of the RF system. Timing coherence is ensured by reclocking the microprocessor outputs with the system 100 kHz clock, although the microprocessor clock is itself locked to the system clock. Up to 8 separate timing sequences or "scenarios" are stored in the microprocessor program and can be called by a control word from the Interdata. Two are used in system "no op" modes and the remaining 6 are available as mode selections. If necessary more could be made available by reloading the microprocessor memory from the Interdata.

The general arrangement of the Front End Processor (FEP) is shown in Figure 2. The structure is designed to permit "pipelined" flow of data from the receiver through the processor and into the main CPU. Two sets of input memories are alternately loaded with data from the ADC's and operated on by the FEP following each transmitted pulse. Similarly, one output memory is being loaded by the FEP CPU while the other is transferred to the Interdata. The FEP is implemented with Schottky LSI 4-bit slice ALU's and control building blocks. The CPU is 24 bits wide to permit fixed point manipulation of the products of the input 12-bit numbers. As the programs are expected to be largely repetitive and of the continuous loop variety, no macro code interpretation is provided, and the program is executed directly from an 84-bit wide microprogram memory which is loaded from the Interdata. This program memory cannot be modified by the FEP CPU itself. Working memory space is provided by the two scratch memories, each 1024 x 24 bits wide. These memories may be addressed in parallel or independently and the required output (or that of a high speed hardware multiplier which multiplies the contents of the addressed memory locations) are selected by a program controlled multiplexer. Sixteen internal general purpose registers are also available within the bit slice ALU for temporary storage. Whenever possible within the FEP, the data flow is pipelined so that operations can be carried out concurrently and at maximum speed. The execution time for one microcoded instruction is one 200 ns clock cycle. This includes all simple fetch, add and subtract, logical compare, and write operations, which for favorable source and destination locations, may be executed concurrently in one clock cycle. The output of the 12-bit x 12-bit multiplier is available in a maximum of 3 clock cycles. With the system transmitting 50 pulses per second, 20 ms is available for processing the data from both receiver channels permitting a maximum of about 10^5 microcode steps (50 per data sample in the normal mode). The size of the output memory presupposes reduction in data volume by at least a factor of 2



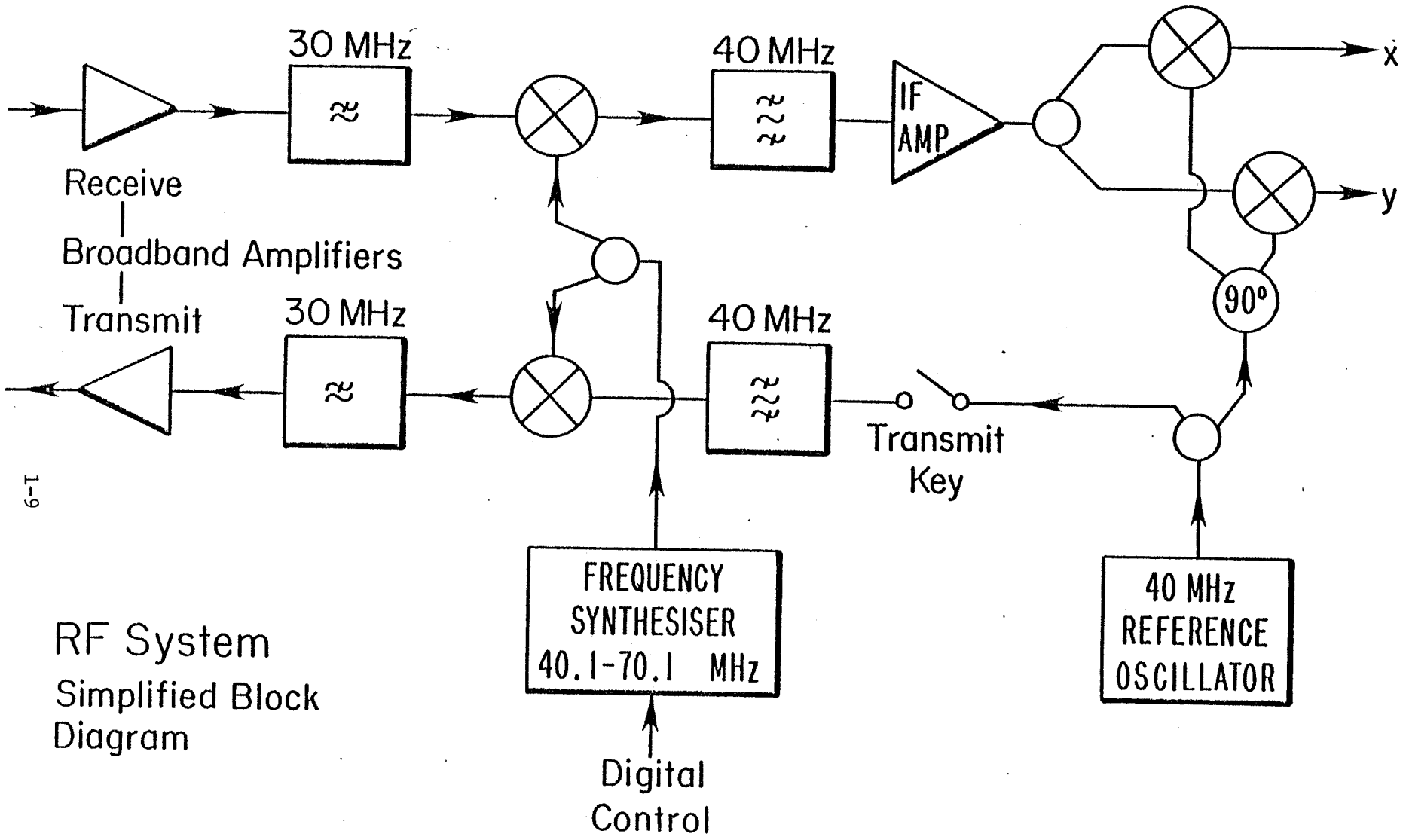
Front End Processor
Simplified Block Diagram

FIGURE 2

in the processing. Data from a single receiver channel can be passed to the output directly for system test or for special operating modes. Microcode assembler program has been developed which is resident in the Interdata.

Figure 3 shows the basic arrangement of the RF system used for the generation of the transmitted signals and the coherent reception of echoes. A symmetrical up- and down-conversion scheme is employed with two oscillators. The first oscillator, a general purpose synthesizer, generates a frequency between 40.1 and 70 MHz and up-converts the receive band of 0.1-30 MHz to a 40 MHz IF. The second oscillator, a fixed-frequency 40 MHz crystal oscillator, is down-converted by the same synthesizer output to form the transmitted frequency. Keying and filtering of the transmitted signal is performed at the fixed 40 MHz frequency. The 40 MHz oscillator then provides the reference for coherent quadrature detection of the received signals. The frequency of operation is selected by the Interdata computer which controls the synthesizer. If operation from an external standard is required both oscillators must be locked.

An important feature of the system is the choice of output signal representation. Most previous ionospheric sounding systems have used logarithmicly compressed amplitude representation with zero crossing phase or logarithmic quadrature components. The use of a logarithmic scale is inconvenient for many kinds of digital signal processing. For instance, if a Fourier transform of the received signal is desired, it has been necessary to exponentiate the logarithmic function, which is likely to be inaccurate if the function was generated by analog means in the first place. The justification for this choice of signal representation has been that it is otherwise difficult or impossible to cover the dynamic range of the received signals in any other manner. However, recent developments in solid state technology have made available stable, wide-band linear amplifiers with extremely wide dynamic ranges, typically > 140 dB in a 30 kHz noise bandwidth. By combining these with passive filters and a well-designed mixer and quadrature component detector, it is possible to build a linear receiver that is basically limited only by the choice of digital quantization and the DC stability of the detector. We have chosen this route. By using 12-bit 2's complement binary encoding of the quadrature components, we have < 60 dB dynamic range between quantization noise and saturation giving a 30-40 dB operating range allowing for reasonable numerical accuracy at the lower end and some margin against overload at the upper end. The position of this range is adjusted to prevailing signal levels between pulses by means of stepped attenuators which are under the control of the Interdata computer. DC offsets are removed by an autocalibration program. Provision has also been made for range dependent gain switching should it be required.



RF System
Simplified Block Diagram

FIGURE 3

A more detailed block diagram of the RF system is shown in Figure 4. The bandwidth of the system is similar to that of previous ionosphere pulse sounders. Maximally flat time delay crystal filters are used, two in each channel of the receiver and one following the transmitter keying circuit. Each filter has a 4-pole response and a 3 dB BW of 30 kHz. This gives an overall 3 dB bandwidth of 22 kHz in the receiver and a matched response to a 60 μs transmitted pulse. The impulse response is Gaussian in form. Provision is made for phase reversal switching in the receiver input multiplexer and for quadrature phase modulation in the transmitted pulse. The sampling rate of the ADC's in the Front End Processor has been chosen to be 100 kHz giving a folding frequency of 50 kHz. At this frequency offset, the receiver IF gain is 56 dB down from the response at the center frequency. The input memory for each receiver channel holds 512 XY pairs corresponding to a total acquired virtual height range of ≃ 776 km.

Great care has been taken to preserve a high degree of linearity at the input of the receiver to reduce intermodulation of received signals and minimize the need for preselection filters. A high level mixer is used, driven by a fast square wave with 1 nanosecond rise and fall time transitions to provide highly linear switching. The 1 dB desensitization point at the main receiver input (excluding the antenna preamplifier) is +15 dBm and the third order intercept +26 dBm with 0 dB RF attenuation. This performance is limited, particularly at low frequencies, by the diode switches in the antenna multiplexer. The receiver gain varies less than $\pm$ 2 dB from 0.2-29 MHz and the tangential sensitivity is < 1 μV. Operating experience indicates that preselection filters are not required for operation in typical site conditions.

The low level transmitter drive output is amplified first by a solid state class A amplifier to the 200 W level. This can be used directly or can be used to drive a pulsed class A wide band vacuum tube amplifier with a 10 kW output. The transmitter outputs are nominally 50 Ω unbalanced. Wide band unbalance-to-balance transformers are used to drive typical sounding antennas.

A feature of the system is the provision for generating a low level replica of the transmitter pulse. This can be inserted at an arbitrary range under control of the Timing Sequence Generator and is coupled to the receiving antennas to serve as an overall calibration of the group and phase delays of the receiver channels and a means of self checking the entire system without making unnecessary transmissions.

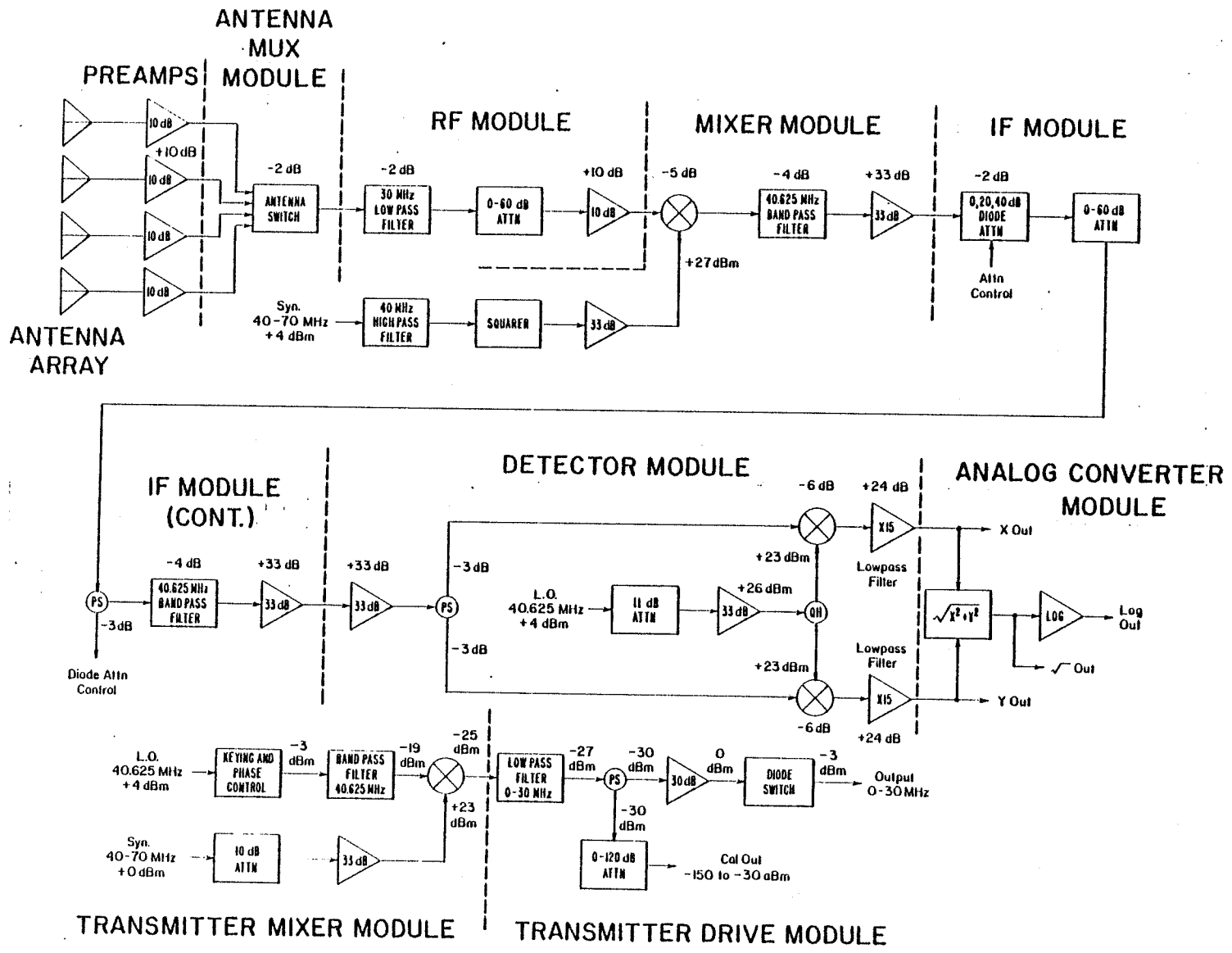

ANTENNA MUX MODULE
PREAMPS
RF MODULE
MIXER MODULE
IF MODULE
10 dB
+10 dB
-2 dB
ANTENNA SWITCH
30 MHz LOW PASS FILTER
0-60 dB ATTN
+10 dB
-5 dB
-4 dB
+33 dB
40.625 MHz BAND PASS FILTER
33 dB
0,20,40 dB DIODE ATTN
Attn Control
0-60 dB ATTN
+27 dBm
Syn. 40-70 MHz +4 dBm
40 MHz HIGH PASS FILTER
SQUARER
ANTENNA ARRAY
IF MODULE (CONT.)
DETECTOR MODULE
ANALOG CONVERTER MODULE
PS
-3 dB
Diode Attn Control
-4 dB
40.625 MHz BAND PASS FILTER
+33 dB
+23 dBm
+26 dBm
L.O. 40.625 MHz +4 dBm
11 dB ATTN
QH
-6 dB
+24 dB
X15
Lowpass Filter
X Out
Y Out
LOG
Log Out
√ Out
L.O. 40.625 MHz +4 dBm
KEYING AND PHASE CONTROL
BAND PASS FILTER 40.625 MHz
LOW PASS FILTER 0-30 MHz
DIODE SWITCH
Output 0-30 MHz
Syn. 40-70 MHz +0 dBm
10 dB ATTN
0-120 dB ATTN
Cal Out -150 to -30 dBm
TRANSMITTER MIXER MODULE
TRANSMITTER DRIVE MODULE

FIGURE 4

An auxiliary component of the system is the housekeeping ADC. This is a multiplexed Analog-to-Digital Converter with 64 inputs. It is controlled by the Interdata through the digital I/O bus. The output is a 12-bits binary number representing a $\pm$ 10 V input range. This unit is to provide general supervisory voltage, current, and temperature monitoring which is recorded along with the data from the sounder. It is also connected to the analog outputs of the receiver and can be used to provide data in the spectrum surveillance mode and also for AGC feedback when the system is used as a general purpose receiver. Additionally, the ADC may be used with additional programming to acquire data from other sensors such as riometers or magnetometers.

Revised 3/11/80

2. THE INTERDATA COMPUTER SYSTEM

2.1 General

This section on the Interdata computer system is not intended to be exhaustive or sufficient for maintenance purposes. The Interdata manuals for the appropriate machine should be consulted for details of the system and schematics, etc. The following general description of the hardware and the configuration used in the HF Radar and its mode of operation will provide the framework for understanding the interfaces with the rest of the system and its operation.

2.2 CPU

The HF Radar uses either the 7/16 CPU with the High Speed Arithmetic and Logic (HSALU) option or the 8/16E CPU with hardware multiply/divide. Both systems have single and double precision floating point hardware. In general, the 8/16 system is slightly faster and is also capable of addressing up to 256 Kb of memory as opposed to 64 Kb for the 7/16.

2.3 I/O

Both the 7/16 and 8/16 have identical I/O bus arrangements except for the differences required by the 8/16 extended memory space in the arrangements for Direct Memory Access.

Each chassis slot used for I/O interface has access to the multiplexor bus. This is a general purpose bus used for all program controlled I/O operations. The chassis is arranged so that either two half boards or one full board can be inserted in each slot. The two connectors on the left and right sides (viewed from the front) are numbered 1 and 0, respectively. The multiplexor bus is available separately on both connectors. The interrupt priority, which is set by the wiring of the RACKO, TACKO (Receive/Transmit Interrupt Acknowledge) daisy chain is generally from top to bottom in the left-hand connector and then from top to bottom in the right-hand connector. Full width cards use the higher priority left-hand connector. Memory Address and Data lines are shared between both connectors. Figures 5 and 6 show the assignment of boards in the chassis for the 7/16 and 8/16 systems, respectively.

2.3.1 The Multiplexor Bus

The multiplexor bus is a bidirectional 16-bit general purpose bus which is used for communication between the CPU and I/O devices under program control. Interdata numbers the bits 0 through 15. 0 is the MSB. The function of the bus is controlled by 5 strobe lines. Note that Interdata mnemonics are terminated by a 1 or 0 indicating whether the line so labeled is active low (0) or high (1). The data bus lines are active low. The function of the lines is as follows.

FIGURE 5

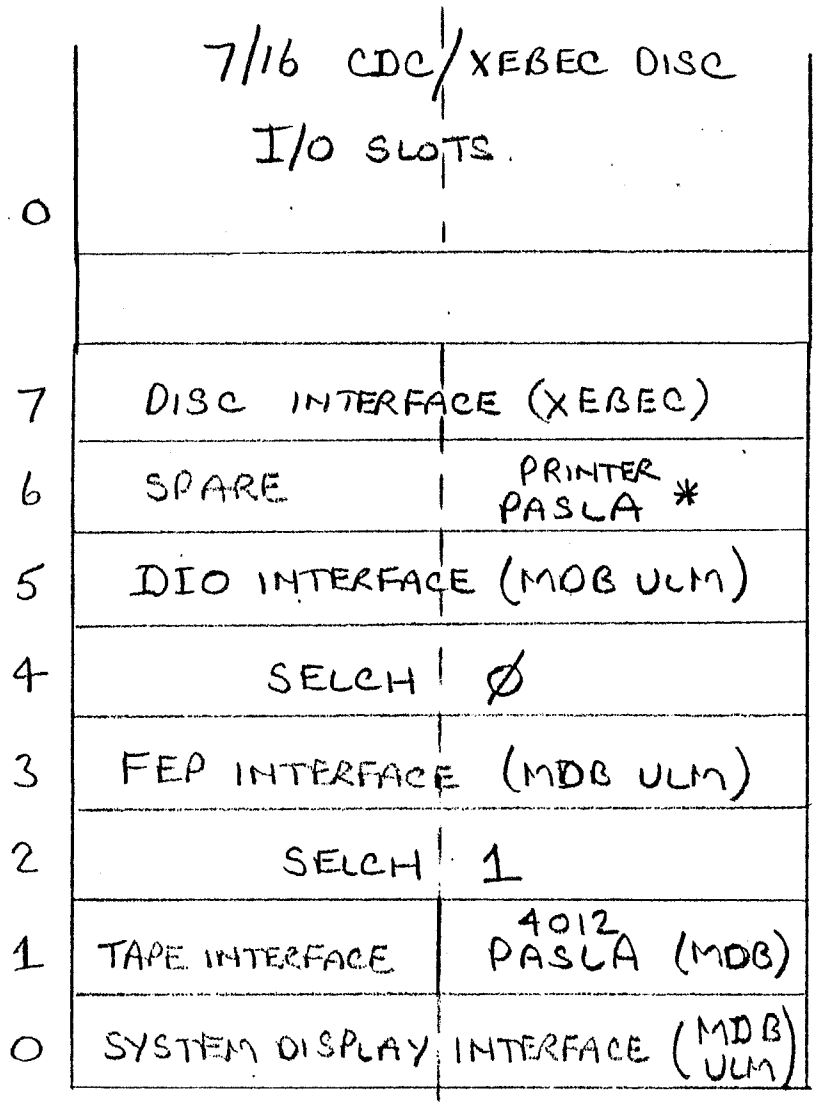
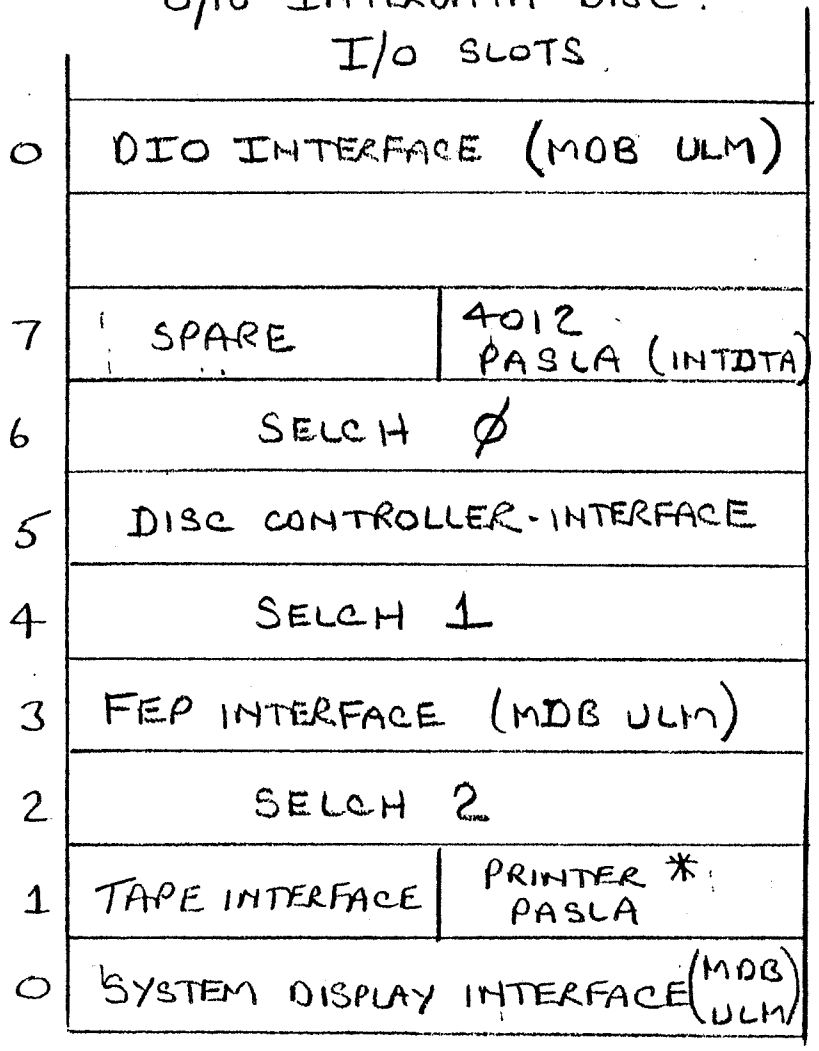


FIGURE 6



* IF REQUIRED.

ADRSO (address control line) indicates that bits 8 through 15 on the bus are to be interpreted as an I/O device address. An addressed device is required to latch its selection for further use. Addresses are hardwired on the cards and are not affected by slot position. An addressed device returns a control line HWO (Half Word Control) which indicates if data transfer operations are on a half word (16-bit) or byte (8-bit) basis. Byte transfers use bits Ø8 through 15.

SRO (Status request control line) places the device status byte in bits 8 through 15 on the bus from the previously addressed device. Note that status bits 12-15 are predefined in meaning and are automatically transferred to the program status word where they may affect the execution of the program. The meanings are:

Bit 12	Device busy.	High true
Bit 13	Examine status or time out.	
Bit 14	End of medium.	
Bit 15	Device unavailable.	

Bits 8-11 are available for newly defined functions and will be device peculiar.

DRO (Data Request). The CPU reads either 16 or 8 bits from the device addressed.

DAO (Data Available) indicates that either 16 or 8 bits of data are present on the bus for the device to read. This control strobe is normally used to latch the data into a register in the I/O device.

CMDO (Command) indicates that bits Ø8-15 on the bus are to be interpreted as command functions. These will normally be latched by the device.

Programming manuals should be consulted for information on the instruction formats required to operate the multiplexor bus.

2.3.2 Direct Memory Access I/O

Two types of provision for Direct Memory Access (DMA) are possible in the Interdata hardware system. Priority in access is set by the wiring of the ACTO/TACO daisy chain and is normally from top to bottom of the card slots.

The first type of provision is that of the dedicated DMA controller which is associated only with one device. The only example of this type in the system is the integral DMA controller for the CDC disc contained on the Xebec disc interface card used in the 7/16 systems.

The second type of provision is the use of an Interdata selector channel (SELCH). This full width card, which can only be installed in even numbered slots and requires back plane wiring changes to interrupt the multiplexor bus physically on the connector 1 side of the chassis. The bus below the SELCH up until a second SELCH is reached becomes a so-called "private bus." Devices using connector 0 are unaffected. At the second SELCH, the multiplexer bus is reestablished from the 0 connector side and a second private bus established below it, etc.

In the resting state, each SELCH connects its private bus to the multiplexor bus so that programmed I/O can take place with all the devices connected to that bus. For a DMA data transfer to take place, the I/O device must first be addressed and any necessary initialization accomplished. The appropriate SELCH is then addressed and the memory starting and finishing addresses loaded. A GO command is then issued to the SELCH which then commences the data transfer to or from memory on a cycle stealing basis with the last device addressed on its bus. Data transfer is regulated by the busy/done status bit and is terminated by any one of status bits 13, 14, or 15 or when the final address is reached. At the termination of the data transfer, the SELCH interrupts the processor which is then able to read the actual final address.

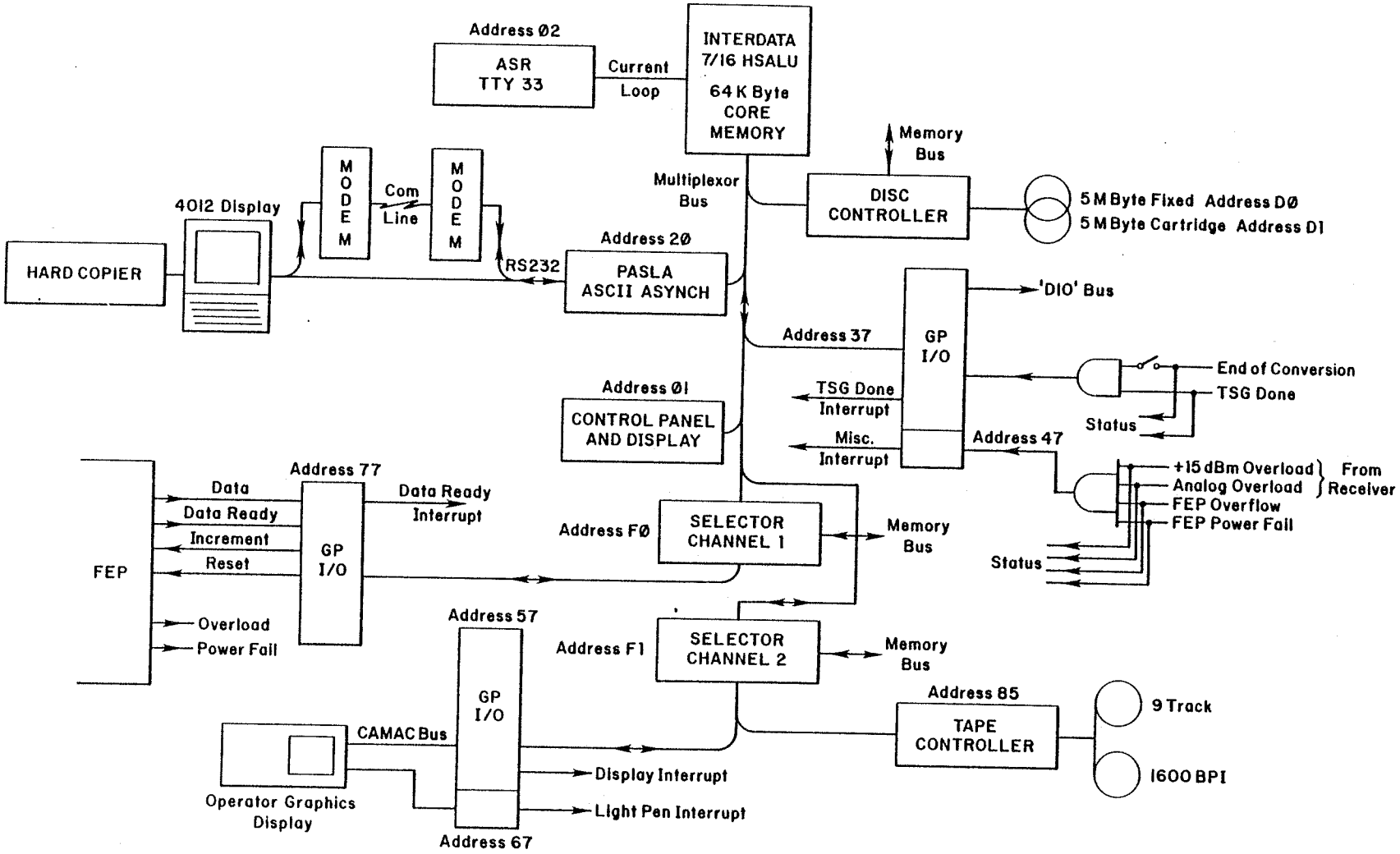
Note that during a DMA operation by the SELCH on its private bus, there is no multiplexor bus access or simultaneous DMA data transfer to other devices on the same private bus.

For more information on the hardware or software associated with DMA operations, refer to the appropriate Interdata manuals.

2.4 Overall Computer System Arrangement

Figure 7 shows the overall arrangement of the peripherals connected to the Interdata computer. Note that this shows the 7/16 system in which the Disc Controller has its own DMA controller. In the 8/16 system, a third SELCH is positioned above the Disc Controller card. The DMA priorities are, first, the 10 Mb disc; second, the Front End Processor (FEP) interface EKO, and third, the Tape Controller and System Display. The philosophy assumed here is that the disc will always be the data repository during sounder operation and that transfer to tape will be programmed to occur when the rest of the system is idling or carrying out data processing.

Interfaces between the multiplexor bus and the Digital Input/Output (DIO) bus, the FEP, and the System Display are implemented using general purpose interface boards (GPIO) manufactured by MDB Systems. These contain the standard logic necessary to interface with the multiplexor bus and have space for wire wrapped logic necessary for the particular application. These will be described in Section 3.



NSF/NOAA HF RADAR
GENERAL COMPUTER I/O

Figure 7

Figure 7 also shows the source of interrupts and the more important status lines. Each GPIO board has one or two device controllers each containing the necessary logic for one interrupt line and one independent status word. The Interdata multiplexor bus addresses for each device are also shown.

3. SPECIAL PURPOSE INTERFACES TO THE INTERDATA

3.1 General

There are three special purpose interfaces to the Interdata multiplexor bus which are implemented using GPIO cards manufactured by MDB Systems, Inc. MDB refers to these as Universal Logic Modules. The MDB manual on the printed circuit portion of the board is included in this manual as Appendix 1. This must be understood in order to follow the descriptions of the 3 special interfaces constructed with these boards which follow.

3.1.1 The DIO System and Interface

3.1.1.1 General

The Digital Input/Output (DIO) bus is an extension of the multiplexor bus to enable a large number of relatively slow control and status monitoring operations to be multiplexed through one interface to the Interdata. The bus structure was chosen so that the simplest possible interface using a minimum package count could be incorporated directly into the device requiring control or status readout. The general arrangement of the DIO bus itself is shown in Figure 8. 25 lines are used with ribbon cable and connectors. 8 lines are used to send data from the Interdata and 8 lines to receive from the device. 6 lines are used to specify a device address 1-63. Address 0 is excluded from use as this is the address initialized on turn-on. The remaining 3 lines carry an address strobe, a data write strobe, and ground.

The operation of the bus is as follows. No handshaking is used. To send data to a device, the Interdata places the DIO address in the least significant 6 bits of the least significant byte and the data in the most significant byte of a 16-bit register. The contents of this register is then sent on the multiplexor bus to the DIO interface card where it is latched into an output register. This automatically starts a sequence of strobe pulses which first latches the appropriate address decoder on the DIO bus, latches the data word into a register in the addressed DIO device and latches the data or status byte placed on the DIO bus by the device into an input data register on the DIO interface card. The latter can then be read by the Interdata using an appropriate multiplexor bus instruction. If a read only operation is desired, a command is used to change operation of the DIO interface so that the write strobe is suppressed. This enables status to be read without disturbing the contents of the device data register. In many DIO devices, the contents of the data register are reflected in the status byte to permit verification if desired. Appendix 2 contains a directory of DIO devices and the control and status assignments.

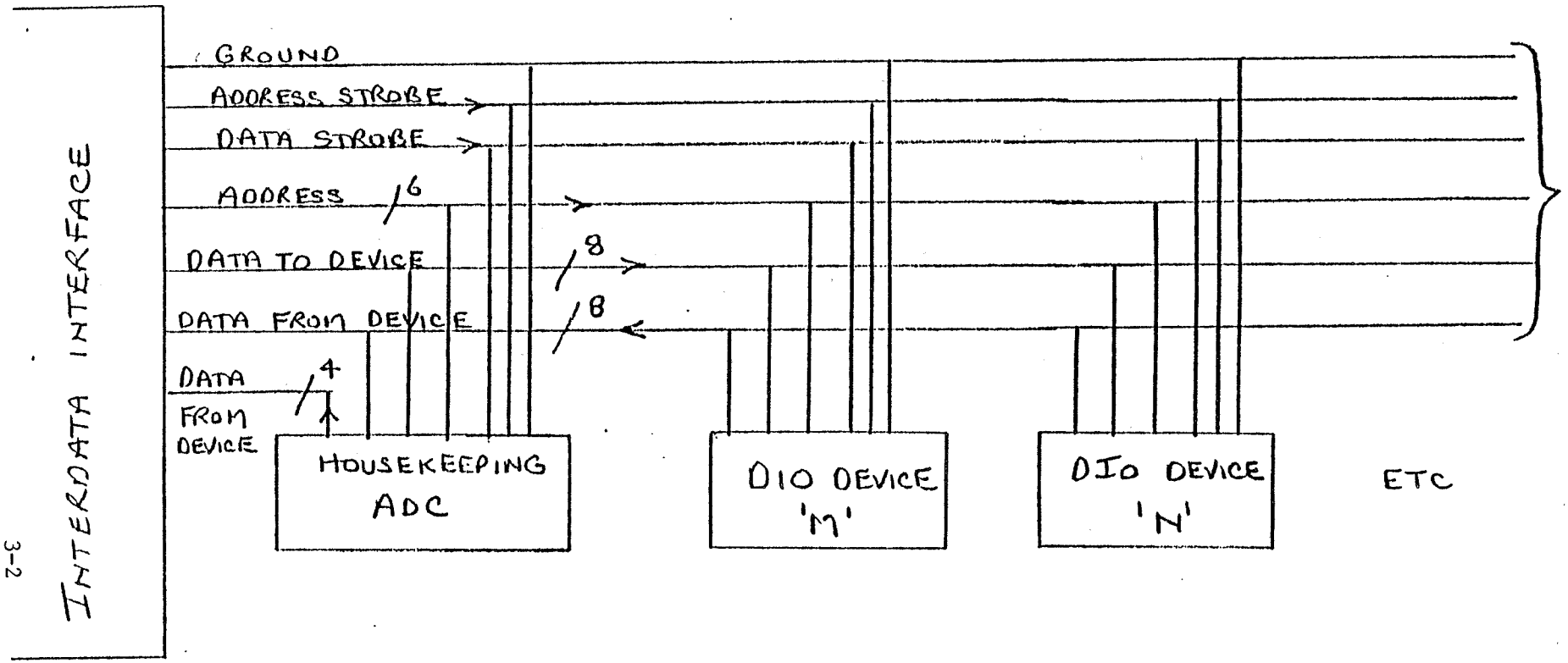


FIGURE 8. GENERAL ARRANGEMENT OF THE DIO BUS.

One DIO device which is slightly different to all others is the Housekeeping ADC. This is specially wired to the interface card to permit the return of a 12-bit data word from the ADC.

3.1.2 The DIO Interface Card

This is built on a MDB ULM GPIO card with the second controller and I/O register 2 options incorporated. The schematic of the added logic in the wire wrapped section is shown in drawing HFS006.

Figure 9 shows the timing diagram. The MDB gated data available strobe DAG10 (pin X 111) starts a timing sequence whenever new data are placed by the Interdata in Output Data Register 2. The DIO bus lines carrying data from the interface come from this latter register, and the bus lines to the interface go to Input Data Register 2. P3 carries the normal 25-pin DIO bus. P2 carries the expanded DIO bus with 12 input lines for the HSK ADC output.

Immediately following the gated strobe DAG10 OS1 generates a 0.5 μs delay to allow the DIO lines to settle. A 1 μs address strobe is then generated by OS2. There is then a further 0.5 μs delay followed by a ≃ 1.7 μs data strobe. The data strobe low causes the previously addressed device to enter the data from the interface output register into its input register and also causes the device to put its output data on the lines to the interface input register. On the rising back edge of the data strobe the data transfer is latched in both the device input register and interface input register. It is necessary in programming to ensure that new data are not placed in the interface output register until this ≃ 4 μs cycle is complete. The data strobe can be inhibited by bit 15 of the command register in the ULM being set low. The state of this line can be read as status bit 10. When inhibited, the DIO only reads from a device but does not change the contents of its input register. At power up, the system reset pulse SCLR10 resets the interface output register to 0.

The DIO bus is driven by open collector buffers with resistive pull-up. This causes the back (rising) edge of the strobe pulses to be slow. This minimizes noise coupled from the strobe at the instant of data or address latching. Some device registers are connected directly to RF filters which slow the response of the register output. The increased length of the data strobe (1.7 μs) allows for this increased settling time so that the register can latch correctly.

The DIO bus signals generated by the interface are suitable only for distribution over short distances within the system racks because they are unbalanced and subject to ground loop noise. Hardware has been designed to allow the extension of the DIO to medium or long distances from the system racks.

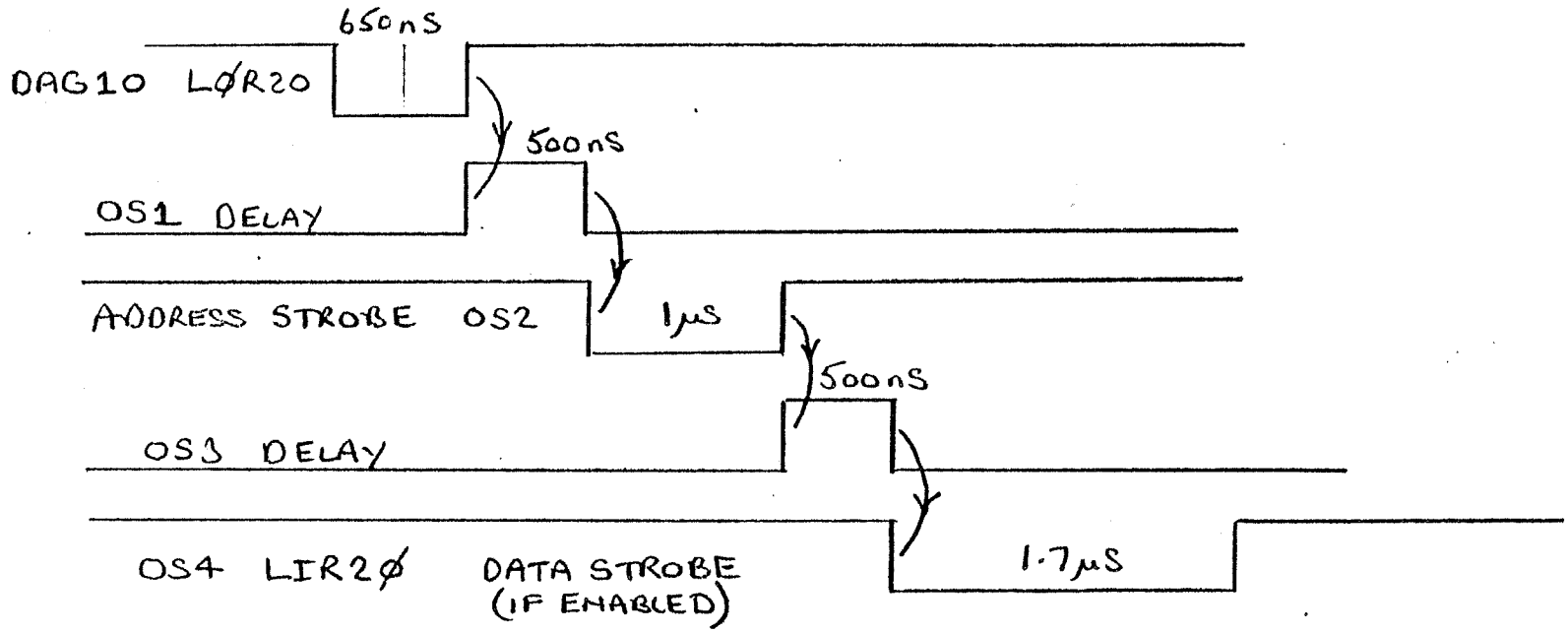


FIGURE 9. DIO STROBE TIMING.

3.1.3 DIO Receivers

A typical DIO bus receiver incorporated in various devices in the system is shown in drawing HFS134. The strobe signals are filtered by low pass filters R_1C_7 and R_2C_8 with ≃ 100 ns time constants before being reformed by the high impedance input hysteresis gates U1. A power-up reset is applied by means of R_3C_9 to ensure that the address comparator latch is reset to the not true state. The device address is set by wire links at the comparator input. When the comparator sees its address on the bus, its latch is set by the strobe taking pin 9 TRUE. This turns on the output tristate buffer which places the status output of the device on the bus and enables the receiving buffer. The following data strobe, if received, turns on the tristate receiving buffer and writes the data into the tristate latch which maintains the data out from the receiver after the data strobe is completed. Unused status inputs of the receiver are normally strapped to the receiver outputs to permit computer verification of receiver operation.

3.1.4 DIO Programming

The DIO is interfaced through an MDB ULM 16-bit I/O card. The Device Address of the ULM is 37_{16}. Each system connected to the DIO has in addition, a DIO 6-bit address. These addresses are listed in the DIO directory (Appendix 2).

Each device connected to the DIO can receive and latch an 8-bit control byte and transmit an 8-bit status byte (12 bits in the case of the ADC output). Depending on the command given to the ULM, a DIO operation may be a read only or a read and write control byte. To the Interdata, all DIO operations appear as data inputs and outputs. The following should make this clear.

To read status from a DIO address:

1. Output command byte to the ULM to set DIO read only state

   OC
OCR } 0037_{16}, $XXXXXXX0_2$

   Note, this is a byte transfer command, and the address in memory of a byte must be specified. This command is latched in the ULM and need not be repeated for a series of reads. The state of this command is echoed in bit 10 of the status word from device 37.

   X = bits that do not affect this operation. In this case, the 2 MSB of the command byte control interrupt status.

2. Address the DIO device:

WD, WDR } 0037_{16}, $XXABCDEF_2$

ABCDEF is the binary DIO 6-bit address. This is latched in the ULM DIO controller.

3. Read the status of or data from the DIO address.

For 8 bits:

RD, RDR } 0037_{16}, $A(X_2)$ / R_2

The contents of R_2 or AX_2 is now the 8 bits returned from the last DIO address outputted.

12 bits:

RH, RHR } 0037_{16}, $A(X_2)$ / R_2

The contents of $A(X_2)$ or R_2 will now be a 16-bit word containing the 12-bit 2's complement number from the ADC, right justified with the sign bit extended.

To read and write to a DIO address.

1. Output command byte to the ULM to set the read/write state:

OC, OCR } 0037_{16}, $XXXXXXX1_2$

(Note, this command is latched and need not be repeated for a series of read write operations.)

2. Address the DIO device and output to the DIO device.

WH, WHR } 0037_{16}, $LMNOPQRSXXABCDEF_2$

A-F is the 6-bit DIO address.
L-S is the desired output byte.

3. Read from the DIO device:

As 3 above.

In very many cases where the DIO device is basically a controller (for instance for an attenuator), the data returned on read are merely the state of the active bits in the output latch plus, in some cases, a status bit showing if a manual override has been invoked. The read function can be used to collect overall status and to check on the correct receipt of a write operation.

3.2 The Front End Processor (FEP) Interface

The wire wrapped logic section of the FEP interface is shown in drawing HFS008. The interface is built on a MDB ULM card with no options implemented. The device address is 77_{16}.

16 data lines are received from the FEP. A control line, Data Ready, which is active high indicates to the interface that the FEP has a block of data ready to transfer to the Interdata. Two control lines go from the interface to the FEP. Firstly, an address counter increment (INC) which enables the interface to step through the FEP output memory and secondly, a RESET line which resets the data ready flag and indicates to the FEP that the data transfer is complete.

Figure 10 shows the timing of the various operations associated with the data transfer. Initially, the 16-bit presettable counter formed by J5, J15, and J14 is reset as is the EOM status bit 14 control flip-flop K15. Thus EOM is high indicating that there are no data to transfer. This also holds the "busy/done" status bit 12 high (busy) via gate L13B. Status bit 15 indicates whether the FEP 5 V power is present via F9A. A general reset to the interface having the same effect as the Interdata system clear can be applied by command bit 11 via F9B and F9C. The command bit should normally be high and is taken low for reset.

When the FEP has completed a processing cycle, it exchanges control of its output memories so that the data to be transferred comes under the control of the output address counter. This counter will have been previously reset to zero. The data block to be transferred must start at zero and the contents of location zero must be the block count (maximum 1023).

The FEP now signals its readiness for a data transfer by taking its data ready (P2, 3) high. This signal is filtered and reformed on the interface board by a 100 ns time constant and hysteresis gates 11M. The state of this reformed signal is made available to the Interdata as status bit 11 (active high). The edge initiates an interrupt from device 77_{16} via L13A. The edge also triggers OS1 which produces a 0.5 µs pulse. This presets the counter J5, 15, 14 with the 1's complement of contents of word zero in the data block. On the back edge of the OS1 pulse, OS5 is triggered which sets the EOM control flip-flop indicating that the interface is now ready to transfer data. The busy/done status bit is now released.

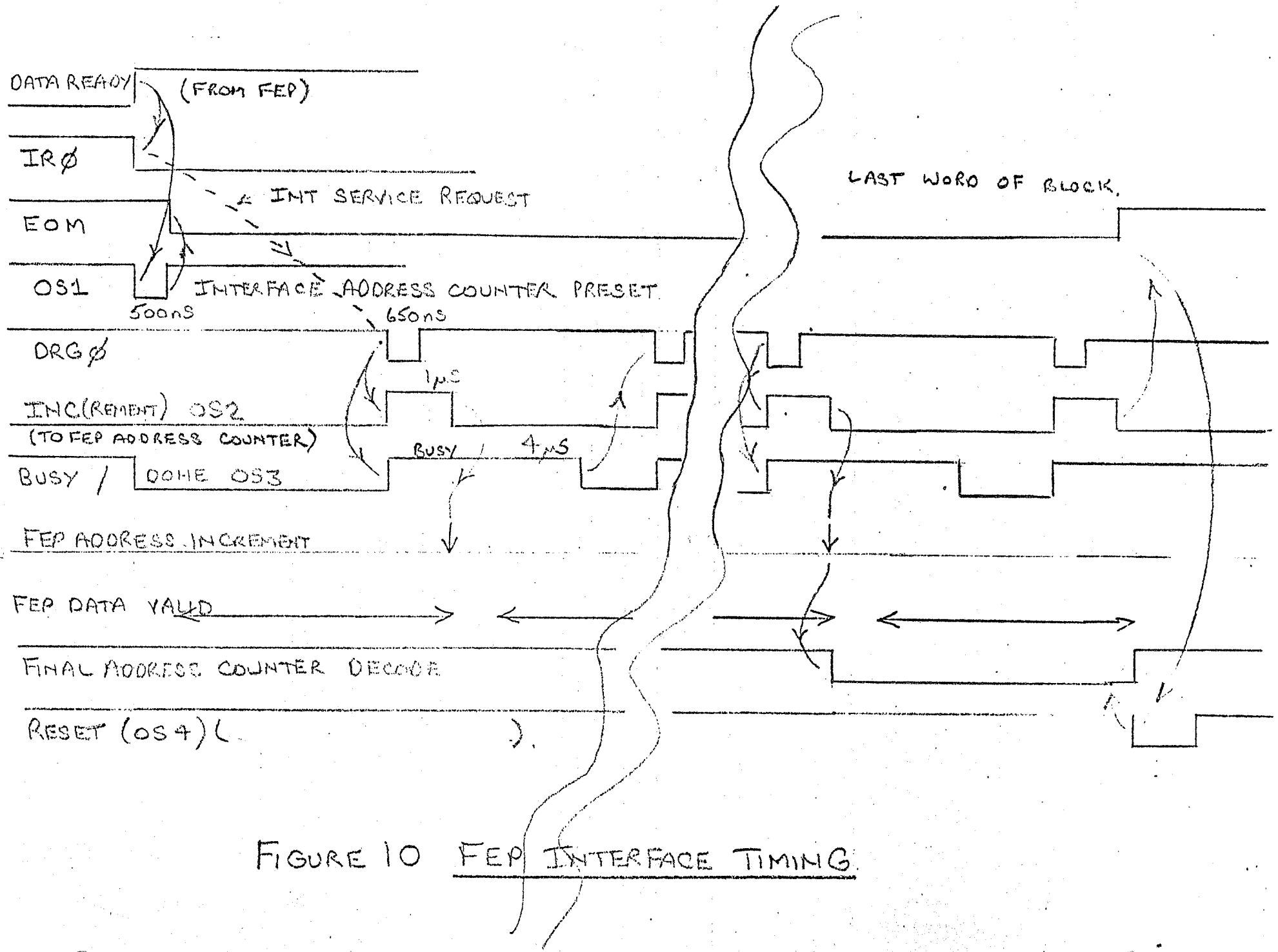


FIGURE 10 FEP INTERFACE TIMING

In normal operation, the Interdata system responds to the interrupt by giving the SELCH a GO signal having previously loaded the buffer memory addresses. For test purposes, transfers may be made under program control either using interrupt initiation or by inspection of the data ready status bit. In either case, the first data word is transferred by the gated data read pulse DRG10. This enables gates F5, 7, 14, and 15 to place the data from the FEP memory on to the multiplexer bus (or SELCH private bus if this is enabled). The front edge of DRG10 fires OS2 and OS3. OS2 generates a 1 μs pulse which is sent as an increment (INC) control signal to the FEP. The address counter in the FEP increments on the back edge of the OS2 pulse. This pulse also increments the block counter J5, 15, 14. OS3 generates a 4 μs pulse which takes the busy/done status bit 12 to busy. The length of this pulse is chosen to prevent the FEP interface monopolizing the Interdata memory bus. When the busy signal times out, the Interdata (or SELCH) responds with a new DRG10 pulse which reads the second word of the data block, and the transfer proceeds in this way at a maximum rate of about 200 kHz until terminated. Termination will normally occur when the block counter J5, 15, 14 reaches all 1's which is decoded by K14 and K13. This takes the data input to the EOM control flip-flop K15 low. The rising edge of the next DRG10 pulse via OS2 clocks the flip-flop taking EOM high and terminating the sequence. One more word than the block count is thus transferred. The flip-flop transition triggers OS4 which resets the block counter J5, 15, 14 and sends a reset to the FEP address counter which also clears the FEP data ready flag. In the case of a SELCH transfer, the data transfer can also be terminated first by the SELCH if the memory buffer length allocated is shorter than the FEP block length. If this occurs, then it is necessary to command an interface reset to permit the next cycle to proceed correctly.

3.3 The System Display Interface

This interface is built on an MDB ULM GPIO board. Input and output register 2 options are incorporated. As the functioning of this interface is an integral part of system display operation refer to the System Display Manual for details of this interface.

4. INTERRUPT STATUS READOUT, AND COMMAND STRUCTURE

The MDB ULM GPIO boards each have one set of interrupt logic and space for a second set of logic to provide both an interrupt and status word input from an independent device address. These capabilities are used to provide for interrupts and status indications from external devices which are not necessarily directly connected with the main function of the ULM board as a data interface. The following section summarizes the sources and meaning of the various signals. The existence of a hardware interrupt or status line does not necessarily mean that existing software makes any use of the information.

4.1 Interrupt and Status

Interrupts are generated from 9 sources. These are grouped to appear from 5 different Interdata device addresses. Distinction between sources in a group is achieved by reading the status word associated with the device address returned by the interrupt service routine. The interrupt sources are:

Group 1: Device Address 37 (DIO I/O Board). Status bits 8, 9, 12-15 are tied low.

a. End of Conversion (EOC INT). Generated by the housekeeping ADC when a requested conversion is complete. Output data are available via the DIO. Status bit 10 goes to zero if this is the source of the interrupt. The status indication remains at zero until a new conversion cycle is initiated. This source can be disabled with a switch on the DIO Interface board.

b. Timing Sequence Generator complete (TSG INT). Generated by the TSG when the current sequence of operations is complete. Status bit 11 goes to zero if this is the source of the interrupt. The TSG will reset the status line when commanded to commence a new sequence.

Group 2. Device Address 47 (DIO I/O Board). Status bits 12-15 are tied low.

a. +15 dBm Overload. This indicates a gross receiver overload which causes the crystal filter damage level to be exceeded. The receiver protection circuit latches and introduces a large value of IF attenuation by turning off all current to the diode IF attenuator. The latch is reset, if the overload has been removed, by the TSG applying the system reset. Status bit 11 goes to zero if this is the source of the interrupt and returns to 1 when the latch is reset.

b. Analog Overload. This indicates an output from the analog $\sqrt{X^2 + Y^2}$ converter of greater than the full scale ADC range of 10 V. A 100 μs analog time constant filters the input to the threshold circuit to prevent it responding to isolated noise impulses. Status bit 10 goes to zero for the duration of the overload. This is the only nonlatched bit in this group, so the absence of a corresponding status indication to this interrupt must indicate a transient analog overload condition.

c. Front End Processor (FEP) Overflow. This indicates that a numerical overflow has occurred in the FEP. Status bit 9 goes to 0. Reset occurs when a new start instruction is given to the FEP.

d. FEP Power Failure. This indicates that a power failure has occurred in the FEP of such a magnitude that data may have been lost from the volatile memories. Status bit 8 goes to zero. A "permanent" zero indicates continuing power failure. Reset occurs when a new program load is given to the FEP.

Group 3. Device Address 57 (System Display Interface Board)

a. System Display. Indicates that the current display instruction has been completed. It is not normally responded to by the program as this device normally operates in the DMA mode via the selector channel. Status returned is the standard busy/done on bit 12 which is used to control data flow from the Selch. Status bit 11 goes low when the light pen flip-flop is set. All other Status bits are strapped low.

Group 4. Device Address 67 (System Display Interface Board)

a. System Display Light Pen. Indicates that the light pen flip-flop has been set and the XY address stored to be read through address 57. Status bit 11 goes low. All other Status bits are strapped low.

Group 5. Device Address 77 (FEP Data Interface Board)

a. FEP data ready. This indicates that a data file is available for transfer from the FEP output memory to the Interdata. Status bit 11 goes high when the data are available and is reset at the completion of data transfer. Data transfer is regulated by the standard busy/done on Status bit 12. The completion of a data file transfer is indicated by Status bits 15, 14, and 12 going high (DU, EOM, EX).

b. Auto Bootstrap Sense Switch. Status bits 10, 9, and 8 are used to sense the position of S_2 and S_3 on the bootstrap loader control panel. S_3 controls bit 10. Low = DSC2; high = DSC 1. Bits 8 and 9 are used as a 2-bit word for file select. Ø = file 1; 1 = file 2, 2 = file 3, 3 = file 4.

4.2 Commands

Commands are latched on the MDB Interface boards. The following are used for specialized functions.

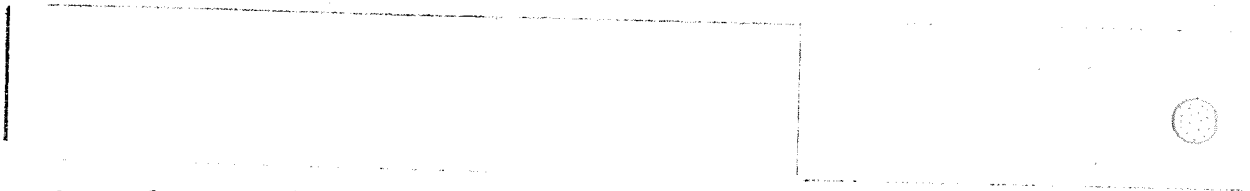
Group 1: Device Address 37 (DIO I/O Board) CMD 151. When low sets DIO read only condition. When high sets read and write. Condition indicated by status bit 10.

Group 2: Device Address 47--no commands.

Group 3/4: Device Address 57/67 Display Interface board--no commands.

Group 5: Device Address 77 FEP Data Interface Board

CMD 111. When low, this inializes all interface flip-flops. If a data transfer is not fully completed, ths reset should be commanded before starting another cycle. SCLR 10 also performs this function.



General: CMD 101 is not used for SEL0 as shown in the MDB command register drawing. SEL0 is strapped for half word operation on all boards. CMD 08 and 09 have the standard Interdata interrupt arm and enable function on all interface boards.

5. SYSTEM TIMING AND SEQUENCING

5.1 Timing

The Timing Sequence Generator (TSG) provides control lines to various parts of the RF and data processing system which provide the sequencing necessary to switch from receive to transmit, define the transmitter pulse length and modulation, revert to receive, acquire digital data from the receiver at the desired ranges and initiate the data processing cycle.

For details of the way the TSG timing lines are generated and the detailed function of the timing control inputs to various parts of the system, the appropriate technical manuals should be consulted. The intent of this section is to give a system level overview.

The basic system clock in normal operation is the 10 MHz oscillator in the AILTECH synthesizer. This is an ovened oscillator with a stability of 5 parts in 10^9 per day after 72 hours operation. This is used for the clock of the microprocessor in the TSG and to generate the 100 kHz clocks used for data conversion and therefore range determination. In the absence of line power to the TSG, a low power 100 kHz oscillator maintains the time of day clock which is kept running on lead acid gel batteries.

There are three groups of output lines from the TSG. The first, called the RF state vector is intended for critical timing operations which must be coherent with the system clock and which take place during the transmitting and data acquisition cycle. These are the lines which are directly controlled by the TSG "scenario" look up tables. These lines are reclocked by D flip-flops at the TSG microprocessor output ports to ensure absolute coherence with the 100 kHz system clock. The second group, called the FEP state vector, are used for noncritical timing operations which are carried out either before the start of a scenario sequence or after it is completed. The allocations of these groups is shown below.

RF Output State Vector

(TSG Processor Address 46ØØ)

LSB	Bit 0	Transmit Enable 1
	Bit 1	Transmitter keying
	Bit 2	Transmitter phase code $Ø_1$
	Bit 3	Transmitter phase code $Ø_2$
	Bit 4	FEP input memory write enable
	Bit 5	Receiver Fast Attenuator Control FA1
	Bit 6	Receiver Fast Attenuator Control FA2
	Bit 7	Transmit Enable 2

FEP Vector

(TSG Microprocessor Address 6EØØ)

Bit 0 FEP input memory select
Bit 1 FEP input memory address counter reset
Bit 2 Spare
Bit 3 Receiver phase code $\emptyset_3$
Bit 4 FEP start
Bit 5 Spare
Bit 6 Sample interval (10 μs/20 μ s)*
Bit 7 FEP Busy/Done flag (This is an input to the TSG.)

*This line controls logic on the TSG board which can pulse the FEP write enable line to cause every other sample to be taken.

The third group of outputs is the FEP command byte usually used as the starting address.

Figure 11 shows a typical sequence of operation of these lines. After a start from the Interdata has been sensed, the TSG waits for its internal clock pacer. This starts the scenario sequence.

The first line to be exercised is normally the Transmit Enable 2 line. This controls the power supply turn-on of the ENI A300 solid-state power amplifier. This amplifier requires ≃ 200 μs to turn-on completely. This line is active low at the input to the A300. The next line active (also low) is the main Transmit Enable 1. This line is used for multiple purposes. In the receiver, it mutes by opening the antenna multiplexer switch and the Fast diode attenuator control. If the overload protection latch in the receiver has been tripped, the Transmitter Enable 1 line resets the latch providing that the overload condition is corrected. In the high power amplifier, the Transmit Enable turns on the cathode current in the final tubes. This occurs quickly and only 30 μs delay is required before RF drive can be applied. The next active line is the tranmitter keying line. This controls the length of the RF pulse transmitted. While this line is active, the two Transmitter phase code lines $\emptyset_1$ and $\emptyset_2$ can be used to modulate the phase with a sequence of 1 out of 4 quadrature phase states. Following the end of the transmitter keying pulse, the two Transmit Enable lines are taken inactive and the system reverts to receive. Data are now acquired at the desired ranges by enabling the FEP input memory write enable. This can be enabled and disabled as many times as desired as long as the total number of memory locations filled does not exceed 512. If the transmitter keying line is now again taken active and any phase code repeated, a low level pulse will be generated at the calibration pulse output. This is normally fed to the receiving antennas and data acquired to form a calibration record of the system. During the data acquisition interval, the receiver fast attenuation lines may be changed at specific ranges to give 0, 20, or 40 dB changes in attenuation. The response time of the attenuator is faster than the characteristic response time of the receiver.

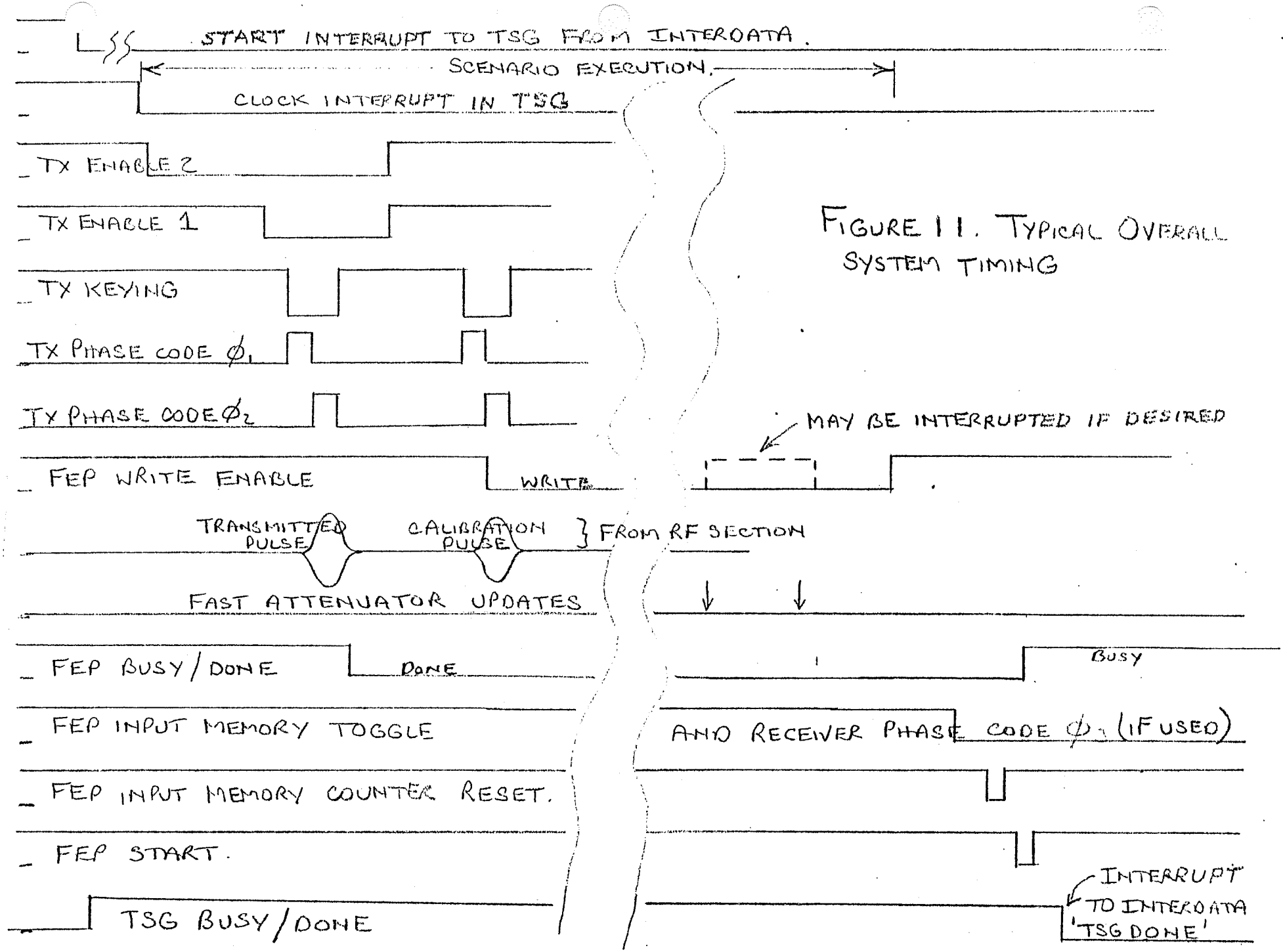


FIGURE 11. TYPICAL OVERALL SYSTEM TIMING

At the completion of the timing scenario execution, the TSG tests the FEP busy/done flag and, if necessary, program loops until a done is sensed. The TSG then reverses the FEP input memories and issues a reset to the address counter. A FEP starting address is issued and the FEP start control line taken active. At some point in this last sequence, the receiver phase control line $\emptyset_3$, which provides a 180° phase reversal in the antenna multiplexers, can be reversed if desired. The TSG at this point has completed its program and loops, sensing for a new start from the Interdata after taking its status line to "done."

5.2 Operating Sequence

The basic operating sequence and data pipelining and the interactions between the Interdata, the FEP, and the TSG are illustrated in Figures 12 and 13. This is of course dependent on Interdata programming, but the details are unlikely to change much for any basic sounding operation.

Taking the sequence from a start-up (NB sections with the same number occur within the same basic timing interval):

1(a) The Interdata loads a command byte into the TSG and sets the desired receiver/transmitter control parameters (frequency, attenution, etc.).

1(b) The Interdata issues a TSG ST (start) to the TSG, by toggling the non maskable interrupt line via the D10.

2(a) On the next timing index (specified by the TSG program), the TSG starts the timing sequence beginning with the transmitter enable and transmitter pulse 1 through terminating the data acquisition in the FEP input memories connected to the ADC's. The TSG then tests the FEP busy/done and if done reverses the FEP input memory, loads an FEP starting address, and issues an FEP start. Depending on the type of measurement and the programs selected, this sequence may loop a specified number of times. At the completion of the overall sequence, the TSG issues an interrupt TSG Done INT to the Interdata.

2(b) The Interdata changes frequency, attenuation, antenna selection, etc., as required and issues a new TSG ST.

3(a) As 2(a) (pulse 2).

3(b) (Starting in period 2.) The FEP processes the data results from pulse 1 (or pulse sequence 1). When the processing is complete, the FEP places the appropriate output memory with the processed data under control of the Interdata ECHO DMA port and issues an interrupt FEP Data Available INT to the Interdata.

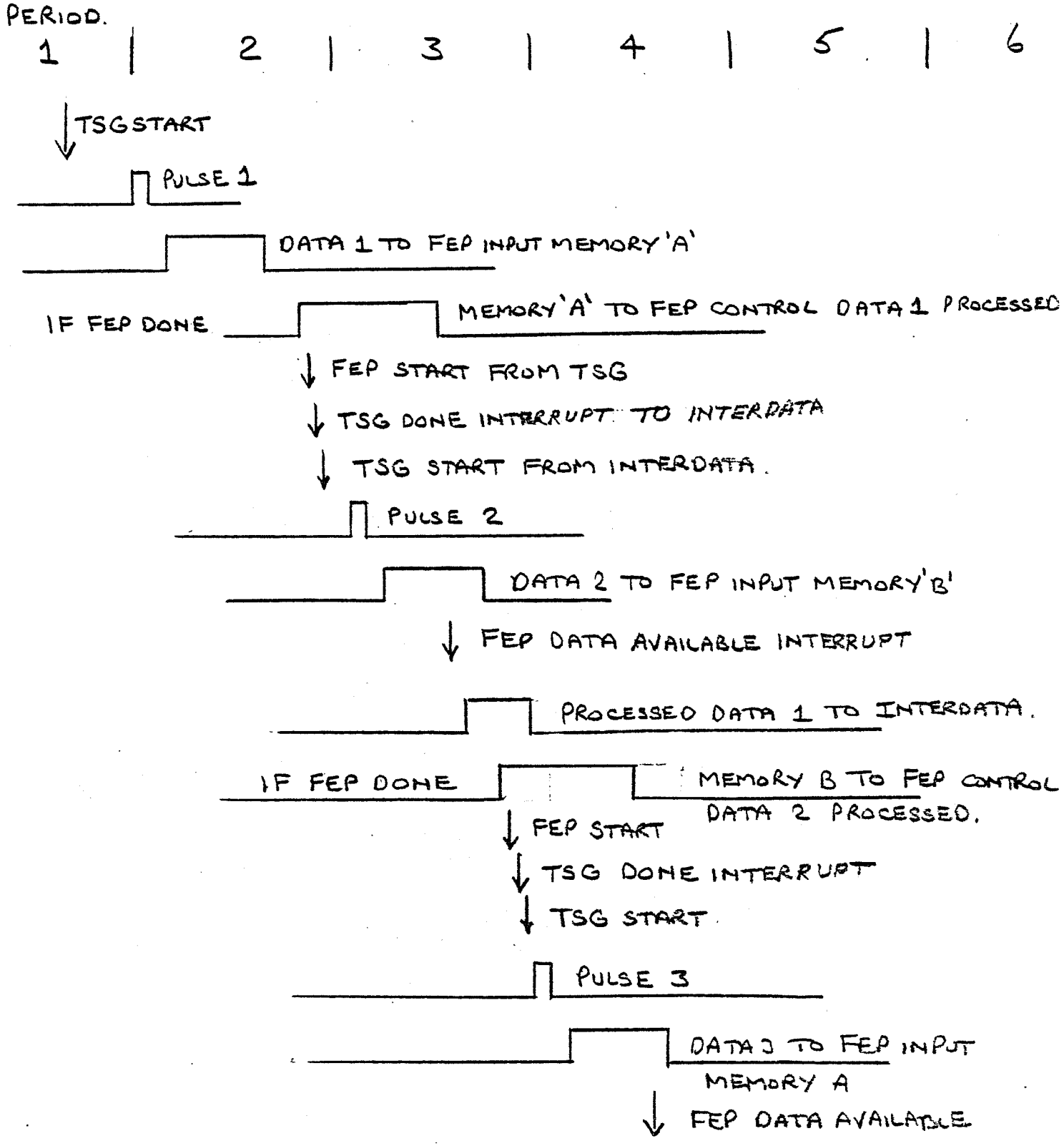
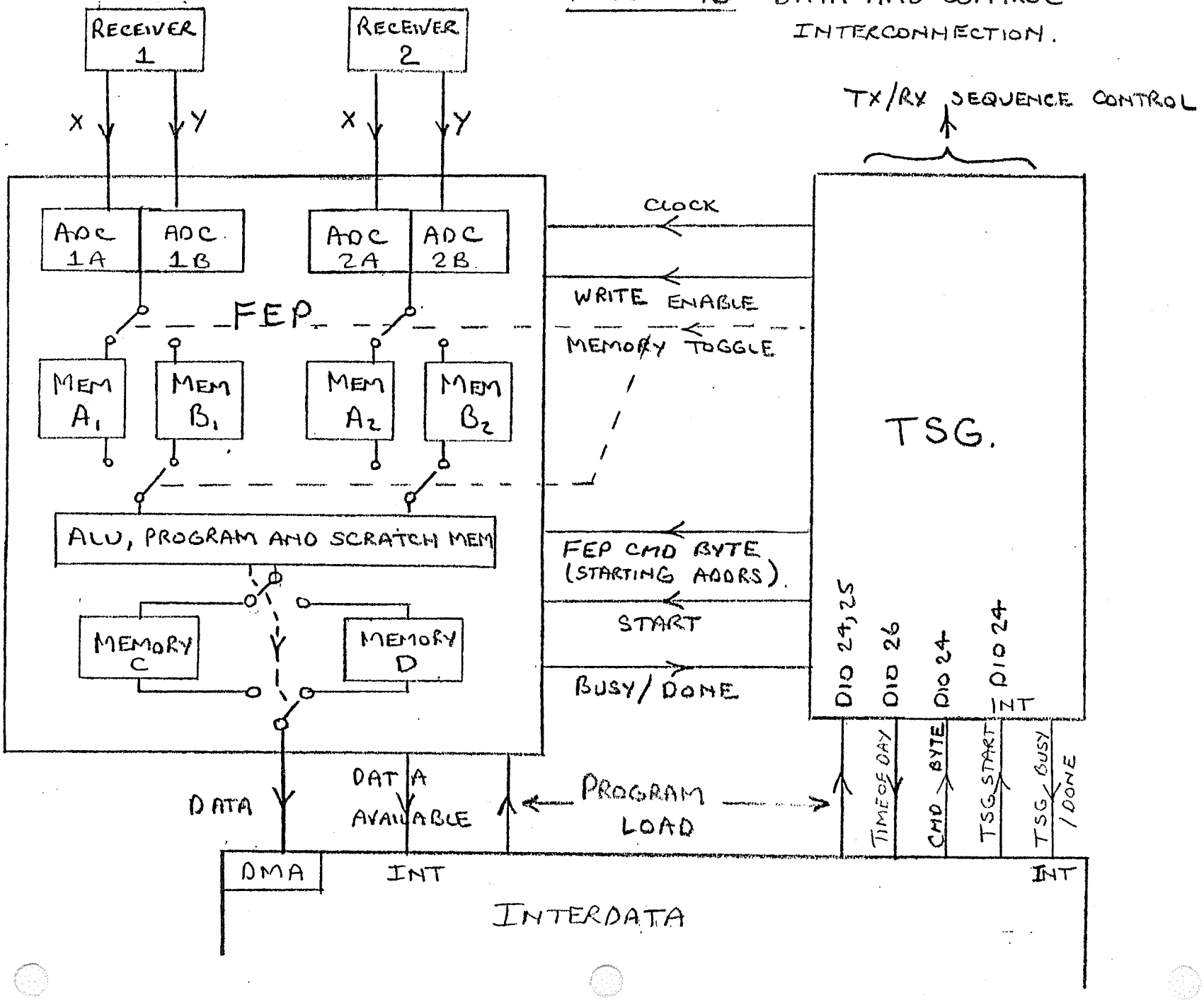


FIGURE 12. BASIC DATA PIPELINE FLOW.

FIGURE 13 DATA AND CONTROL INTERCONNECTION.



3(c) (May overlap into 4.) The Interdata responds to the FEP INT by instructing the DMA controller (SELCH) to load data from pulse 1 from the FEP output memory into the Interdata memory.

3(d) As 2(b).

4(a) As 3(a) (pulse 3).

4(b) 3(b) for data results from pulse 2. Checking that data from previous processing has been read.

4(c) As 3(c) for data results from pulse 2.

4(d) As 3(d).

5(a) As 4(a) (pulse 4).

Etc.

In the case of signal averaging or complementary coded pulse deconvolution operations, the TSG and FEP operate together to form a sequence of transmitted pulses which are operated on by the FEP to form one output data block for the Interdata. The sequencing is controlled by the TSG in its repeat count mode and/or by more complex scenarios, e.g., both parts of a complementary code sequence can be sent as one scenario. In this mode, the repetition rate limitations are set by the time required for program execution by the TSG and FEP and this is not limited by the Interdata.

6. THE HOUSEKEEPING ADC/MUX

6.1 General

The Housekeeping ADC and Multiplexer is used for the collection of housekeeping parameters such as voltages and temperatures in the system and may also, with suitable system programming, be used to obtain data from external geophysical sensors. Note that the main XY receiver outputs are separately digitized by converters contained in the FEP. The ADC system consists of commercial building block modules forming a 64-channel multiplexer and 12-bit ADC which is interfaced to the DIO bus to permit address selection and conversion. A conversion is completed in $\simeq$ 30 µs. The inputs are unbalanced, $\pm$ 10 V range, and the output is coded in offset binary: -10 V = 000_{16} and + 10 V = FFF_{16}.

6.2 Circuit Description

The schematic of the system is in drawing HFS 400.

The system selects (on demand from the CPU) a specific (1 out of 64) analog channel for the ADC, where the analog voltage at this channel is converted to a 12-bit digital data word. The End-Of-Conversion (EOC) is sent to the CPU and its result is stored in the ADC for transfer to the CPU on demand.

This data cycle starts with a CPU-originated address 33_{16} = 110011 placed on the 6-bit DIO address bus. A 6-bit Unified Bus Comparator IC 1 (DM8131) is used to detect equivalence between two 6-bit words. One comes from the 6-bit address bus and is latched-in by ADDRESS-STROBE; the other is provided by 6 hardwired bits, changeable by wire links. The address coincidence is sent to a tri-state octal buffer, IC 2 (DM81LS95N) as an enable (TRUE).

The desired channel number appears as a binary code on the 8-bit DIO OUTPUT DATA line. As only 6 of the available 8 bits are used, the code can reflect up to 64 channels.

The result of 33_{16} detection in IC 1 ($\overline{\text{ADDR}}$) enables IC 2 in coincidence with its DATA STROBE input. The channel number is accepted by the channel MUX of the ADC on the occurrence of the LOAD ENABLE = $\overline{\text{ADDR}}$ + DAT STRB pulse and its 2-gate delayed version (IC 8) used as $\overline{\text{STROBE}}$.

The acceptance and number of the required channel can be reported back to the CPU by the DIO Address Y "33" via IC 3 on the DIO data lines returning to the CPU.

The ADC is described in the MP6848 Expander and the MP6812 ADC data sheets (Appendix 3).

The time relationships pertaining to the ADC, from the address update to the data word output to the CPU, are shown in Figure 14.

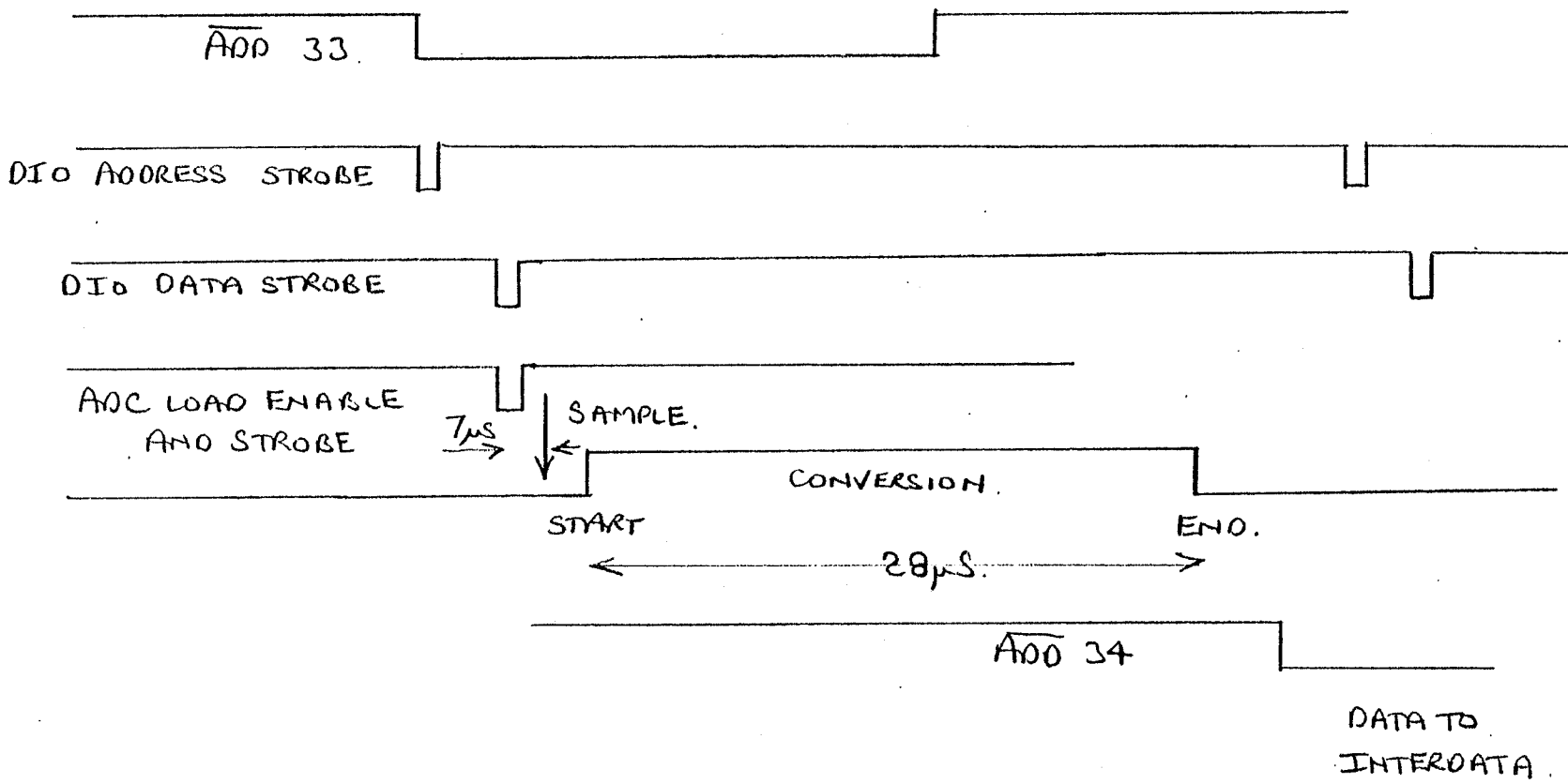


FIGURE 14. HOUSEKEEPING ADC TIMING.

The conversion starts 7 µs after the acquisition of channel data due to an internally delayed ADC pulse. End-Of-Conversion (EOC) occurs after a maximum of 28 µs. EOC is buffered by IC 9. The converted data word is presented to the CPU via IC's 4 and 5 on the DIO data input lines, if the DIO Address X "34" and the ADDR STRB are given.

6.3 Operation

Care is necessary in the connection of the inputs to the Housekeeping ADC if errors are to be avoided. The input impedance of the channels is extremely high (> 100 MΩ) and the bias currents although small will produce large offsets in open circuit channels. Unused inputs should be short circuited.

Input voltages must be kept within the limits ± 12 V to avoid errors in other channels. The system uses unbalanced inputs and care must also be taken to minimize ground loop DC offset errors in making connection to signal sources.

AC common mode voltages will also cause errors. Remote sources of data should be buffered by auxiliary instrumentation amplifiers to reduce common mode interference effects.

The source impedance of the inputs should be kept low if errors due to transient charge dumped by the input multiplexer are to be avoided. If the source resitance is >1KΩ it is recommended that a 0.1µF capacitor or greater be added in parallel. Sources which are to be sampled rapidly should come from low impedances if errors are to be avoided.

7. TEMPERATURE SENSORS

7.1 General

Temperature sensors are used to monitor cabinet air temperatures, the High Power Transmitter cooling air temperatures, and ambient temperatures. The sensors are integrated circuits designed for this purpose which produce an output voltage linearly related to temperature (10 mV/°C) and which can be zeroed at 0°C for ease of interpretation. Table 7.1 lists the positions nominally assigned for the sensors. A similar assembly with a different schematic is used in the High Power Transmitter as an overtemperature warning.

7.2 Description

Mechanical details of the temperature probe are shown in drawing number HFS 193. The PC board which is mounted in the sensor can be either a TM (Temperature Monitor) board, or a TC (Temperature Controller) board. The circuit diagrams for both boards are also shown in drawing number HFS 193. The TM board has an analog output proportional to Celsius temperature at 10 mV per Celsius degree. The TC board has a TTL output which goes low when the temperature exceeds a set threshold. The TM board is used in all positions, and, in addition, a TC board is used in #10, the PA upper tube exit air. Characteristics of U1, the LX5700 temperature transducers, are given in Figure 15.

All temperature sensors are connected to the temperature monitor panel, located in rack 1. Those which are located in the same rack are connected through cables having 5 pin amphenol connectors (#5, #6, #12, #13). Those in racks 2 and 3 are connected through cables having 5-pin amphenol connectors to a junction box in each rack, which adapts to a single 25 line ribbon cable with "D" connectors which connects to the temperature monitor panel. A wiring diagram of the temperature monitor panel is shown in drawing number HFS 192. All the temperature sensors receive their $\pm$ 15 volt supply and ground connection from the temperature monitor panel. 1µF capacitors have been added in parallel to all the monitor outputs in most systems to reduce transient noise errors.

An additional sensor containing a temperature control board is mounted at position #10 (PA upper tube exit air), and is connected to the transmitter controller. When the preset temperature is exceeded, the output goes low and signals a fault to the controller, which turns off the transmitter without dumping and sends an interrupt to the Interdata.

The manufacturer's data sheet should be consulted for additional information and specifications of the LX5700 sensor.

LX5600A/LX5600, LX5700A/LX5700 temperature transducers

general description

The LX5600/LX5700 series temperature transducers are highly accurate temperature measurement or control systems for use over a −55°C to +125°C temperature range. Fabricated on a single monolithic chip they include a temperature sensor, stable voltage reference and operational amplifier.

The output of the LX5600/LX5700 is directly proportional to temperature in degrees Kelvin at 10 mV/°K. Using the internal op amp with external resistors any temperature scale factor is easily obtained. By connecting the op amp as a comparator, the output will switch as the temperature transverses the set-point making the device useful as an on-off temperature controller.

An active shunt regulator is connected across the power leads to the LX5600/LX5700 to provide a stable voltage reference. In addition to providing a reference, it regulates the operating voltage to 6.8V. This allows the use of any power supply voltage with suitable external resistors.

The op amp can amplify the 10 mV/°K from the sensor to almost any desired output. The input bias current is low and relatively constant with temperature, ensuring high accuracy when high source impedance is used. Further, the output collector can be returned to a voltage higher than 6.8V allowing the LX5600/LX5700 to drive lamps and relays from a 28V supply.

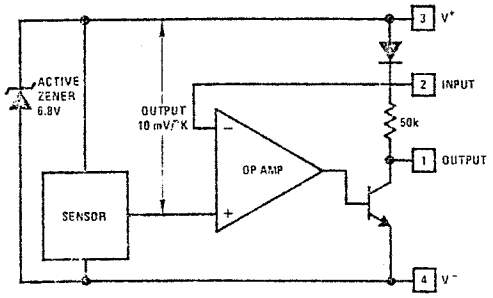
The LX5600 uses the difference in emitter-base voltage of transistors operating at different current densities as the basic temperature sensitive element. Since this output depends only on transistor matching the same reliability and stability as present op amps can be expected.

The LX5600 and LX5600A operate over a −55°C to +125°C range and are available in 4 lead TO-5 package. The LX5700 and LX5700A also operate over the −55°C to +125°C range and are available in the 4 lead TO-46 package.

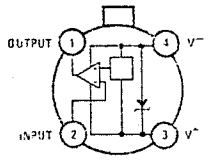
features

- Calibration accuracy of ±4°C over −55°C to +125°C
- Internal op amp with frequency compensation
- Linear output of 10 mV/°K (10 mV/°C)
- Directly calibrated in degrees Kelvin
- Output can drive loads up to 35V
- Stable voltage reference
- Four lead device—minimizing wiring

block and connection diagrams



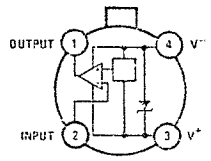
TO-5 Metal Can Package



TOP VIEW

NOTE: PIN 4 CONNECTED TO CASE

TO-46 Metal Can Package



TOP VIEW

NOTE: PIN 4 CONNECTED TO CASE

Figure 15

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Table 7.1

	Position	Function
1	Rack 1 (Computer)	Upper Exit Air
2	" "	Lower Inlet Air
3	" "	Computer Exit Air
4	" "	FEP Exit Air
5	Rack 2 (Receiver)	Upper Exit Air
6	" "	Lower Inlet Air
7	Rack 3 (HPA)	Upper Exit Air
8	" "	Lower Inlet Air
9	" "	PA Inlet Air
10	" "	PA Upper Tube Exit Air
11	" "	PA Lower Tube Exit Air
12	Room	Air Temperature
13	Outside	Air Temperature

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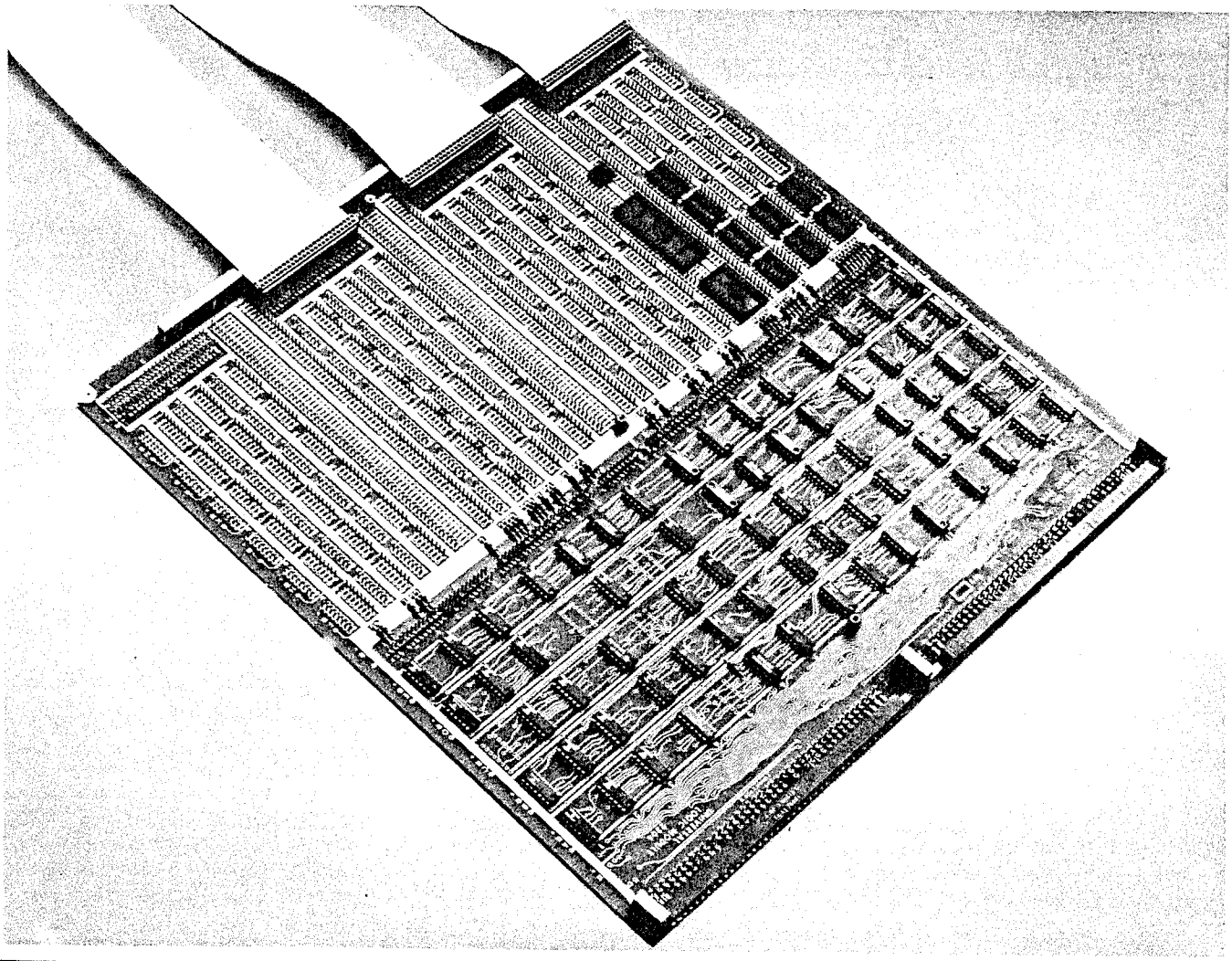
MDB

INTERDATA

UNIVERSAL LOGIC MODULE

TECHNICAL DESCRIPTION



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INTRODUCTION

This document describes the installation, configuration and applications of the MDB Systems Universal Logic Module (ULM) for Interdata computers. This description assumes a general knowledge of designing device controllers to the Interdata Multiplexor or Selector Channel I/O bus.

The ULM is a module that contains the basic logic to interface any device controller to the computer I/O bus with up to four 16-bit input/output data registers. Approximately one-half of the ULM board has provision for wirewrap sockets or circuits (any configuration) or discrete components to accommodate the user's logic design to a particular device or peripheral. The purpose of the ULM is to relieve the logic designer of repetitive design, wiring and checkout of the basic handshake logic to the computer that is common to all device controllers, thereby minimizing the time and cost to produce a complete device controller.

GENERAL DESCRIPTION

The ULM is a printed circuit board that is 15 inches square and requires only one slot position in any Interdata 15-inch chassis. The ULM provides a basic configuration that buffers all computer I/O control and data lines and handshake logic to design any device controller. Within this logic is: device address decoding; status gates to send user status to the processor; and interrupt request and priority logic.

In an optional configuration, the ULM can provide the handshake logic for a second device controller if the user wishes to package two independent device controllers on the same board. This configuration also provides address decoding, status gates and interrupt control logic or, in place of interrupt control logic, the user may specify data channel control logic. If data channel logic is specified, the user must design the interrupt control logic on the wirewrap section of the board.

There are also two register options that the user may specify. Register option 1 has a 16-bit output register that is loaded with the contents of the computer data bus. The outputs of the register are accessible to the user's logic via wirewrap posts. These outputs are also sent to a byte MUX so that the user may transfer 16-bit computer data to a byte-oriented device. This option also includes a 16-bit input register whose contents are loaded from the user's logic. Each byte of this register may be loaded separately so that the user may pack byte oriented data into a 16-bit word. The outputs of this register are multiplexed to the computer data bus under user control.

Register option 2 has a 16-bit output register that is also loaded with the contents of the computer data bus. This register is also implemented as a 16-bit binary up counter so that it can be used as a memory address counter for data channel transfers. The user can increment this counter from the least-significant bit or the second-least-significant bit for memory word transfers.

This register option also has a 16-bit input register whose contents are loaded from the user's logic. Each byte of this register may also be loaded separately and is also implemented as a binary "up" counter that can be incremented from the least-significant or second-least-significant bit. The outputs of this register are also multiplexed to the computer data bus under user control.

For users who only require a byte transfer of data to/from the computer data bus, the above options may be ordered with an eight-bit data bus or eight-bit data registers at a reduced cost.

The wirewrap section of the ULM has provision for up to 92 14 and/or 16-pin integrated circuits. Some of these socket positions will also accommodate 18, 22, 24 or 40-pin devices or any components that have .3, .4 or .6 inch centers with lead spacing of .1 inch. At the top edge of the board, provision is made for four I/O connectors up to 50 conductors each. Ribbon cable sub-assemblies are available from MDB that mate to these I/O connectors.

Separating the wirewrap section from the printed circuit etched logic on the ULM are two rows of wirewrap posts. These allow the user access to the ULM printed logic from his wirewrap logic. At the bottom edge of the board, all I/O pins directly connected to the computer backplane are also accessible via wirewrap posts.

ULM BASIC BOARD

The logic for the ULM basic board is shown on ULM logic drawing 2304-3, sheet 1. All logic terms ending in a 0 are asserted true in the low state (0 volts) and all logic terms ending in a 1 are asserted true in the high state (+5 volts), e.g; the term ID010 is input data bit 01 and is true in the 0 volt state.

Data Line Bus Drivers and Receivers

The computer data lines D000 - D150 are received by inverting gates whose outputs are called OD001 - OD151. OD081 - OD151 drive inverters whose outputs are OD080 - OD150. All outputs are accessible to the user on wirewrap posts. D080 - D150 are gated with RATN10 or RATN20. RATN10 goes true when the interrupt control logic on the basic controller returns a device controller address in response to an interrupt acknowledge instruction. RATN20 returns an address from the second device controller option. RATN20 has a pull-up resistor and is brought out to wirewrap post Y100. The second device controller drives this line with an open-collector gate. If the user mechanizes a third device controller (a user may design in more than the second device option offered) that handles interrupts on the wirewrap section of the ULM, he may also drive this line with an open-collector gate.

Computer data lines D000-D150 are driven by the ULM by dual buffers from the terms called ID000 - ID150. These lines have pullup resistors and are accessible by wirewrap posts to the user. The ULM uses these lines to return status, device address, and data from the register options with open-collector gates. If the user needs to return additional data to the computer I/O from the wirewrap section, he also must drive these lines with open-collector gates. Table I lists the data bus terms and their wirewrap pin numbers.

Device Address Decoding and Control

The device code address of the basic controller must be wired by the user by connecting the terms DS108 - DS115 in the device address decoding section to the appropriate output data bus terms OD080/1 - OD150/1. As an example, to select the device address of X'8B' connect the following wirewrap pins:

DS108	Y116	to	X95	OD081
DS109	Y117	to	X96	OD090
DS110	X115	to	X42	OD100
DS111	X116	to	X100	OD110
DS112	Y114	to	Y68	OD121
DS113	Y115	to	X101	OD130
DS114	X113	to	X93	OD141
DS115	X114	to	X94	OD151

The device address flip-flop ADF11 is used to gate the control signals SR1, DR1, DA1 and CMD1 to form the terms SRG11, DRG11, DAG11 and CMG11, respectively. All control lines from the computer's I/O bus are buffered with gates. These outputs are used in the basic device controller logic and the second controller logic, and are also connected to

Table 1. Input/Output Data Bus Pin Assignment

Computer Data Bus	Pin Number	ULM Output Bus	Pin Number	ULM Input Bus	Pin Number
D000	111-1	OD001	Y57	ID000	Y45
D010	211-1	OD011	X58	ID010	Y66
D020	112-1	OD021	X56	ID020	Y67
D030	212-1	OD031	Y58	ID030	Y50
D040	113-1	OD041	X59	ID040	Y51
D050	213-1	OD051	X60	ID050	Y39
D060	114-1	OD061	X57	ID060	Y35
D070	214-1	OD071	Y59	ID070	Y28
D080	115-1	OD081 OD080	X95 Y95	ID080	Y123
D090	215-1	OD091 OD090	X97 X96	ID090	Y125
D100	116-1	OD101 OD100	X67 X42	ID100	Y122
D110	216-1	OD111 OD110	X99 X100	ID110	Y124
D120	117-1	OD121 OD120	Y68 X98	ID120	Y119
D130	217-1	OD131 OD130	Y94 X101	ID130	Y121
D140	118-1	OD141 OD140	X93 Y96	ID140	Y118
D150	218-1	OD151 OD150	X94 X102	ID150	Y120

wirewrap pins. These pins are provided to allow the user to mechanize a third controller in the wirewrap section. Table 2 lists the control line signals and their wirewrap pin numbers..

Table 2 Computer Input Control Signals

Computer Control Bus	Pin Number	ULM Control	Pin Number	ULM Gated Control	Pin Number
ADRS0	219-1	ADRS1	Y112	SAD10	Y113
SR0	119-1	SR1	X106	SRG10 SRG11	X109 ---
DR0	120-1	DR1	Y107	DRG10	Y71
DA0	221-1	DA1	Y111	DAG10	X111
CMD0	220-1	CMD1	Y110	CMG10 CMG11	X110 X103
SCLR0	126-1	SCLR1 SCLR10 SCLR20	X66 Y105 X104		

The user may use the gated control signal CMG10 or CMG11 as a load pulse to a user-provided command register for such functions as starting a device, or setting a device mode such as read or write, etc. The DAG10 may be connected to output data to a device, or to load the output data registers with the ULM's register option. The user may connect the DRG10 signal to enable user-provided open-collector gates that are tied to the input data bus ID000-ID150 with inputs from an input device or, with the register option, he may load data into the input data register and connect DRG10 to the register to output the contents to the computer data bus.

SRG10 enables eight status gates with outputs connected to the ULM input data bus ID080 -ID150. Each gate input S1081 - S1151 is connected to a wirewrap post to allow the user to return status information from the user's logic. A high logic level on the inputs will return a true status to the computer. Unused status inputs must be connected to ground to return false status for that bit. The following are the status gate input pin assignments:

USER STATUS INPUT		COMPUTER DATA BUS
S1081	X122	D080
S1091	X124	D090
S1101	X121	D100
S1111	X123	D110
S1121	X118	D120
S1131	X120	D130
S1141	X117	D140
S1151	X119	D150

The gated control signals SAD10, DAG10 amd CMG10 are gated together to return SYN0 to the computer within 50 nanoseconds. The gated control signals SRG10, DRG10 and RATN10 are gated together to return SYN0 to the computer within 180 nanoseconds. Any control signals from the user's logic that return SYN0 must be connected directly to the computer's I/O connector at pin 123-1 with an open-collector gate.

The computer's general reset signal SCLR0 is gated with a gate input Y103 to allow the user to generate a controller reset from an external source. SCLR10 is used to reset the ULM controller logic and is connected to a wirewrap pin. SCLR20 is connected to a wirewrap pin but is not used by the ULM logic. Either signal may be used by the user to initialize his logic.

For computer half word data transfers the HW0 signal is dual buffered and connected to two wirewrap pins HW10 (Y101) and HW20 (Y102). One of these pins must be connected by the user to the ADF10 output (X50) of the address decode flip flop. The other pin may be connected to the second device controller or to the user's logic.

Interrupt Control and Priority Logic

The interrupt circuitry is controlled by program control. Data bits 8 and 9 of the output command instruction control the interrupt logic in the following manner:

Data bit 8	9		
$\overline{0}$	$\overline{1}$	Enable -	Interrupt logic is enabled. When the user sets an interrupt request the ULM will set the ATN0 line true.
1	0	Disable -	Interrupt logic is disabled but armed. The interrupt will be queued in the ULM but will not set the ATN0 signal until enabled.

Data bit 8	9		
1	1	Disarm -	Interrupt will not be queued in the ULM. Any interrupt requests will be ignored by the ULM. A system reset will disarm interrupts in the ULM.
0	0	No Change-	The previous control state issued to the ULM will not change with this code.

When interrupt control is enabled the user can issue an interrupt request on IR10, pin Y109. A negative-going transition will set the ATN0 (223-1) line true to the computer. The interrupt priority logic receives RACK0 (122-1) from the computer and if the ATN0 flip flop is set, it generates the pulses RATN10 and RATN11. RATN10 gates D080-D150 to force OD080/1 - OD150/1 true. This logically causes the device address decode inputs DS108 - DS115 to assume the state of the device address. (X'8B' in the case of a previous example.) RATN10 also returns the SYN0 line to the processor and resets the ATN0 flip-flop. RATN11 is used to gate DS108 - DS115 to the input data bus ID080 - ID150, thereby returning to the processor the device address of the ULM.

If RACK0 is received and the ATN0 flip-flop is reset, or the interrupt control is not enabled, the interrupt priority logic generates TACK10 to wirewrap pin X108. If the basic controller is the only controller on the ULM with interrupt capability, the user must connect TACK10 to TACK0 pin X107 which is connected to the I/O connector (222-1).

If the second controller or user-mechanized controllers have interrupt capability, then the TACK10 from the basic controller's priority logic must be connected to the RACK0 input of the other controller in a daisy-chain manner so that the last controller will have its TACK0 connected to the I/O connector TACK0 (X107). With multiple controllers on the ULM the basic controller will always have the highest priority.

Figures 1 and 2 are a design example using the basic controller with register option 1, with a simplified 8-bit input peripheral device such as a tape reader. Figures 3 and 4 are an example using the device controller and register 1 option to interface to a simple 8-bit output device.

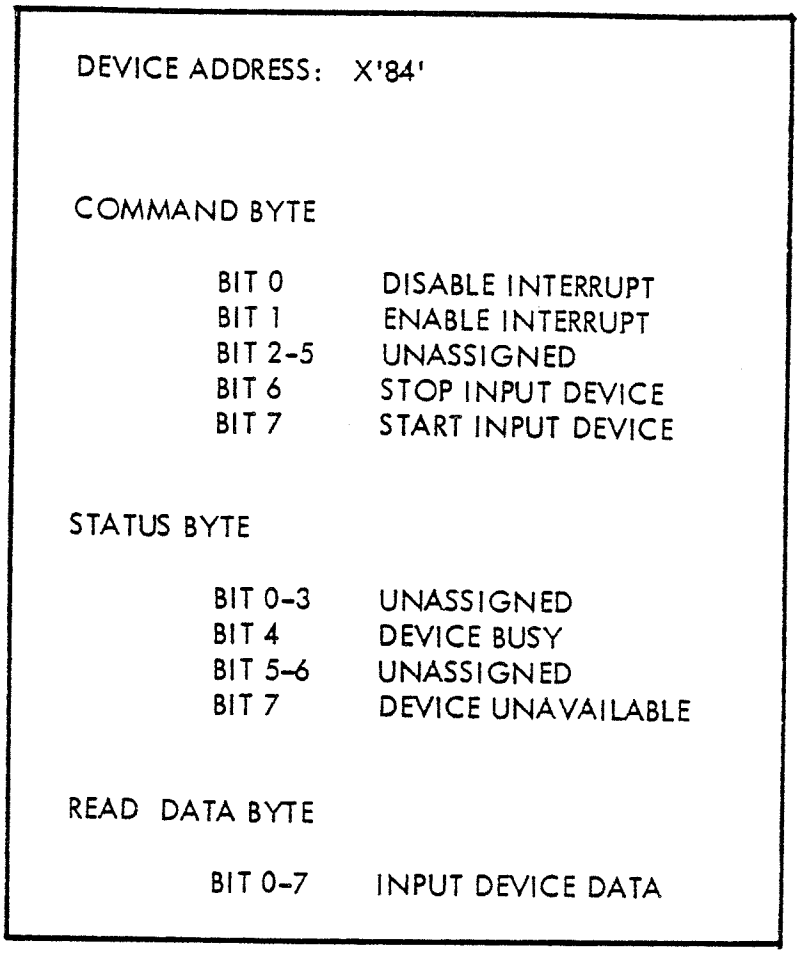


Figure 1 Example of Program Format for Input Device Controller

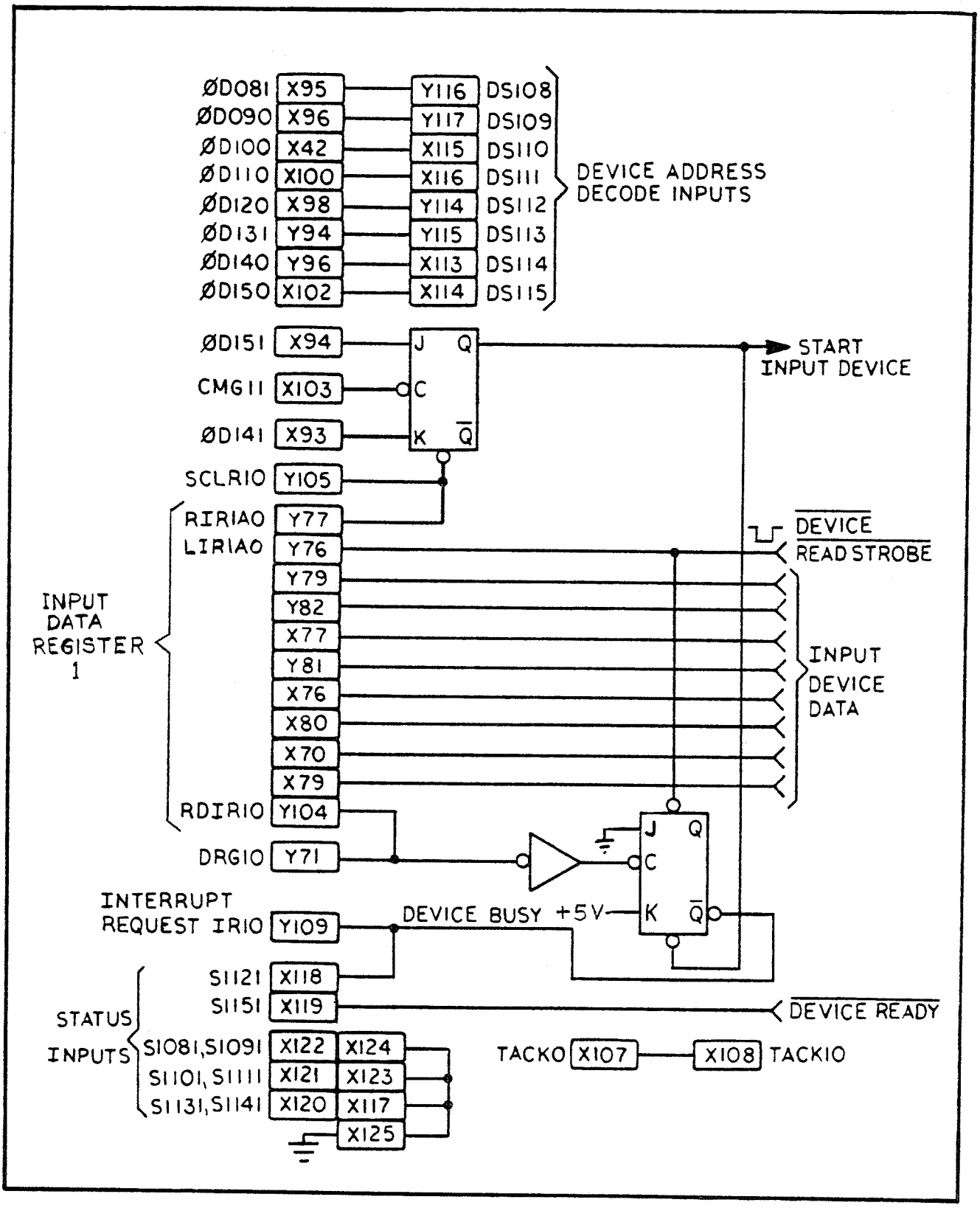


Figure 2 Example of Interface for Input Device Controller

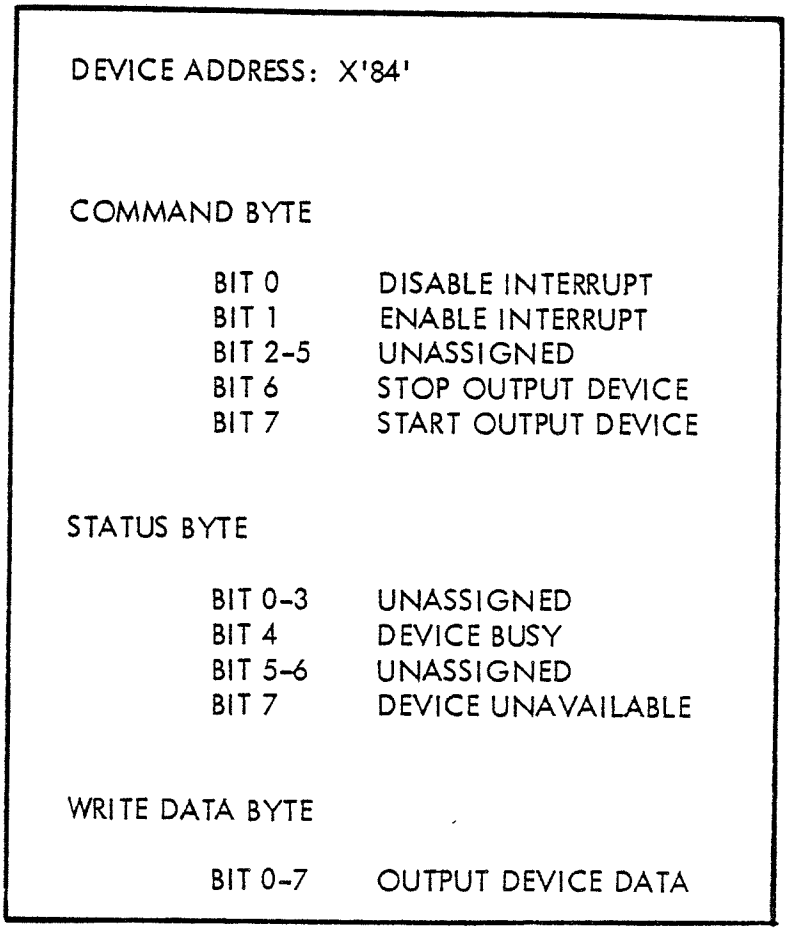


Figure 3 Example of Program Format for Output Device Controller

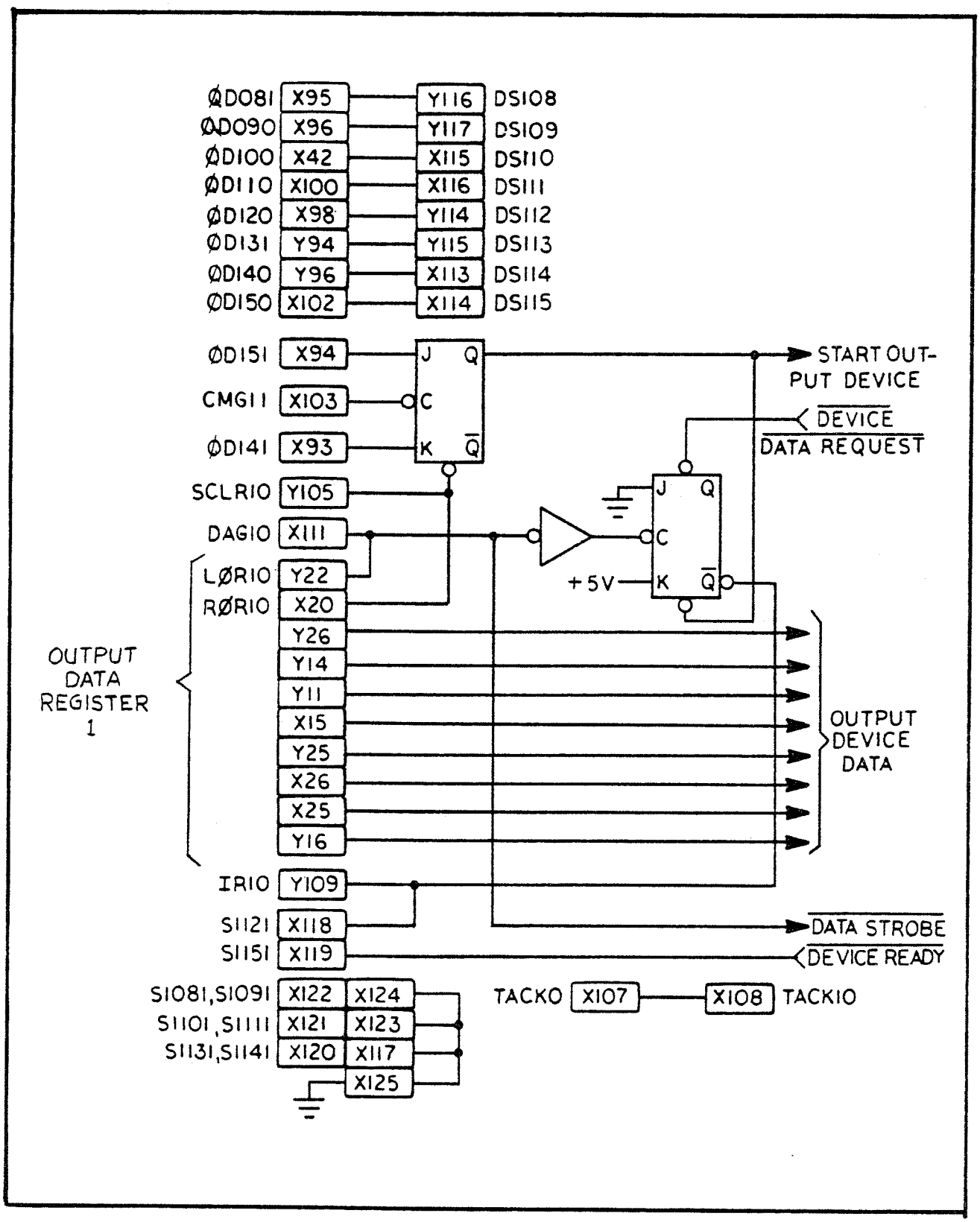


Figure 4 Example of Interface for Output Device Controller

SECOND CONTROLLER OPTION WITH INTERRUPT CONTROL

The logic for the ULM second controller option with interrupt control is shown on Sheet 2 of the logic drawing. Basically this controller is used in the same manner as the basic controller. The device code must be wired by the user to DS208 - DS215. These pin numbers are as follows:

DS208	Y64
DS209	X65
DS210	X63
DS211	Y65
DS212	X64
DS213	Y63
DS214	X62
DS215	Y62

The user status gate inputs are designated S2081 - S2151 and are assigned the following pin numbers:

S2081	X71
S2091	Y75
S2101	Y72
S2111	X74
S2121	X72
S2131	Y74
S2141	Y73
S2151	X73

The gated control signals are listed as follows:

SAD20	X41
SRG20	Y42
DRG20	X27
DRG30	Y27
DAG20	X34
DAG30	X28
CMG20	X33
CMG21	X68

In the second controller option there are two additional gated control signals. DRG30 and DAG30 are enabled only when the line DADR30, Y40 is asserted by the user. These signals can be used in the special case where a user has a requirement to load two separate registers or read two separate registers in his controller.

This can be done by connecting the address decode lines to decode dual consecutive device addresses such as X'84' and X'85'. The program can then load one register with a write data instruction to device X'84; and the other register to device X'85'; or, similarly, read the registers with a read data instruction to device address X'84' and X'85'. Figure 5 is an example using device addresses X'84' and X'85' where the DAG20 and DRG20 control signals respond to X'84; and the control signals DAG30 and DRG30 respond to device address X'85'.

Note that when using this example, the returned device address for interrupts will always be X'84; and that the command control signal CMG20 and status control signal SRG20 will respond to both X'84'and X'85'.

The interrupt logic on the second controller is the same as on the basic controller with one exception. This controller has its RACK20 input to the priority logic connected to wirewrap pin Y2. This pin must be connected to a TACK0 output of a higher priority controller on the ULM or, if it is the only interrupting controller, it must be connected to RACK0, pin 122-1 on the I/O connector. The user can set an interrupt request to this controller by asserting the IR20 input, pin Y43.

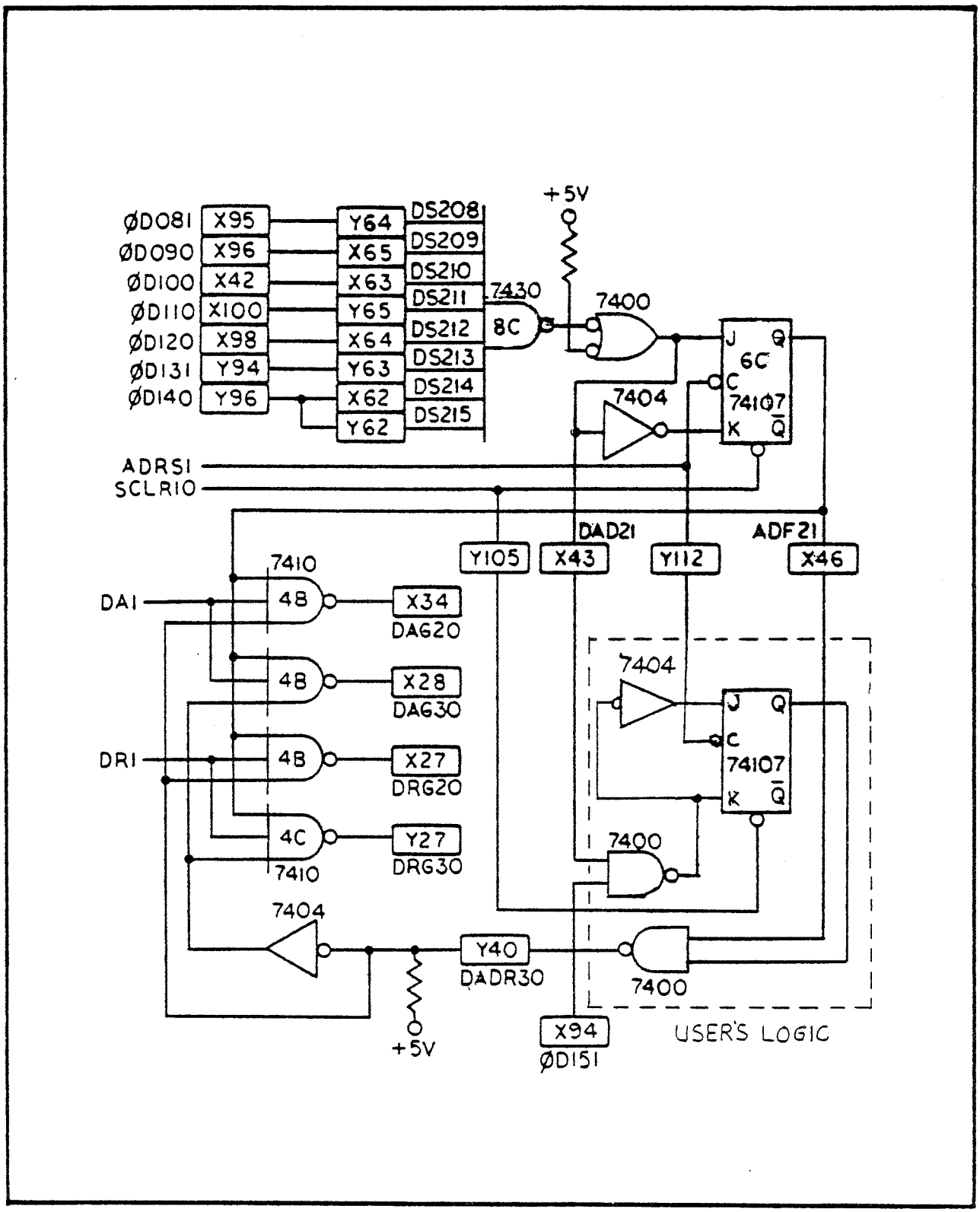


Figure 5 Interface Using DAG30 and DRG30

REGISTER 1 OPTION

The ULM register 1 option consists of two 16-bit data registers that are shown on the logic drawing sheet 3. The output data register has its data inputs connected to the ULM output data bus OD001-OD151. The outputs of this register are accessible by wirewrap pins and are also connected to a byte multiplexer. This register is loaded from the output data bus when the user asserts the load signal LOR10, pin Y22. Typically this signal would be connected to DAG10 of the basic controller. Note that the HWO signal must be asserted by the controller to transfer 16 bits of data into this register. If data transfer from the computer is in the byte mode, then the register output loaded from OD081-OD151 is the only valid data. The register output pins are:

OUTPUT REGISTER 1 DATA INPUT	OUTPUT REGISTER 1 DATA OUTPUT	OUTPUT REGISTER 1 DATA INPUT	OUTPUT REGISTER 1 DATE OUTPUT
OD001	Y20	OD081	Y16
OD011	X21	OD091	X25
OD021	X19	OD101	X26
OD031	Y21	OD111	Y25
OD041	X10	OD121	X15
OD051	X24	OD131	Y11
OD061	X14	OD141	Y14
OD071	Y24	OD151	Y26

This register may be reset to zero by asserting the reset control signal ROR10, pin X20.

The byte mux may be used to transfer computer half-word data to a byte-oriented device. The mux control signal STR0, pin X7 must be asserted low to enable the output of the mux. The signal BSEL1, pin X23 when low will select the most significant byte of the output register (loaded from OD001 - OD071). When high, the least significant byte of the register will be selected. The byte mux outputs are:

MUX INPUT BSELI = LOW	BSEL1 = HIGH	MUX OUTPUT STRO = LOW
Y20	Y16	Y7
X21	X25	X6
X19	X26	X22
Y21	Y25	Y23
X10	X15	Y8
X24	Y11	X8
X14	Y14	X13
Y24	Y26	Y15

The Input Data Register 1 consists of two separate byte registers, each with a load and reset control input. The data inputs are connected to wirewrap pins to be loaded by user data, and the data outputs are connected to wirewrap pins and open-collector gate inputs connected to the ULM input data bus ID000 - ID150. The user may allow the program to read the two registers with a half-word read instruction by connecting the read gate control RDIR10, pin Y104, to the basic controller's DRG10 signal. With byte data transfers, only the byte register connected to ID080 - ID150 will be read. By connecting both register data inputs to a byte-oriented device and alternately loading each register, the user can pack bytes into a half word to be read by the program. The register pin numbers are:

MSB INPUT REGISTER 1

Load Control LIR1B0 Y 33
Reset Control RIR1B0 Y46

Data Input	Data Output	Input Data Bus
Y44	X51	ID000
Y49	X47	ID010
X44	X45	ID020
X48	Y48	ID030
X30	Y29	ID040
X32	Y31	ID050
Y30	X29	ID060
Y32	X31	ID070

LSB INPUT REGISTER 1

Load Control LIR1A0 Y76
Reset Control RIR1A0 Y77

Data Input	Data Output	Input Data Bus
X79	X81	ID080
X70	Y84	ID090
X80	X82	ID100
X76	X84	ID110
Y81	X83	ID120
X77	Y85	ID130
Y82	Y83	ID140
Y79	X85	ID150

REGISTER 2 OPTION

The ULM register 2 option consists of two 16-bit data registers that are shown on sheet 4 of the logic drawing. These registers may be used as data registers for data transfer, or as a memory address counter and word block counter for data channel operation.

The output data register has its data inputs connected to the ULM output data bus OD001 - OD151. The user may load this register with computer data by asserting the load input signal LOR20, pin Y12. He may reset the contents of this register by asserting the reset input signal ROR20, pin Y10. The outputs of this register are connected to wirewrap pins as follows:

REGISTER 1 OPTION

The ULM register 1 option consists of two 16-bit data registers that are shown on the logic drawing sheet 3. The output data register has its data inputs connected to the ULM output data bus OD001-OD151. The outputs of this register are accessible by wirewrap pins and are also connected to a byte multiplexer. This register is loaded from the output data bus when the user asserts the load signal LOR10, pin Y22. Typically this signal would be connected to DAG10 of the basic controller. Note that the HWO signal must be asserted by the controller to transfer 16 bits of data into this register. If data transfer from the computer is in the byte mode, then the register output loaded from OD081-OD151 is the only valid data. The register output pins are:

OUTPUT REGISTER 1 DATA INPUT	OUTPUT REGISTER 1 DATA OUTPUT	OUTPUT REGISTER 1 DATA INPUT	OUTPUT REGISTER 1 DATE OUTPUT
OD001	Y20	OD081	Y16
OD011	X21	OD091	X25
OD021	X19	OD101	X26
OD031	Y21	OD111	Y25
OD041	X10	OD121	X15
OD051	X24	OD131	Y11
OD061	X14	OD141	Y14
OD071	Y24	OD151	Y26

This register may be reset to zero by asserting the reset control signal ROR10, pin X20.

The byte mux may be used to transfer computer half-word data to a byte-oriented device. The mux control signal STR0, pin X7 must be asserted low to enable the output of the mux. The signal BSEL1, pin X23 when low will select the most significant byte of the output register (loaded from OD001 - OD071). When high, the least significant byte of the register will be selected. The byte mux outputs are:

MUX INPUT BSELI = LOW	BSEL1 = HIGH	MUX OUTPUT STRO = LOW
Y20	Y16	Y7
X21	X25	X6
X19	X26	X22
Y21	Y25	Y23
X10	X15	Y8
X24	Y11	X8
X14	Y14	X13
Y24	Y26	Y15

The Input Data Register 1 consists of two separate byte registers, each with a load and reset control input. The data inputs are connected to wirewrap pins to be loaded by user data, and the data outputs are connected to wirewrap pins and open-collector gate inputs connected to the ULM input data bus ID000 - ID150. The user may allow the program to read the two registers with a half-word read instruction by connecting the read gate control RDIR10, pin Y104, to the basic controller's DRG10 signal. With byte data transfers, only the byte register connected to ID080 - ID150 will be read. By connecting both register data inputs to a byte-oriented device and alternately loading each register, the user can pack bytes into a half word to be read by the program. The register pin numbers are:

MSB INPUT REGISTER 1

Load Control LIR1B0	Y33
Reset Control RIR1B0	Y46

Data Input	Data Output	Input Data Bus
Y44	X51	ID000
Y49	X47	ID010
X44	X45	ID020
X48	Y48	ID030
X30	Y29	ID040
X32	Y31	ID050
Y30	X29	ID060
Y32	X31	ID070

LSB INPUT REGISTER 1

Load Control LIR1A0	Y76
Reset Control RIR1A0	Y77

Data Input	Data Output	Input Data Bus
X79	X81	ID080
X70	Y84	ID090
X80	X82	ID100
X76	X84	ID110
Y81	X83	ID120
X77	Y85	ID130
Y82	Y83	ID140
Y79	X85	ID150

REGISTER 2 OPTION

The ULM register 2 option consists of two 16-bit data registers that are shown on sheet 4 of the logic drawing. These registers may be used as data registers for data transfer, or as a memory address counter and word block counter for data channel operation.

The output data register has its data inputs connected to the ULM output data bus OD001 - OD151. The user may load this register with computer data by asserting the load input signal LOR20, pin Y12. He may reset the contents of this register by asserting the reset input signal ROR20, pin Y10. The outputs of this register are connected to wirewrap pins as follows:

OUTPUT REGISTER 1 DATA INPUT	OUTPUT REGISTER 2 DATA OUTPUT	OUTPUT REGISTER 2 DATA INPUT	OUTPUT REGISTER 2 DATA OUTPUT
OD001	Y9	OD081	X4
OD011	X11	OD091	Y18
OD021	X9	OD101	Y5
OD031	X12	OD111	X17
OD041	X5	OD121	X3
OD051	Y17	OD131	Y19
OD061	Y6	OD141	Y4
OD071	X16	OD151	X18

This register is also implemented as a binary ripple counter which may be used as a data channel word counter by loading the two's complement of the word or block count, and incrementing the contents after each data channel word transfer. The user can then monitor the outputs to terminate the data channel block transfer when the register overflows to a zero value. This register can be incremented by one by clocking the clock input COR2A0, pin Y3,and connecting the pin X18 output (bit 15) to clock input COR2B0, pin Y13. It may also be incremented by two by clocking the COR2B0 input and not connecting the COR2A0 input. Both clock inputs increment the register on the negative-going transition of the clock.

Input data register 2 consists of two separate byte registers, each with a separate clock input(s), load and reset control input. The data inputs are connected to wirewrap pins to be loaded by user data,and the data outputs are connected to wirewrap pins and open-collector gate inputs connected to the ULM input data bus ID000 - ID150. The user may allow the program to read the two registers with a half-word read instruction by connecting the read gate control RDIR20, pin Y106,to the basic controller's DRG10 output.

This register is also implemented as two separate 8-bit binary ripple counters. The least-significant-byte register may be incremented by one by clocking the CIR2A0 input,and connecting the data output Y90 (bit 15) to the clock input CIR2B0 input. The most-significant-byte register may be incremented by clocking the CIR2C0 input. This register may be used as a data channel memory address counter by connecting the data inputs to the ULM output data bus, connecting the data output Y92 (bit 08) to clock input CIR2C0,and clocking input CIR2B0 after each data channel transfer. The program can then load the starting memory address into this register by connecting the register load inputs to the controller's DAG20 output. The read gate control RDIR20 may be connected to the ULM's data channel controller signal DRG20 which is asserted for each data channel transfer

to allow a controller to send the memory address to the processor for a data channel input or output.

Input data register 2 wirewrap pin assignments are as follows:

MSB REGISTER 2			LSB REGISTER 2		
Load Control LIR2B0		Y52	Load Control LIR2A0		Y86
Reset Control RIR2B0		Y36	Reset Control RIR2A0		Y80
Data Input	Data Output	Input Data Bus	Data Input	Data Output	Input Data Bus
Y54	X52	ID000	Y69	Y92	ID080
Y56	X54	ID010	Y78	X92	ID090
X53	Y53	ID020	X69	X91	ID100
X55	Y55	ID030	X78	Y93	ID110
Y38	X36	ID040	X87	Y91	ID120
X40	X38	ID050	X86	X89	ID130
X37	Y37	ID060	X88	X90	ID140
X35	X39	ID070	Y87	Y90	ID150

SECOND DEVICE CONTROLLER WITH DATA CHANNEL CONTROL OPTION

The ULM second device controller with data channel control is shown on sheet 5 of the logic drawing. It should be noted to the user that this controller has limited use in that it may only be used with the Interdata Model 70, 80 and 85 computer and that it may not be used concurrent with Interdata's selector channel operation.

The data channel control and priority logic is very similar to the interrupt logic. The user may generate a data channel request by asserting the UDCR0 signal, pin Y43. The negative-going transition of this signal will assert the data channel request signal DC0, pin 127-0, to the processor. For a data channel write transfer, the WRT1 signal, pin Y41, must be true which will assert the DCR0 signal, pin 227-0, to the processor when a data channel transfer with the ULM is in operation. The WRT1 signal should be false for a data channel read operation. The processor determines device data channel priority in the same manner as it does for interrupt priority. The user must therefore connect the data channel controller's RACK20 signal, Y2 to X2 which is connected to the computer I/O as RDACK0, pin 128-0 and connect TACK20, pin Y1 to X1 which is connected to TDACK0, pin 228-0. It should be noted that the ULM uses the "1" I/O connector for standard multiplex channel signals and the "0" I/O connector for data channel control

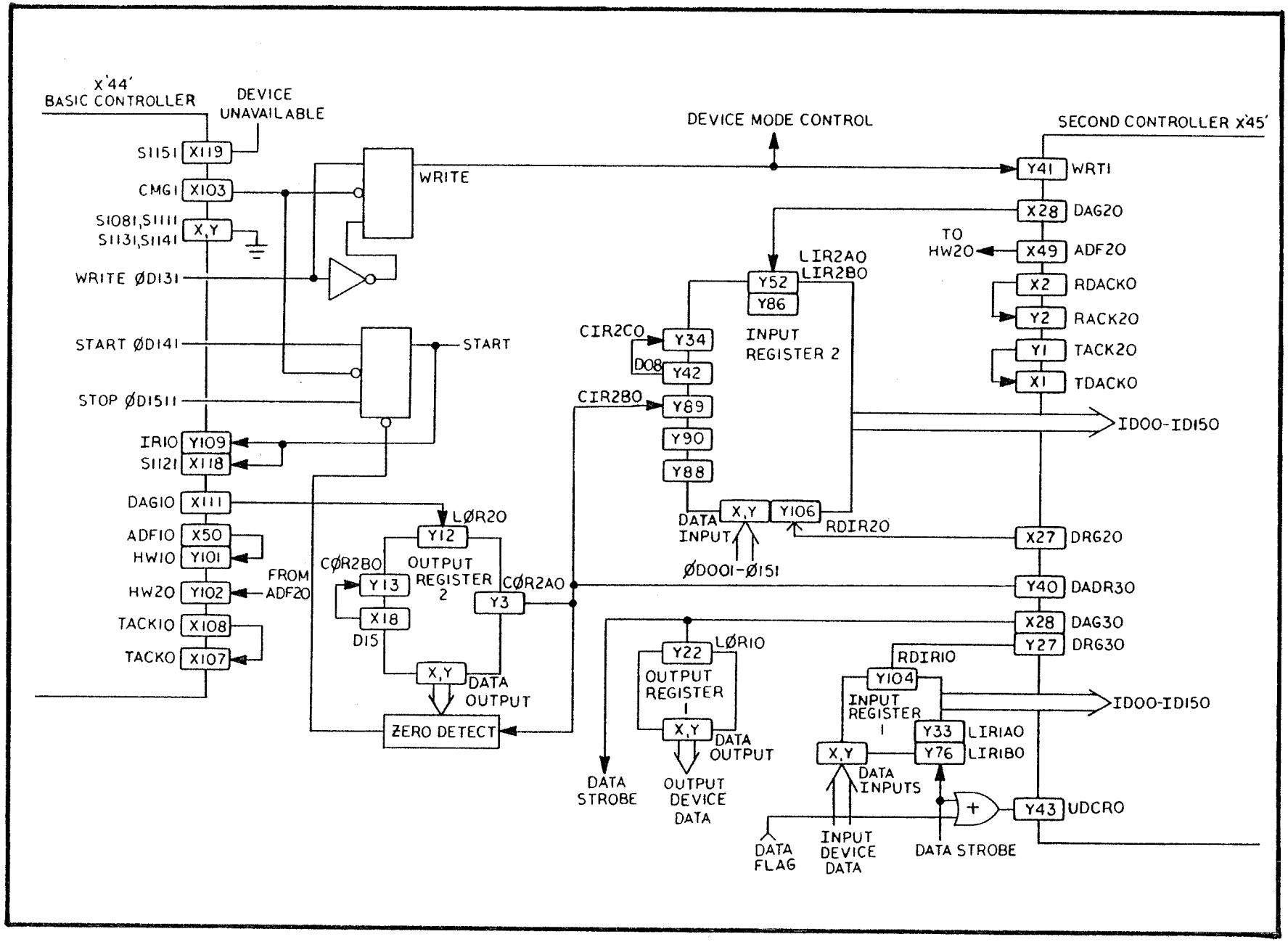


Figure 6 Interface for Data Channel Operation

signals. For a data channel transfer the user must connect the DRG20 signal, pin X27, to gate a memory address on the computer data bus. For a write operation the DRG30 signal, pin Y27, must be connected to gate the half-word data on the computer data bus that is to be written into the memory location defined by the DRG20 address data. For a read operation the user should connect the DAG30 signal, pin X28, to load a data register with inputs connected to the data bus. This is the data read from the memory location defined by the DRG20 address data.

The CMG20, pin X68; or the CMG21, pin X68, signals may be used to load a user's command register under program control. The SRG20 signal, pin Y42, will gate user's status information to the computer data bus. The status information pin numbers are the same as the second controller with interrupt control. The DAG20 signal, pin X34, may be used to load data to the controller under program control. The user can read the current contents of the memory address register with a half-word read instruction to this controller. In this case the DRG20 signal would be asserted for both program control and data channel control. The device address decode input pin assignments are the same as the second controller with interrupt control.

Figure 6 is a block diagram example of using the basic controller and second controller for data channel operation. In this example the basic controller will have a device address of X'44'. The output command will be used to enable interrupts, set read or write mode, and start the data channel operation. The status command will indicate data channel busy and device unavailable. The write-half-word instruction will load output register 2 with block count information. Data channel block complete will generate an interrupt on this controller. The second controller will have the device address X'45'. The command and status instructions will not be assigned for this controller. The write half word instruction will load input register 2 with the starting memory address for the data channel. The read-half-word instruction may be used to read the current contents of this register. Output register 1 will be used for data from memory, and Input register 1 will be used for data to memory.

USER INTEGRATED CIRCUIT WIREWRAP SECTION

The ULM wirewrap section will contain up to ninety-three 14- or 16- pin integrated circuit positions for user-designed logic. There are fifteen columns of IC positions designated 1 - 15, and seven rows designated F, H, J, K, L, M and N. Row F-M have fifteen IC positions while row N has three IC positions in columns 4, 8 and 12.

Columns 1-3, 5-7, 9-11 and 13-15 have a geometric pattern to accommodate standard 16-pin integrated circuits that insert on 0.3 inch centers. These IC locations have pin 8 connected to the ground plane on the component side, and pin 16 connected to the +5-volt plane on the solder side. On the solder side there is also a connection between pin 7 and pin 8 so that these locations have power dedicated for a 14-pin integrated circuit

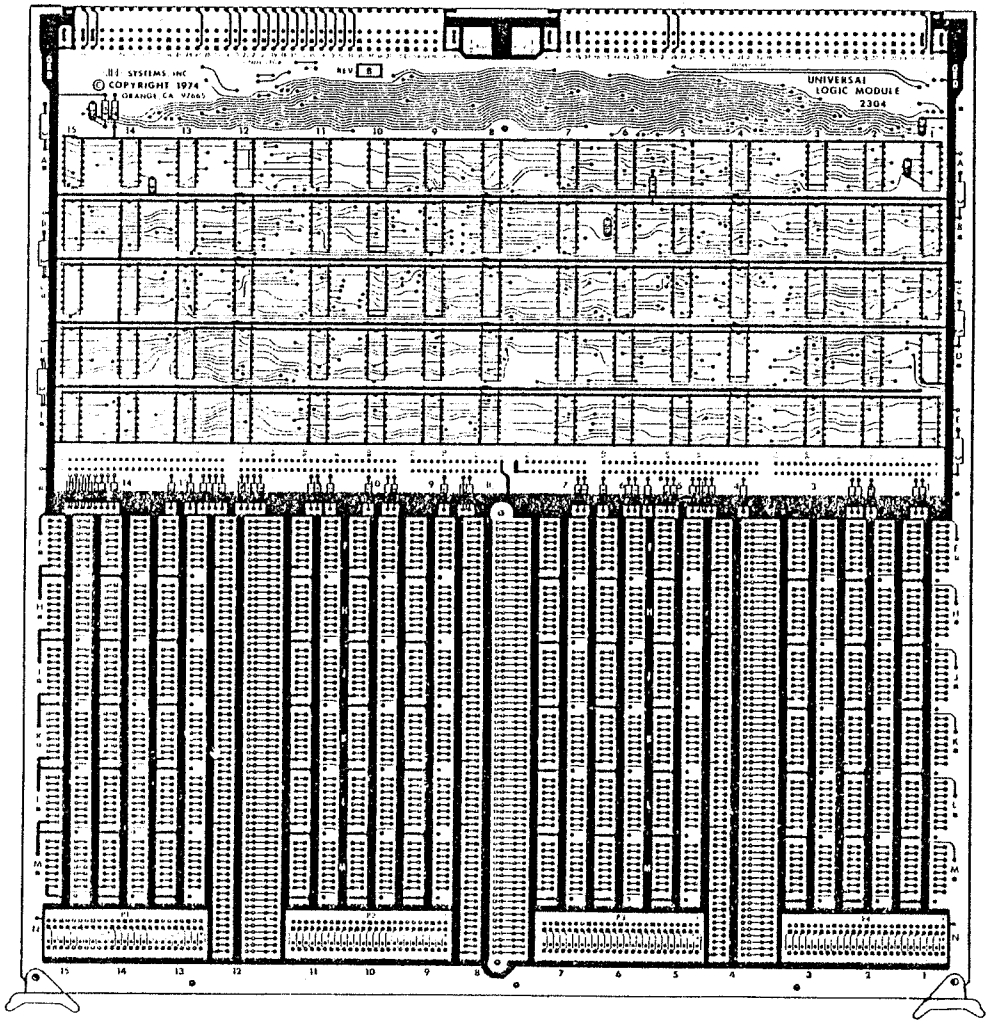
with standard VCC and ground pin assignments. The user may use these locations for 16-pin IC's by removing the etch connecting pin 7 to pin 8. For IC's with non-standard power and ground the user must remove the etch connected to the power and ground plane of these locations. In between the rows of these locations there are provisions to mount ceramic decoupling capacitors on 0.3-inch centers. On both edges of the wirewrap section the user may install tantalum decoupling capacitors on 0.7-inch centers.

Columns 4, 8 and 12 have a hole pattern that is continuous from row F to N on 0.1-inch pin spacing. Mounting centers can accommodate components on 0.3, 0.4 or 0.6-inch centers. These locations have power and ground dedicated for standard 16-pin integrated circuits with pin 8 connected to the ground plane and pin 16 connected to the +5 volt plane. When mounting 22-pin IC's on 0.4-inch centers, or 24 or 40-pin IC's on 0.6-inch centers, the user must remove the etch connecting pin 8 and/or pin 16 to the ground and power plane. When using 14-pin IC's in these locations the user should wirewrap pin 7 to another location's ground pin. Most discrete components are easily mounted in these locations. Sockets or wirewrap pins in the IC locations are optional accessories. Consult MDB price list.

Between the ULM logic and the wirewrap section are two continuous rows of wirewrap pins, row X and Y, that are numbered from 1 to 125. These pins are used to connect the user's logic to the ULM printed circuit logic. Between the I/O connectors "0" and "1" and the ULM logic are wirewrap pins connected to the I/O connectors. The user may use these pins to connect his logic directly to the computer's I/O bus.

In the N row of the wirewrap section are provisions to mount up to four ribbon cable connectors. These locations are designated P1 - P4. They will accommodate MDB standard ribbon cable subassemblies of 20, 26, 34, 40 or 50-pin connectors.

An optional protective cover may be purchased with the ULM. This cover is usually desirable to prevent the user's wirewrap wire from interfering with the module that is mounted directly above the ULM in the chassis.

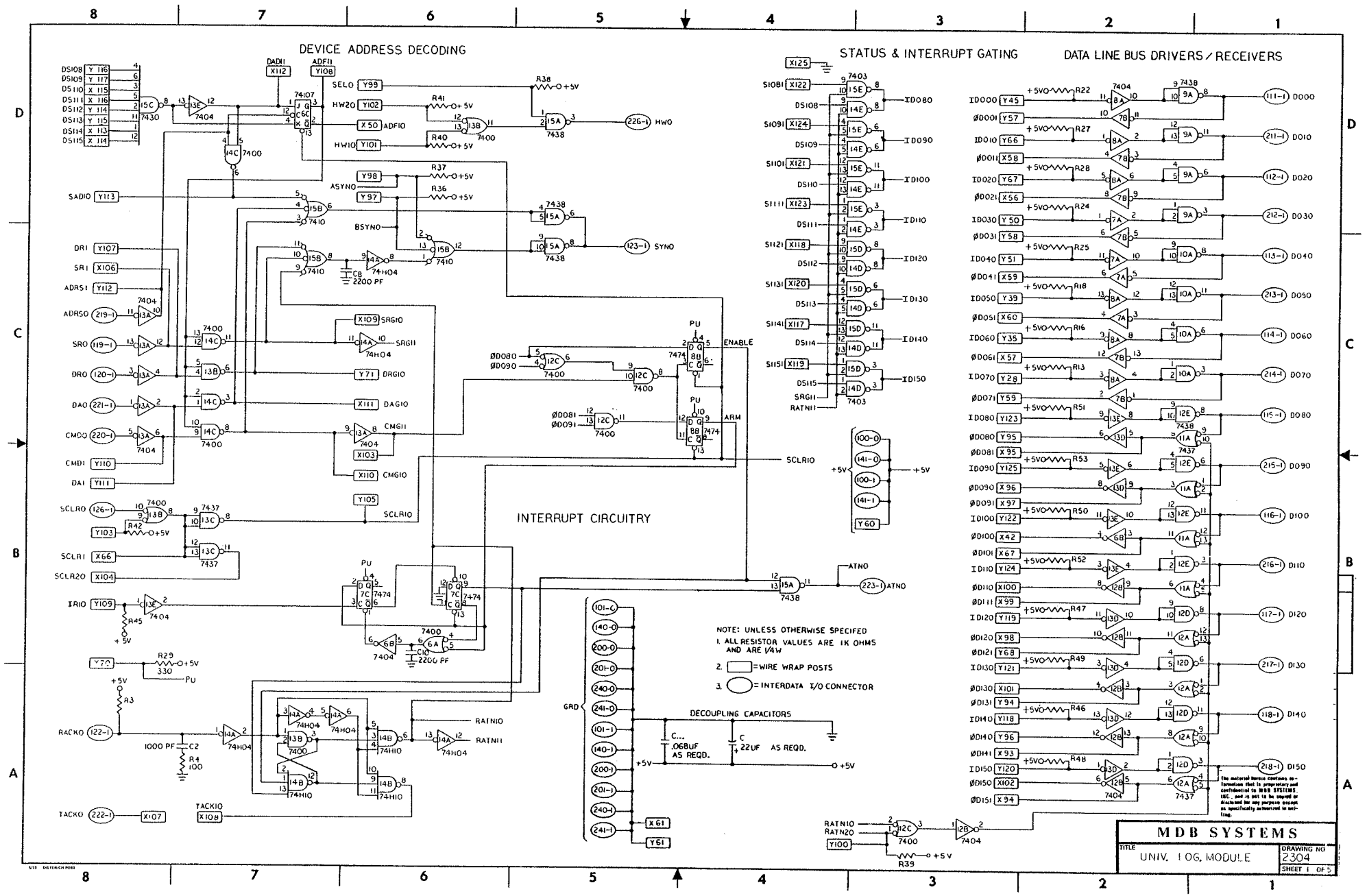


COMP. SIDE

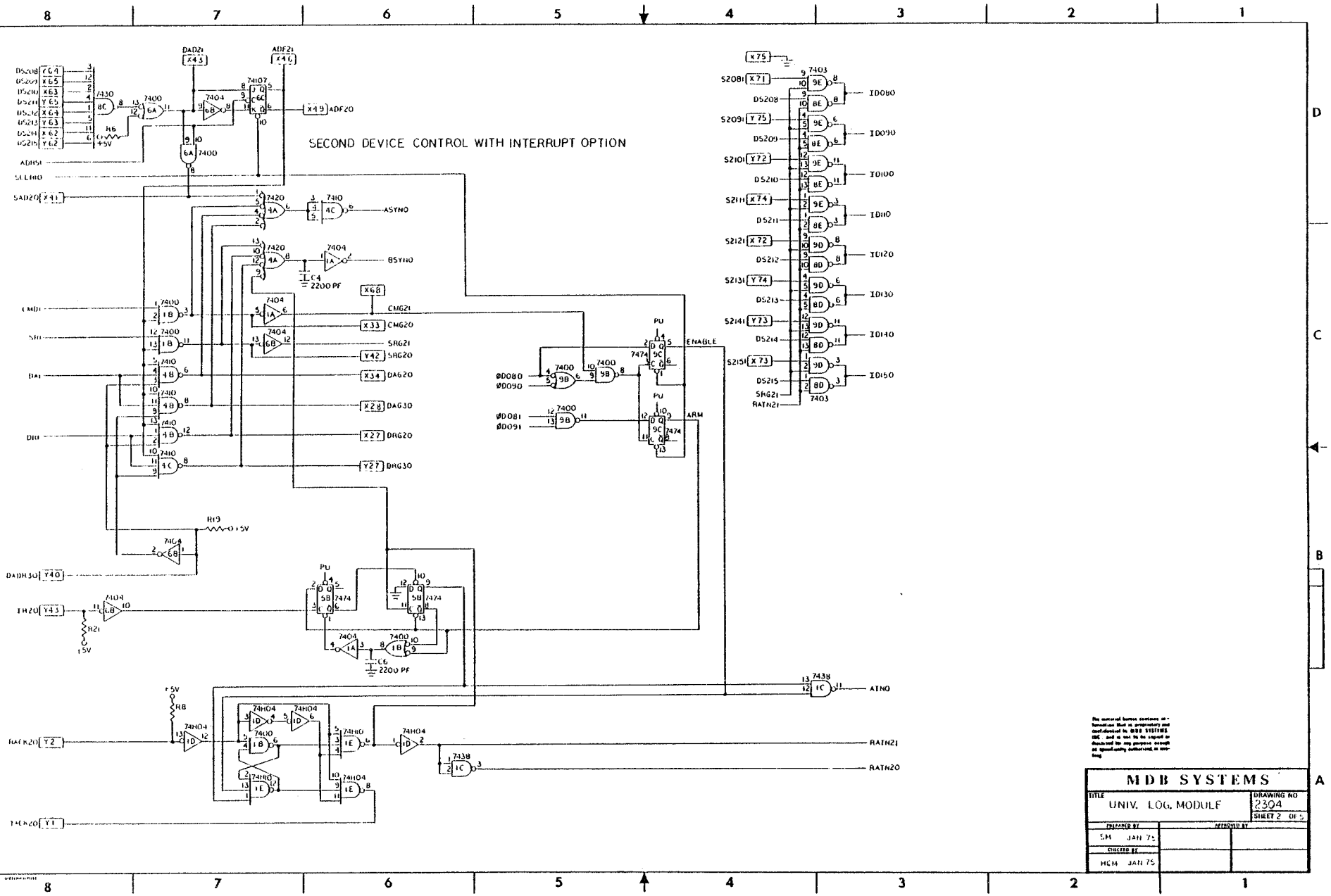
NOTE: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLE PER QUALIFIED MANUFACTURING STANDARDS
2. SQUARE PADS INDICATE POSITIVE SIDE OF CAPACITORS
3. FOR DETAIL SEE DWG. NO. 2304
   FOR SCHEMATICS SEE DWG. NO. 2304

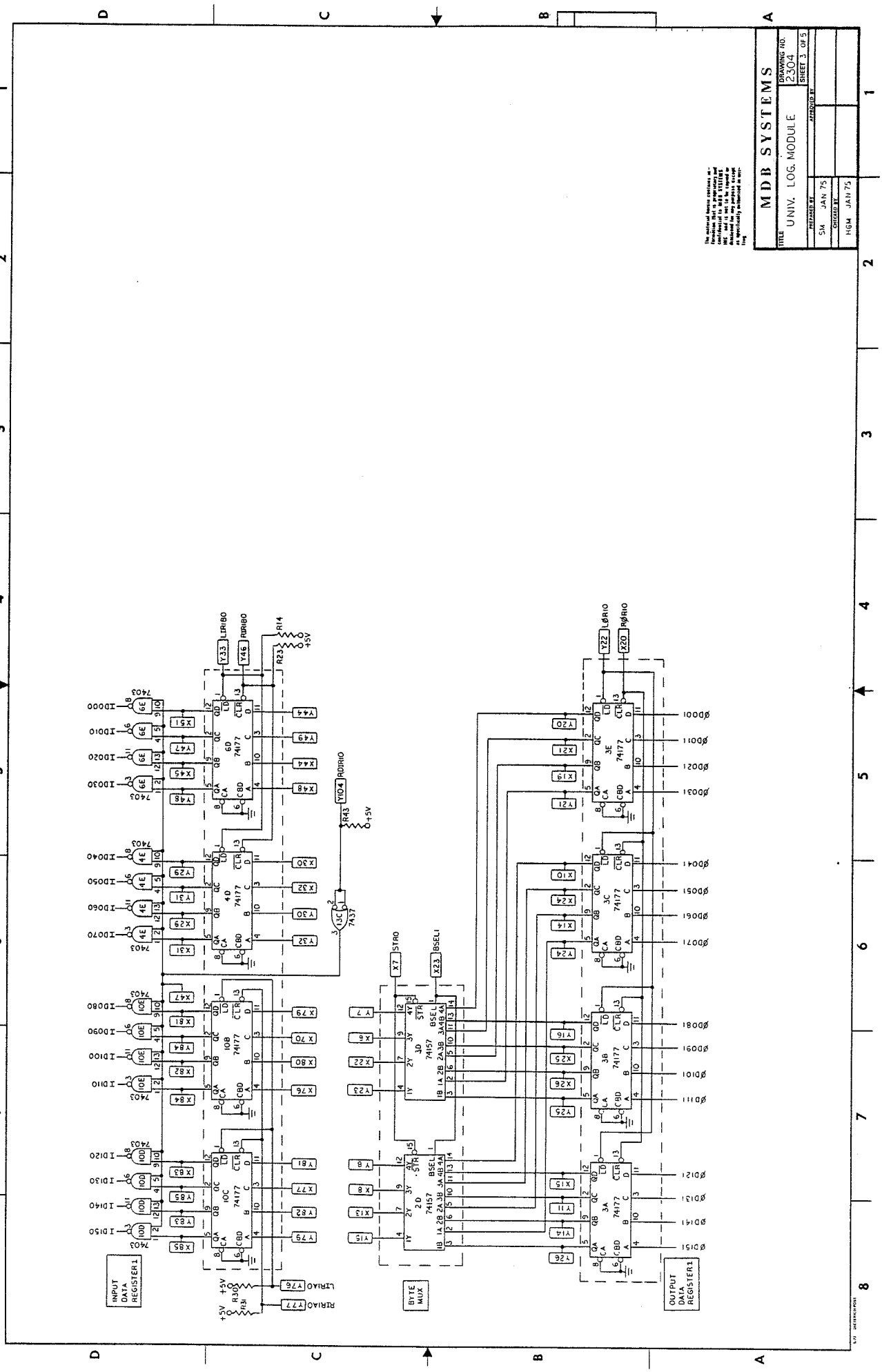
MDB SYSTEMS		
TITLE ASSEMBLY DWG UNIVERSAL LOGIC MODULE		DRAWING NO. 2304 SHEET 1 OF 1
PREPARED BY	APPROVED BY	
SRH OCT 74	REV. B	
CHECKED BY		
HGH OCT 74		
SIZE / CODE IDENT NO.		LTR
SCALE		SHEET OF

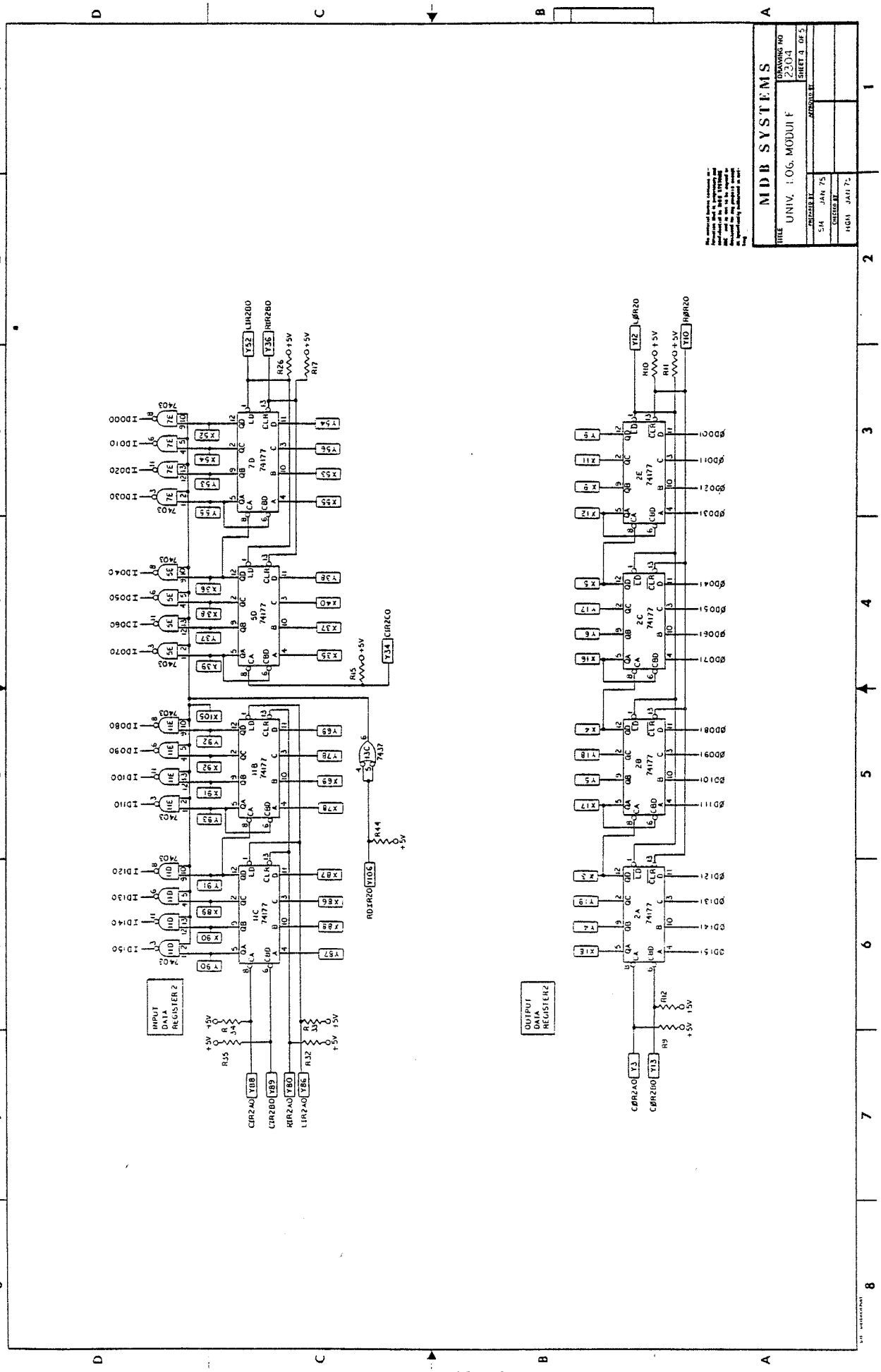

DEVICE ADDRESS DECODING
STATUS & INTERRUPT GATING
DATA LINE BUS DRIVERS / RECEIVERS
INTERRUPT CIRCUITRY
DECOUPLING CAPACITORS
NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE 1K OHMS AND ARE 1/4W
2. = WIRE WRAP POSTS
3. = INTERDATA I/O CONNECTOR
MDB SYSTEMS
UNIV. I.O.G. MODULE
DRAWING NO 2304
SHEET 1 OF 5

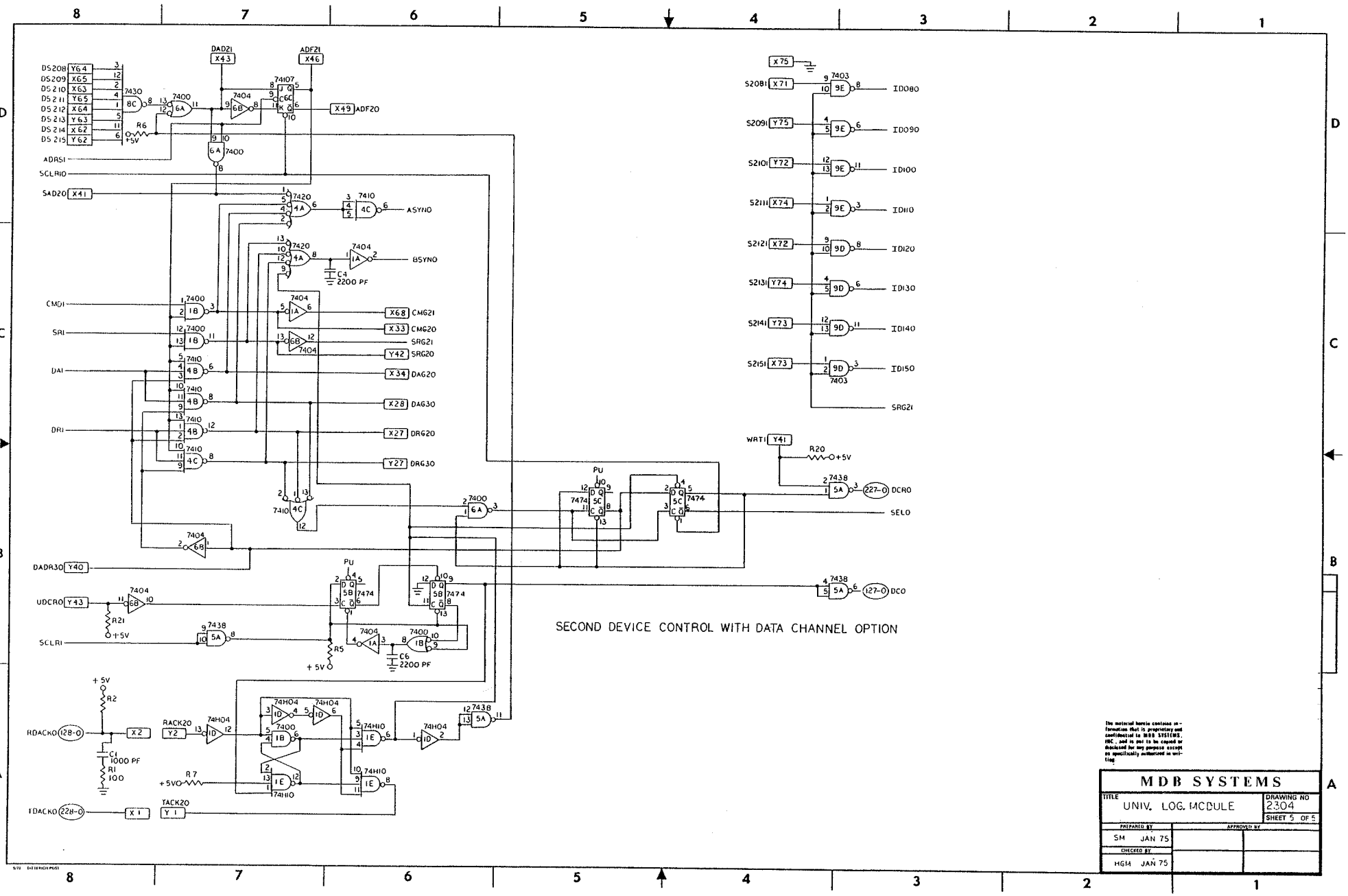
A1-27


SECOND DEVICE CONTROL WITH INTERRUPT OPTION
DAD2I
ADF2I
ADF20
ADH5I
SCLHI0
SAD20
ASYN0
BSYN0
C4 2200 PF
CMD1
SR1
DA1
DI1
CMG2I
CMG20
SRG2I
SRG20
DAG20
DAG30
DRG20
DRG30
R13
DADH30
IH20
R21
C6 2200 PF
R8
BACK20
TACK20
ENABLE
ARM
ATN0
RATN2I
RATN20
ØD080
ØD090
ØD081
ØD091
S2081
S2091
S2101
S2111
S2121
S2131
S2141
S2151
SRG2I
ID080
ID090
ID100
ID110
ID120
ID130
ID140
ID150
MDB SYSTEMS
UNIV. LOG. MODULE
DRAWING NO 2304
SHEET 2 OF 5
SM JAN 75
HGM JAN 75

A1-28


MDB SYSTEMS
TITLE
UNIV. LOG. MODULE
DRAWING NO.
2304
SHEET 3 OF 5
PREPARED BY
SM JAN 75
APPROVED BY
CHECKED BY
HGM JAN 75
INPUT DATA REGISTER1
BYTE MUX
OUTPUT DATA REGISTER1
LRIA0
RRIA0
LRIB0
RRIB0
RDRIO
LDRIO
RDRIO
+5V


MDB SYSTEMS
UNIV. LOG. MODULE
DRAWING NO 2304
SHEET 4 OF 5
INPUT DATA REGISTER 2
OUTPUT DATA REGISTER 2



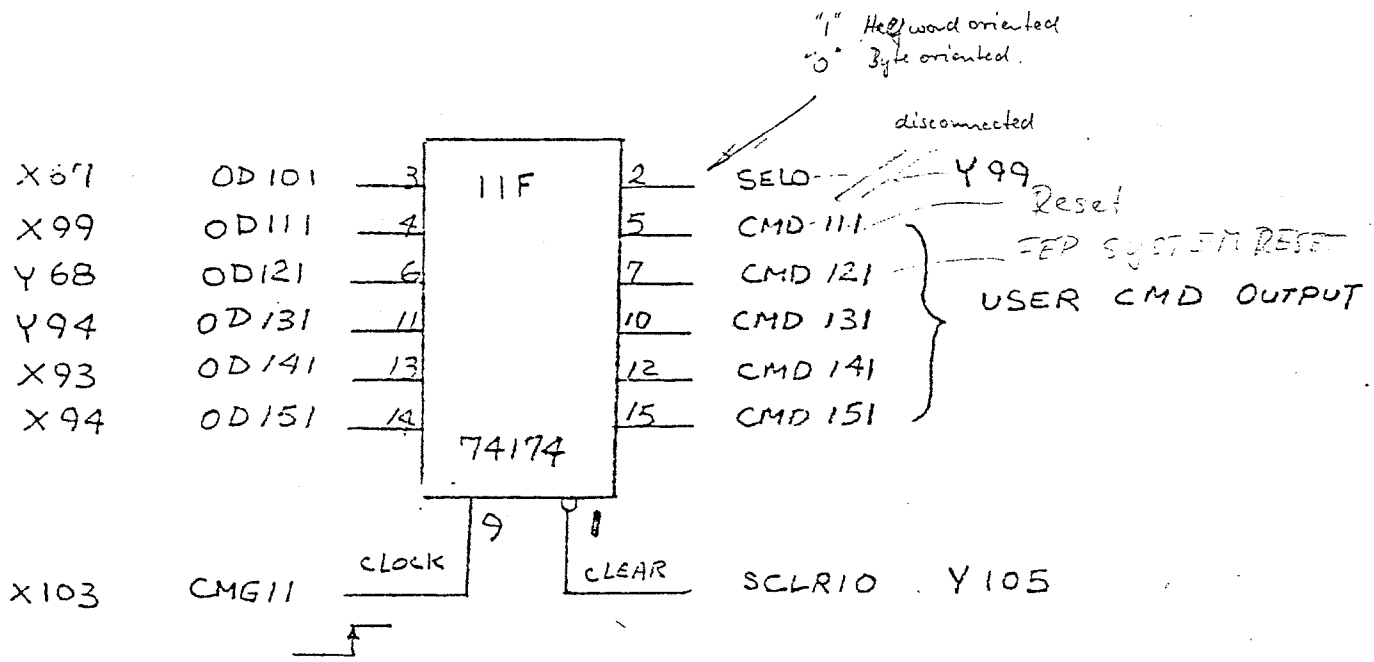
SECOND DEVICE CONTROL WITH DATA CHANNEL OPTION

MDB SYSTEMS

TITLE	DRAWING NO
UNIV. LOG. MODULE	2304
	SHEET 5 OF 5

PREPARED BY	APPROVED BY
SM JAN 75	
CHECKED BY	
HGM JAN 75	

SIZE	APPLICATION		REVISIONS				
A	NEXT ASSY	USED ON	DESCRIPTION	LTR	DR	CHK	APPD



WIRE WRAP X50 TO Y101

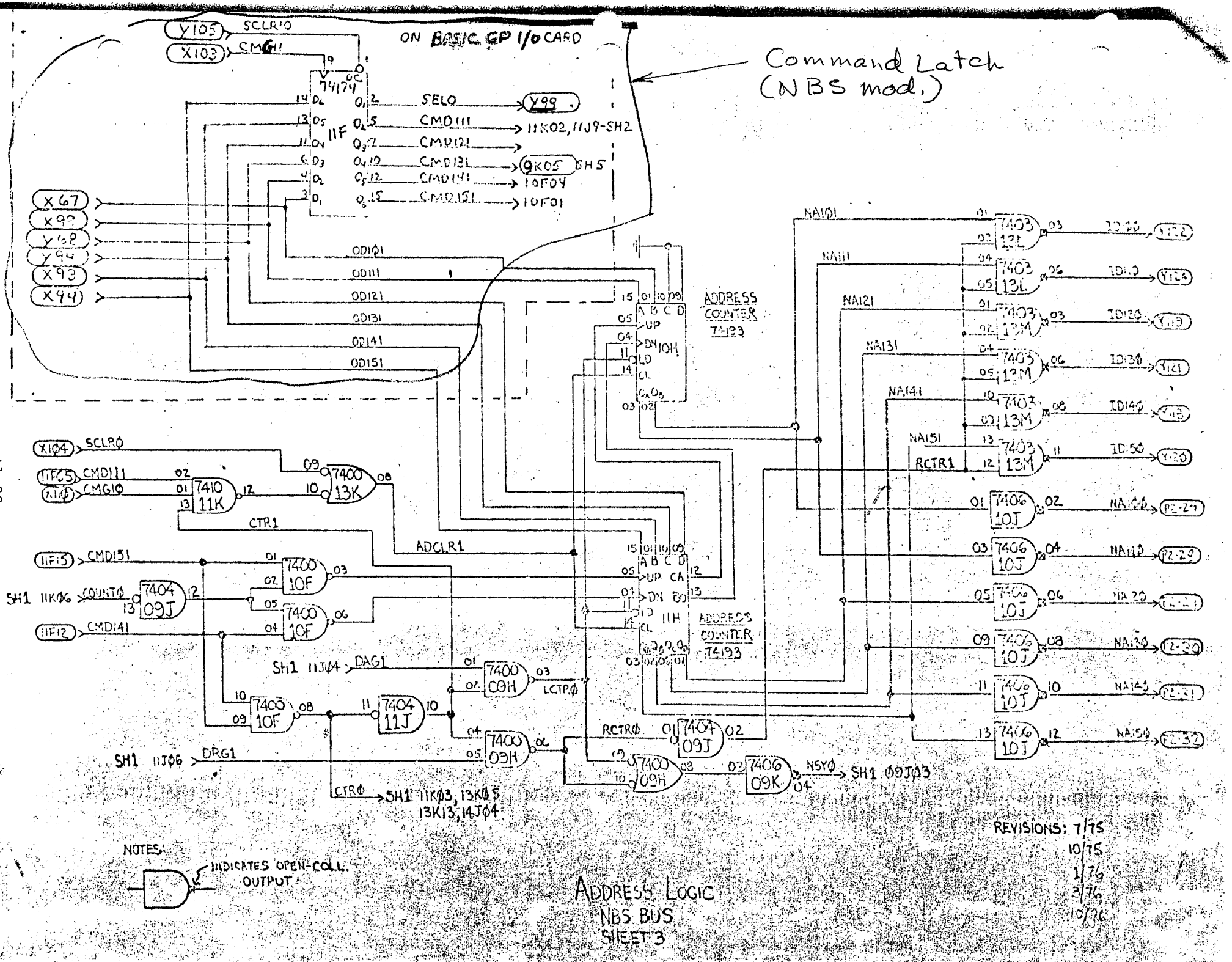
PIN 16 +5 V
PIN 8 GND

CUT ETCH ON IC LOCATION 11F, BETWEEN PIN 7 & 8

OD 8 & OD 9
control interrupt
status

OD 10 - 15
available for user commands
Command validated by CMD 0

MATERIAL	MDB SYSTEMS, INC. ORANGE CA. 92667	TITLE: COMMAND REGISTER ADD TO MDB IULM-16-01	DRAWING NO.
FINISH			SHEET 1 OF 1
SCALE		PREPARED BY: FRED KATO	APPROVED BY
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE		CHECKED BY	
XXX ±.010 / .XX ±.03 / ANGLES ±0° 30'			


ON BASIC GP I/O CARD
Command Latch (NBS mod.)
X105 SCLR10
X103 CMG11
74174
SEL0
CMD111
CMD121
CMD131
CMD141
CMD151
X67
X98
X68
X94
X93
X94
ODI01
ODI11
ODI21
ODI31
ODI41
ODI51
ADDRESS COUNTER 74193
NAI01
NAI11
NAI21
NAI31
NAI41
NAI51
RCTR1
ID:00
ID:10
ID:20
ID:30
ID:40
ID:50
X104 SCLR0
CMD111
CMG10
7410 11K
7400 13K
CTR1
ADCLR1
CMD151
CMD141
7404 09J
7400 10F
SH1 11K06 COUNT0
SH1 11J04 DAG1
7400 C9H
LCTR0
7404 11J
SH1 11J06 DRG1
7400 09H
RCTR0
7404 09J
7406 09K
NSY0
SH1 09J03
CTR0 → SH1 11K03, 13K05, 13K13, 14J04
7406 10J
NA:00
NA:10
NA:20
NA:30
NA:40
NA:50
NOTES:
INDICATES OPEN-COLL. OUTPUT
ADDRESS LOGIC
NBS BUS
SHEET 3
REVISIONS: 7/75
10/75
1/76
3/76
10/76

MDB

MDB SYSTEMS, INC.
1995 N. Batavia St.
Orange, California 92665
714-998-6900
TWX: 910-593-1339

APPENDIX 2

ADDRESS ASSIGNMENTS AS OF AUGUST 19, 1981

ADDRESS	ASSIGNED TO
00	Not to be used.
01	Not assigned.
02	
03	
04	
05	Optional Antenna MUX
06	
07	
08	
09	
0A	
0B	
0C	
0D	
0E	
0F	
10	Receiver
11	
12	
13	
14	
15	
16	
17	
18	
19	
1A	
1B	
1C	
1D	
1E	
1F	Not Assigned

ADDRESS	ASSIGNED TO
20	Not assigned.
21	
22	
23	
24	Timing Sequence Generator
25	
26	
27	Optional Serial Interface
28	
29	
2A	
2B	
2C	
2D	
2E	
2F	
30	Transmitter Controller
31	" "
32	" "
33	Housekeeping-ADC
34	" "
35	Transmitter Controller
36	Front End Processor
37	
38	Not Assigned
39	
3A	
3B	
3C	
3D	
3E	
3F	

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 10 (HEX)

DEVICE: Antenna Multiplexer Module, Channel 1

CONTROL FROM DIO TO DEVICE

BIT		FUNCTION	
0	LSB	A	Antenna Selection
1		B	
2			
3			
4		Local-Remote	
5			
6			
7			

FLAG TO DIO FROM DEVICE

BIT		FUNCTION	
0	LSB	A	Antenna Selection
1		B	
2			
3			
4		Local-Remote	
5			
6			
7			

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 11 (HEX)

DEVICE: Antenna Multiplexer Module, Channel 2

	BIT		FUNCTION	
CONTROL FROM DIO TO DEVICE	0	LSB	A	Antenna Selection
	1		B	
	2			
	3			
	4		Local-Remote	
	5			
	6			
	7			

	BIT		FUNCTION	
FLAG TO DIO FROM DEVICE	0	LSB	A	Antenna Selection
	1		B	
	2			
	3			
	4		Local-Remote	
	5			
	6			
	7			

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 12 (HEX)

DEVICE: Filter Module, Channel 1

	BIT		FUNCTION	
CONTROL FROM DIO TO DEVICE	0	LSB	A	RF Band Selection
	1		B	
	2		C	
	3		D	
	4		Local-Remote	
	5			
	6			
	7			

	BIT		FUNCTION	
FLAG TO DIO FROM DEVICE	0	LSB	A	RF Band Selection
	1		B	
	2		C	
	3		D	
	4		Local-Remote	
	5			
	6			
	7			

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 13 (HEX)

DEVICE: Filter Module, Channel 2

CONTROL FROM DIO TO DEVICE

BIT		FUNCTION	
0	LSB	A	RF Band Selection
1		B	
2		C	
3		D	
4		Local-Remote	
5			
6			
7			

FLAG TO DIO FROM DEVICE

BIT		FUNCTION	
0	LSB	A	RF Band Selection
1		B	
2		C	
3		D	
4		Local-Remote	
5			
6			
7			

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 14 (HEX)

DEVICE: RF Module, Channel 1

CONTROL FROM DIO TO DEVICE

BIT		FUNCTION	
0	LSB	4	RF Attenuation (dB)
1		8	
2		16	
3		32	
4		Local-Remote	
5			
6			
7			

FLAG TO DIO FROM DEVICE

BIT		FUNCTION	
0	LSB	4	RF Attenuation (dB)
1		8	
2		16	
3		32	
4		Local-Remote	
5			
6			
7			

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 15 (HEX)

DEVICE: RF Module, Channel 2

CONTROL FROM DIO TO DEVICE

BIT		FUNCTION	
0	LSB	4	RF Attenuation (dB)
1		8	
2		16	
3		32	
4		Local-Remote	
5			
6			
7			

FLAG TO DIO FROM DEVICE

BIT		FUNCTION	
0	LSB	4	RF Attenuation (dB)
1		8	
2		16	
3		32	
4		Local-Remote	
5			
6			
7			

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 16 (HEX)

DEVICE: IF Module, Channel 1

	BIT		FUNCTION	
CONTROL FROM DIO TO DEVICE	0	LSB	4	IF Attenuation (dB)
	1		8	
	2		16	
	3		32	
	4		Local-Remote	
	5			
	6			
	7			

	BIT		FUNCTION	
FLAG TO DIO FROM DEVICE	0	LSB	4	IF Attenuation (dB)
	1		8	
	2		16	
	3		32	
	4		Local-Remote	
	5			
	6			
	7			

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 17 (HEX)

DEVICE: IF Module, Channel 2

CONTROL FROM DIO TO DEVICE

BIT		FUNCTION	
0	LSB	4	IF Attenuation (dB)
1		8	
2		16	
3		32	
4		Local-Remote	
5			
6			
7			

FLAG TO DIO FROM DEVICE

BIT		FUNCTION	
0	LSB	4	IF Attenuation (dB)
1		8	
2		16	
3		32	
4		Local-Remote	
5			
6			
7			

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 18 (HEX)

DEVICE: Detector Module, Channel 1

	BIT		FUNCTION
CONTROL FROM DIO TO DEVICE	0 LSB	A	Bandwidth Selection
	1	B	
	2		
	3		
	4		Local-Remote
	5		
	6		
	7		

	BIT		FUNCTION
FLAG TO DIO FROM DEVICE	0 LSB	A	Bandwidth Selection
	1	B	
	2		
	3		
	4		Local-Remote
	5		
	6		
	7		

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 19 (HEX)

DEVICE: Detector Module, Channel 2

	BIT		FUNCTION	
CONTROL FROM DIO TO DEVICE	0	LSB	A	Bandwidth Selection
	1		B	
	2			
	3			
	4			Local-Remote
	5			
	6			
	7			

	BIT		FUNCTION	
FLAG TO DIO FROM DEVICE	0	LSB	A	Bandwidth Selection
	1		B	
	2			
	3			
	4			Local-Remote
	5			
	6			
	7			

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 1A (HEX)

DEVICE: Transmitter Drive Module

	BIT		FUNCTION	
CONTROL FROM DIO TO DEVICE	0	LSB	8	Output Attenuation (dB)
	1		16	
	2		32	
	3		64	
	4		Local-Remote	
	5			
	6			
	7			

	BIT		FUNCTION	
FLAG TO DIO FROM DEVICE	0	LSB	8	Output Attenuation (dB)
	1		16	
	2		32	
	3		64	
	4		Local-Remote	
	5			
	6			
	7			

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 1B (HEX)

DEVICE: Control/Adder Module

	BIT		FUNCTION
CONTROL FROM DIO TO DEVICE	0 LSB	1	Synthesizer Frequency Hundreds Hz
	1	2	
	2	4	
	3	8	
	4	1	Synthesizer Frequency Units kHz
	5	2	
	6	4	
	7	8	

	BIT	
FLAG TO DIO FROM DEVICE	0 LSB	
	1	
	2	
	3	
	4	As above
	5	
	6	
	7	

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 1C (HEX)

DEVICE: Control/Adder Module

	BIT		FUNCTION	
CONTROL FROM DIO TO DEVICE	0	LSB	1	Synthesizer Frequency Tens kHz
	1		2	
	2		4	
	3		8	
	4		1	Synthesizer Frequency Hundreds kHz
	5		2	
	6		4	
	7		8	

	BIT		FUNCTION
FLAG TO DIO FROM DEVICE	0	LSB	As above
	1		
	2		
	3		
	4		
	5		
	6		
	7		

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 1D (HEX)

DEVICE: Control/Adder Module

	BIT		FUNCTION	
CONTROL FROM DIO TO DEVICE	0	LSB	1	Synthesizer Frequency Units MHz
	1		2	
	2		4	
	3		8	
	4		1	Synthesizer Frequency Tens MHz
	5		2	
	6		4	
	7		8	

	BIT		FUNCTION
FLAG TO DIO FROM DEVICE	0	LSB	As above
	1		
	2		
	3		
	4		
	5		
	6		
	7		

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 1E (HEX)

DEVICE: Control/Adder Module

	BIT	FUNCTION
CONTROL FROM DIO TO DEVICE	0 LSB	
	1	
	2	
	3	
	4	
	5	
	6	
	7	
FLAG TO DIO FROM DEVICE	0 LSB	Synthesizer Out of Range
	1	Synthesizer Local-Remote
	2	Synthesizer Power Off
	3	
	4	
	5	
	6	
	7	

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 24 (HEX)

DEVICE:

	BIT	FUNCTION
CONTROL FROM DIO TO DEVICE	0 LSB 1 2 3 4 5 6 7 MSB	Data to JOLT PIA 4802 (Parallel Program Load and command byte)
FLAG TO DIO FROM DEVICE	0 LSB 1 2 3 4 5 6 7 MSB	Data to Interdata from JOLT PIA 4800 (Parallel Load Check)

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 25 (HEX)

DEVICE: Timing Sequence Generator

	BIT		FUNCTION
CONTROL FROM DIO TO DEVICE	0	LSB	JOLT Reset
	1		11 Bit Serial EIA Code Input (not now used)
	2		Start Sequence Interrupt
	3		
	4		
	5		
	6		
	7		
FLAG TO DIO FROM DEVICE	0	LSB	EIA Out
	1		Interrupt from JOLT (PIA 4800 data ready)
	2		
	3		Done Interrupt to Interdata
	4		
	5		
	6		
	7		

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 26 (HEX)

DEVICE: Timing Sequence Generator

	BIT	FUNCTION
CONTROL FROM DIO TO DEVICE	0 LSB	Not Used
	1	
	2	
	3	
	4	Request BCD Time (Ident Code)
	5	
	6	
	7 MSB	
FLAG TO DIO FROM DEVICE	0 LSB	BCD Time Data
	1	
	2	
	3 MSB	
	4 LSB	BCD Time Ident Code
	5	
	6	
	7 MSB	

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 30 (HEX)

DEVICE: Transmitter Controller

CONTROL FROM DIO TO DEVICE

BIT	FUNCTION	
0	Filament on	TTL Low Level
1	High Voltage on	TTL Low Level
2	Reset	TTL Low Pulse
3	Set	TTL Low Pulse
4	Antenna Connected (TTL Low Level)	
5		
6		
7		

FLAG TO DIO FROM DEVICE

BIT	FUNCTION	
0	Filament off	Control Setting Indicated By TTL Low
1	High Voltage off	Control Setting Indicated By TTL Low
2	Reset Condition	Control Setting Indicated By TTL Low
3	Set Condition	Control Setting Indicated By TTL Low
4	Dummy Load Connected	Control Setting Indicated By TTL Low
5		
6		
7		

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 31 (HEX)

DEVICE: Transmitter Controller

	BIT		FUNCTION
CONTROL FROM DIO TO DEVICE	0	1	dB Attenuation Inserted by TTL Low
	1	2	
	2	4	
	3	8	
	4	16	
	5		
	6		
	7		
FLAG TO DIO FROM DEVICE	0	1	dB Attenuation Indicated by TTL Low
	1	2	
	2	4	
	3	8	
	4	16	
	5		
	6		
	7		

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 32 (HEX)

DEVICE: Transmitter Controller

	BIT	FUNCTION	
CONTROL FROM DIO TO DEVICE	0		
	1		
	2		
	3		
	4		
	5		
	6		
	7		
FLAG TO DIO FROM DEVICE	0	Filament Off	Condition Indicated by TTL Low
	1	High Voltage Off	
	2	Dummy Load Connected	
	3	High Voltage Dump	
	4	Relay Voltage Reset	
	5	90 Sec HV Delay	
	6	Fault Holdoff	
	7	Relay Voltage Failure	

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 33 (HEX)

DEVICE: Housekeeping Unit

	BIT	FUNCTION
CONTROL FROM DIO TO DEVICE	0 LSB	Channel Address
	1	
	2	
	3	
	4	
	5 MSB	
	6	
	7	
FLAG TO DIO FROM DEVICE	0 LSB	Control of the Selected Channel Address
	1	
	2	
	3	
	4	
	5 MSB	
	6	
	7	

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 34 (HEX)

DEVICE: Housekeeping Unit

	BIT		FUNCTION
CONTROL FROM DIO TO DEVICE	0	LSB	
	1		
	2		
	3		
	4		
	5		
	6		
	7	MSB	
FLAG TO DIO FROM DEVICE	0	LSB	ADC Output
	1		
	2		
	3		
	4		
	5		
	6		
	7		
	8		
	9		
	10		
	11	MSB	

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 35 (HEX)

DEVICE: Transmitter Controller

	BIT	FUNCTION	
CONTROL FROM DIO TO DEVICE	0		
	1		
	2		
	3		
	4		
	5		
	6		
	7		
FLAG TO DIO FROM DEVICE	0	Interlock Fault	Fault Condition or Out-of-Limit Condition Indicated by TTL Low
	1	Ground Fault	
	2	Air Temperature	
	3	Air Pressure	
	4	Peak Current Upper Limit	
	5	Avg. Current Upper Limit	
	6	HV Upper Limit	
	7	HV Lower Limit	

DIO ADDRESSES AND FUNCTIONS

ADDRESS: 36 (HEX)

DEVICE: Front End Processor

	BIT	FUNCTION
CONTROL FROM DIO TO DEVICE	0 LSB	FEP Micro Program Data Bit MDØ
	1	" " " " " MD1
	2	" " " " " MD2
	3	" " " " " MD3
	4	" " " " " MD4
	5	" " " " " MD5
	6	" " " " " MD6
	7	" " " " " MD7

	BIT	
FLAG TO DIO FROM DEVICE	0 LSB	Not Used
	1	
	2	
	3	
	4	
	5	
	6	
	7	

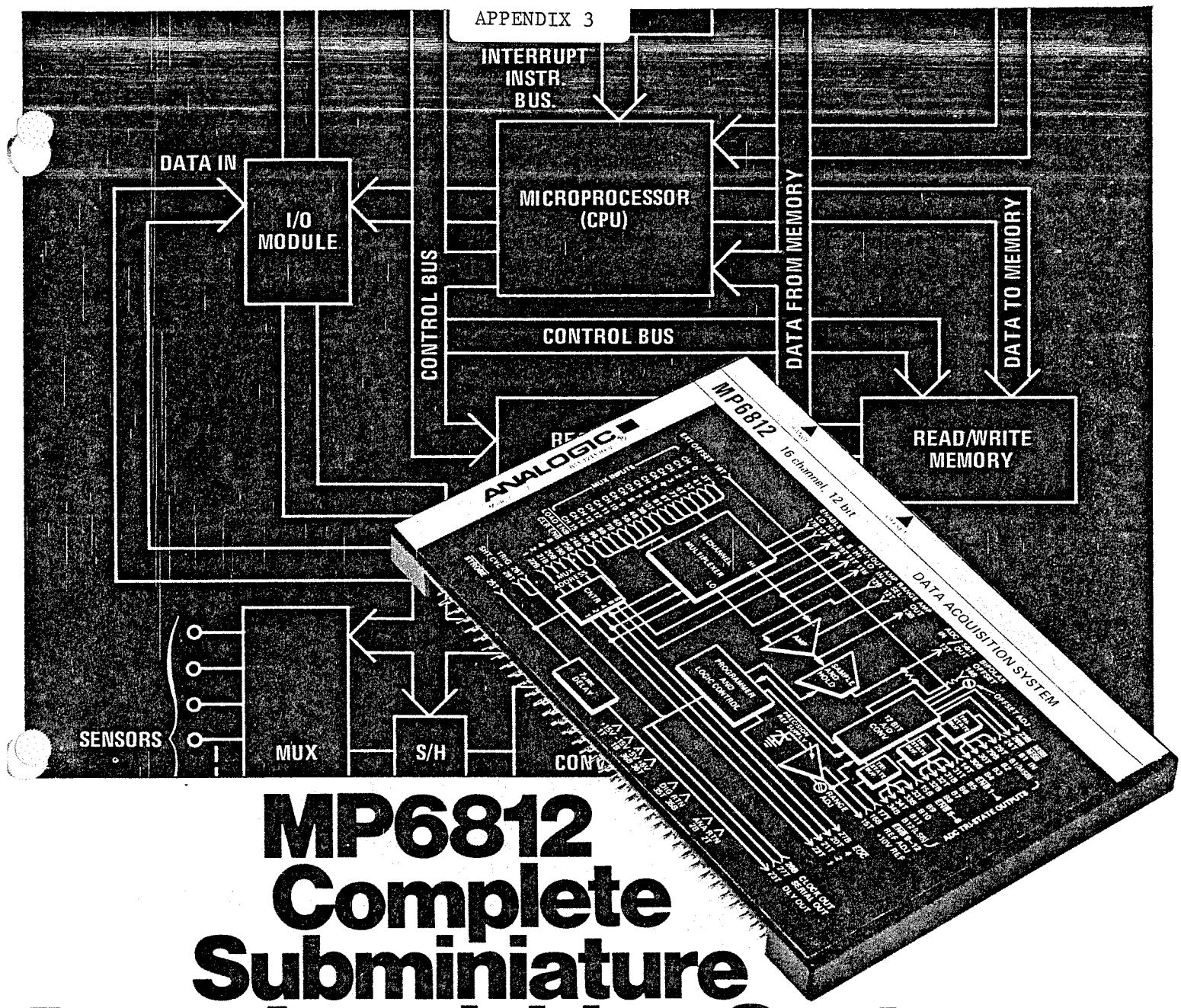
DIO ADDRESSES AND FUNCTIONS

ADDRESS: 37 (HEX)

DEVICE: Front End Processor

	BIT	FUNCTION
CONTROL FROM DIO TO DEVICE	0 LSB	FEP Micro Program Control Bit MCØ
	1	" " " " " MC1
	2	" " " " " MC2
	3	" " " " " MC3
	4	" " " " " MC4
	5	" " " " " MC5
	6	" " " " " MC6
	7	" " " " " MC7

	BIT	
FLAG TO DIO FROM DEVICE	0 LSB	Not Used
	1	
	2	
	3	
	4	
	5	
	6	
	7	



MP6812 Complete Subminiature Data-Acquisition System

FOR LOW-COST

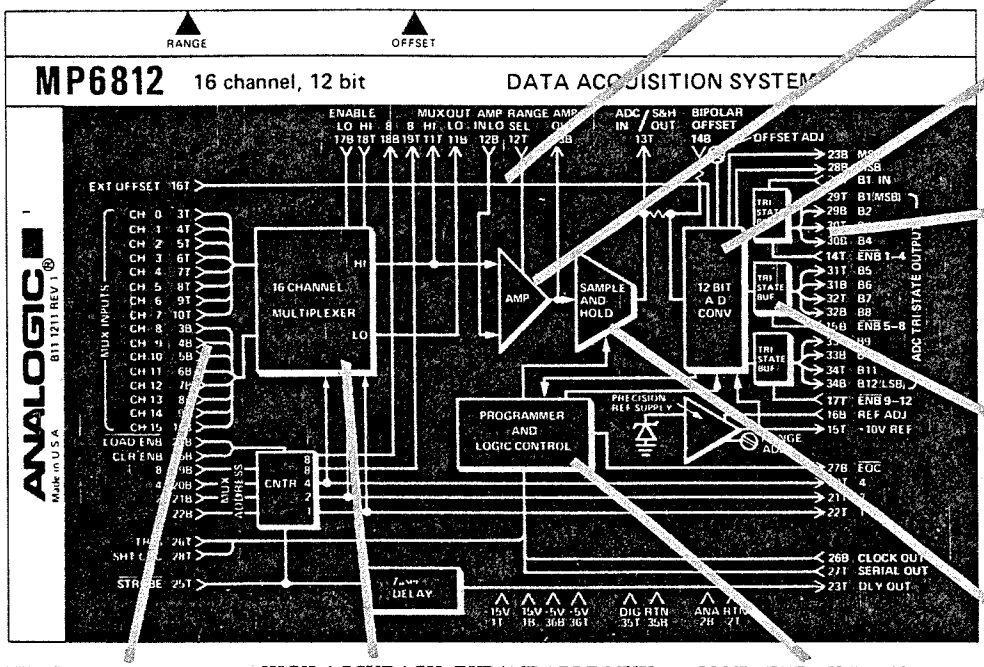
- Stand-Alone Data Acquisition
- Interfacing Minicomputer Systems
- Interfacing Microprocessor-Based Systems
- Automatic Test Equipment (ATE)
- Industrial Digital Controller Systems
- Scientific and Analytical Instrumentation
- Data Communications Systems
- Biomedical and Physiological Data Logging

ANALOGIC®

...The Digitizers

ANOTHER ANALOGIC DESIGN BREAKTHROUGH

Once again, Analogic engineering has anticipated and responded to a critical industry requirement. The new MP6812 satisfies the need for a *very-low-cost, completely self-contained,* high-performance, multichannel A/D conversion system for applications with throughput rates up to 30kHz. These applications range from microprocessor-based and minicomputer-based data acquisition and process control to automatic testing, scientific and analytical instrumentation, telephonic and data communication, telemetry, and biomedical/biophysical measurements. Like the earlier MP6912, the industry's most widely used module in its class, the MP6812 provides maximum flexibility of input/output configurations, ranges, modes, formats, and codes, in subminiature module suitable for mounting on p.c. cards with 0.5″ spacing.



POWER-SUPPLY LEVEL VERSATILITY.
Provides choice of either +5/±15V supplies or ±15V only.

LOW-DISSIPATION, ALL CMOS DESIGN.
All logic circuitry in the MP6812 employs low-power CMOS devices. This adds significantly to reliability, minimizes self-heating drift, and minimizes power drain.

TRUE-DIFFERENTIAL BUFFER.
A standard option, for applications requiring high common-mode rejection.

PREMIUM A/D CONVERTER.
Excellent absolute and relative accuracy, low noise, *very* low T.C.'s. Performance is well within overall system accuracy of 0.025% F.S. up to 30 kHz throughput rate.

VERSATILE OUTPUT FORMAT.
Jumper selection of 3 codes: natural binary, offset binary, or two's complement. Jumper selection of resolution, too, from full 12 bits to any short-cycled word length, for optimum speed/resolution tradeoff.

TRI-STATE OUTPUT BUFFERS.
For full compatibility with microprocessor circuitry, all data interfaces are implemented with tri-state logic, and data outputs are buffered and strobed by BYTE-select inputs.

LOW-APERTURE SAMPLE-HOLD.
Fast acquisition, low-feed-through design, with less than 5ns aperture uncertainty and negligible gain error. Slew and droop characteristics limit maximum *dynamic* error to less than 1 LSB.

VERSATILE INPUT CONFIGURATION.
Accepts 16 single-ended, 16 pseudo-differential, or 8-true differential signal inputs.

HIGH-ACCURACY, EXPANDABLE MUX.
Fast-settling, low-crosstalk, low-noise multiplexer. Negligible gain error. Provides for MUX expansion to 32 differential, 64 single-ended channels. Accommodates random, sequential-continuous, and sequential-triggered modes.

COMPLETE BUILT-IN TIMING AND CONTROL.
No logic to add. No external circuitry required, except for jumpers; all external control by normally available system signals.

ALL REQUIRED CONTROL, TIMING, AND INTERFACE FUNCTIONS ARE BUILT IN.

Unlike many currently available low-cost A/D front-end "systems", which provide *only* the basic building blocks (usually, a MUX, a sample-hold, and an A/D converter), the MP6812 is a *completely integrated subsystem,* in which all of the required control and timing logic has been incorporated into the module – *plus* circuitry that provides for three different analog input configurations, four different ranges, three different output codes, and three different output formats (parallel, byte-serial, and bit-serial). In every sense, the MP6812 is a stand-alone system, requiring only a power supply (such as the Analogic MP3015 or MP3035, depending on the application) for support.

A COMPLETE, HIGH-PERFORMANCE 12-BIT SYSTEM FOR LESS THAN YOUR IN-HOUSE COMPONENT AND LABOR COSTS.

Analogic achieves significant economies due to volume purchasing, long-run production, and computer-programmed testing of data-conversion products like the MP6812 . . . savings that are passed on to you, as witness the low price of the MP6812. In moderate OEM quantities, the price of an MP6812 is actually less than the average user's bare cost of components and labor (excluding engineering, debugging, and test costs). Furthermore, the performance and reliability of the Analogic design, exhaustively verified by comprehensive computer-programmed testing, will usually prove to be superior to an assembled custom system. (See page 11 for test description.)

THEORY OF OPERATION

NOTE: Many of the circuit features mentioned briefly on this page are explained in more detail on pages 4-5, under DESIGN FEATURES.

ARCHITECTURE: The MP6812 comprises the following elements, all self-contained, and all standard (except for the differential buffer amplifier, which is furnished as a standard option, as described on page 7).

- A 16-line multiplexer, which may be used with any one of three signal-source configurations, as described elsewhere on this page. This basic channel capacity is expandable by a compatible accessory (see page 9).
- A high-performance differential buffer amplifier, with two jumper-selectable gains (this feature provides a total of four different full-scale input ranges).
- A high-speed sample-hold circuit, with very low aperture uncertainty (5ns) and many advanced circuit features that increase the overall system accuracy at maximum throughput rates.
- A high-performance 12-bit successive-approximation A/D converter that incorporates a newly developed premium 12-bit IC DAC, a high-stability premium reference zener, and a fast-settling, low-offset, high-stability comparator. The conversion register and conversion-control logic used in this converter provide a wide choice of output codes, and also provide for short-cycling by jumper connection.
- Tri-state output buffers, arranged for digit-serial/bit-parallel, or full-parallel output modes. These buffers will drive output cables or multiple loads, and their tri-state format makes them completely compatible with standard microprocessors.
- A clock-pulse generator providing program-control timing, at a factory-set rate.
- A MUX-address circuit that provides a choice of sequential or random modes, as well as address-output and address-hold signals.
- Provisions for both internal and external trimming of both range and offset . . . and facilities for remote adjustment or sequence configuration of the programming and control functions, as described on later pages.

INPUT CONFIGURATIONS. The MP6812 provides a choice of 3 input configurations, as shown in figure 1. In the simplest, 16 single-ended inputs may be connected to the multiplexer, all referenced to ANALOG GND. Alternatively, the inputs may be presented, in 8 pairs, to the differential amplifier (optional), merely by connecting MUX OUT LO terminal to the AMP IN LO terminal as shown in 1b. Finally, 16 "pseudo-differential" channels may be created, under favorable sensor-ground-path conditions, by using the AMP IN LO terminal as the ground-return point for all 16 sensors.

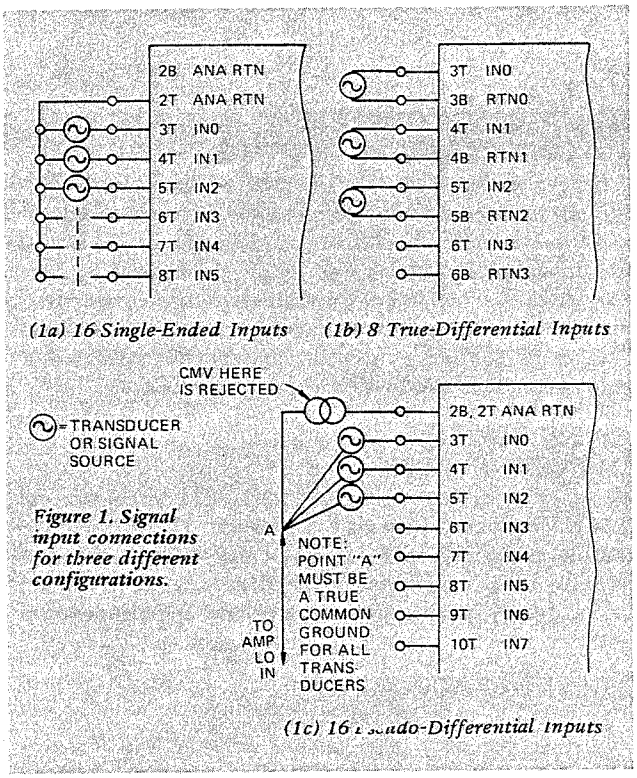


Figure 1. Signal input connections for three different configurations.

CONTROL/TIMING.

The simplified timing diagram of figure 2, below, shows the time constraints and sequence of events in the random-addressed mode. Note that 7μsec (t_{01}) is assigned to the overall settling time of the MUX, buffer amplifier, and sample-hold acquisition, and another 28μsec is allowed for a complete 12-bit conversion (B1 to B12). The diagrams on page 7 are more detailed, and describe the behavior of every control, address, output, and analog element in the data path.

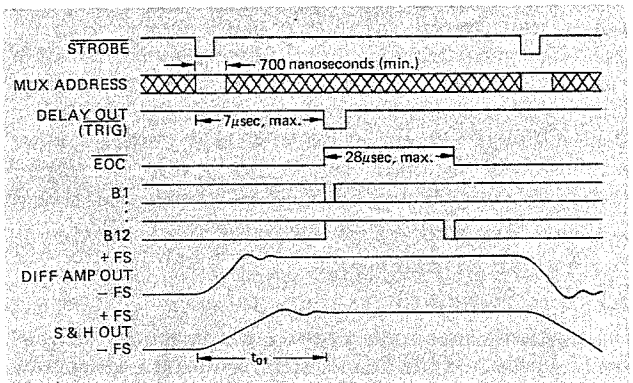


Figure 2. Simplified timing diagram, showing time-interval assignments and constants.

DESIGN FEATURES

- **LOWEST-COST COMPLETE MICROPROCESSOR INTERFACE.**

We believe the MP6812 to be the lowest-cost modular interface system that provides *complete* microcomputer-compatible interface circuitry, including all required timing and control logic. Although other low-priced modules have been offered as "complete", examination of their specifications immediately reveals the need for significant amounts of external circuitry . . . . with consequent increases in direct and indirect production and engineering costs.

- **LOWEST-POWER COMPLETE SYSTEM.**

Due to the extensive use of CMOS/LSI circuitry, the MP6812 dissipates less than 1.5 Watts. Considering the available convection surface area of the MP6812, this corresponds to a maximum temperature rise of less than 8° C . . . greatly enhancing both reliability and temperature stability.

- **EXCELLENT ACCURACY, LINEARITY, AND STABILITY.**

Despite its low price, the MP6812 provides the accuracy and linearity of A/D interfaces costing 3-5 times as much; and its time and temperature stabilities compare favorably with premium-grade A/D converters. At the full 30kHz throughput rate, the relative and absolute accuracies are ±0.025% FS – i.e., ±1LSB! The T.C.'s range from 3 to 20 PPM/° C, which allows operation over wide temperature ranges without serious degradation of accuracy. (See detailed specifications, page 6.)

- **FASTER THROUGHPUT THAN REQUIRED BY MOST APPLICATIONS.**

Most microprocessors have operation-cycle times ranging from 2.5 to 12.5 microseconds, and the software routines used in most microcomputers typically require 6 to 20 operations per data input word. Corresponding minimum rates for data throughput from the interface module range from 4 kHz to about 65 kHz, with the average well below 20 kHz. The 30 kHz rate of the MP6812 is, therefore, more than adequate for most applications. (Note that higher throughput rates are possible at lower resolution, as shown in figure 3, by "short-cycling" the converter.)

- **TRI-STATE BUFFERED DATA INTERFACE.**

The standard data-output interface is a strobeable array of three four-bit Tri-State data registers, compatible with CMOS logic levels and capable of driving 2 TTL loads. Optionally (see page 7), the MP6812 can be furnished with Tri-State TTL output registers, in the same format, that are capable of driving 10 TTL loads for fast, long-lines drive capability. (The standard CMOS circuit will accommodate approximately 100pF of capacitance loading without significant effect on the data-throughput rate.)

- **EXCELLENT MUX AND SAMPLE-HOLD DYNAMICS.**

The total of MUX settling time and Sample-Hold Acquisition time in the MP6812 is about 7μsec, during which the maximum error (for a worst-case FS-to-FS transition between successively addressed channels) falls to less than 1 LSB. An internal fixed delay of 7μsec is provided, to inhibit the HOLD command for that interval, thereby eliminating dynamic error as an accuracy factor (see figure 4). Alternatively, the user may apply whole commands derived from his own system timing. The aperture uncertainty is less than 5ns . . . negligible, even for fast rates of change of signal. Droop is negligible for the 28μsec (max.) conversion time.

- **GREATEST INPUT-CIRCUIT VERSATILITY.**

As explained on page 3, the MP6812 can accommodate almost any input-source configuration. With the differential

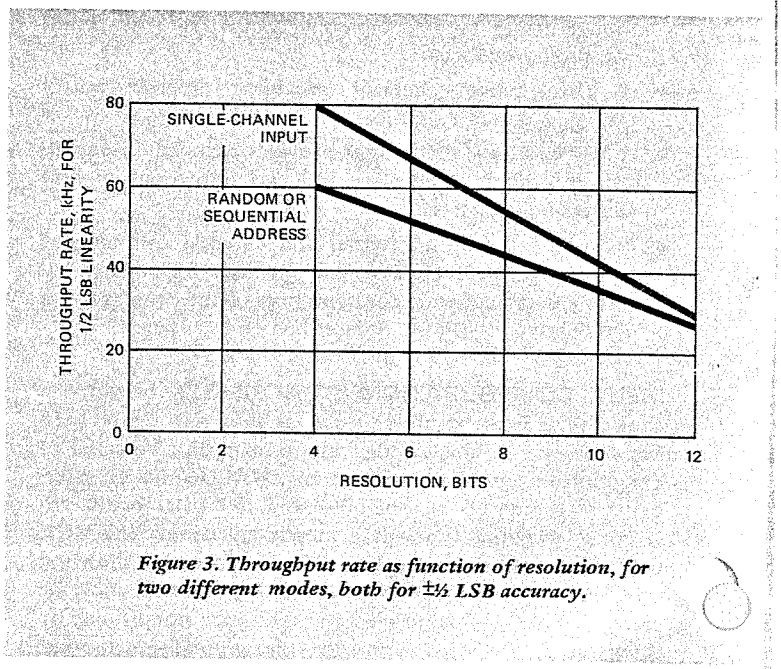


Figure 3. Throughput rate as function of resolution, for two different modes, both for ±½ LSB accuracy.

amplifier option, using 8 true-differential channels, excellent CMRR and common-mode-noise rejection is provided. In non-critical, low-noise situations, where ground loops are not a problem, the 16-channel single-ended capability may be used. Finally, for applications in which a true common ground exists near the signal sources, but remote from the MP6812, the intermediate choice of a pseudo-random, 16-channel interface is also available.

• LOW-COST, CONVENIENT MUX EXPANSION.

As discussed in detail on page 9, the channel capacity of the MP6812 can be expanded up to a total of 64 single-ended or pseudo-differential channels (32 differential), by adding a standard outboard module. All of the necessary interconnections are provided for in the MP6812, by bringing the pertinent circuit connections to terminals. The 7μsec built-in delay allows for the full capacitance loading of a 64-channel, expanded multiplexer.

• THREE OUTPUT FORMATS – PARALLEL, BYTE-SERIAL, SERIAL.

The 12-bit output of the MP6812 is available in three output formats: as a serial pulse train (clock synchronized), MSB first; as a full parallel 12-bit output, enabled by strobing the 3 byte-control lines simultaneously; and as a byte-serial output, in three 4-bit bytes, by sequentially strobing the 3 byte-control lines. The serial output is always available, regardless of the use of the parallel or byte-serial outputs. (See page 6.)

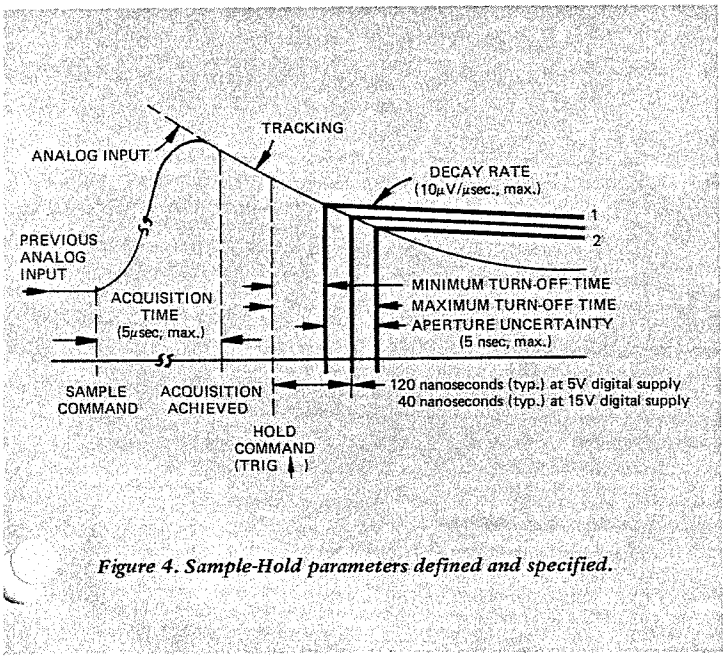


Figure 4. Sample-Hold parameters defined and specified.

• PREMIUM-GRADE 12-BIT A/D CONVERTER.

The A/D converter used in the MP6812 has, as described on page 3, exceptional accuracy, linearity, and stability. It preserves high-accuracy over wide ranges of temperature and power-supply voltage, and over long periods of time (6-month recalibration interval). The total 3-sigma noise (referred to input) including reference noise is less than 0.01% FSR. A typical worst-case limit-of-error calculation for this converter, over ±10°C and ±3% power-supply voltage, at full scale, predicts less than .025% uncertainty . . . an order of magntiude better than most off-the-shelf systems can attain.

• OUTPUT CODE AND RANGE FLEXIBILITY.

The standard MP6812 provides three pin-selectable codes: natural binary, two's complement, and offset binary. The output ranges available on the standard design are: −10V to +10V, 0V to +10V, −5V to +5V, and 0 to +5V. Optionally (see page 7), the reference may be factory adjusted to provide endpoints at 10.24V and 5.12V for convenient volts/bit values. (For example, with a 0V to +10.24V range, each LSB = 2.5mV, exactly.)

• EXCELLENT ENVIRONMENTAL IMMUNITY

The MP6812 is designed for long, trouble-free life under realistic industrial conditions – operating temperatures from 0°C to 70°C (storage, −25°C to +85°C), relative humidity from 0 to 95% non-condensing, moderate shock and vibration, and strong electromagnetic and/or electrostatic fields (see below). The power supply regulation is not at all critical . . . ±3% on the ±15V supplies, and ±5% on the 5V logic supply. As noted earlier, the low temperature rise significantly enhances reliability.

• SUBMINIATURE, SELF-SHIELDED, REPAIRABLE PACKAGE.

The MP6812 is enclosed in an insulated steel case measuring only 3" x 4.6" x 0.375" . . . a low enough profile to permit its mounting on a p.c. board having 0.5" spacing to adjacent boards. The case forms a continuous 6-sided shield, except for the slots provided to accommodate the connector. The case cover is easily removed for inspection, modification, or component replacement, if that should ever be necessary. U. S. Patent No. 3,895,267 issued for modular construction of MP6812 and associated modules.

SPECIFICATIONS

ANALOG INPUTS

Number of Inputs to Multiplexer	16 Single-Ended, 8 True-Differential, or 16 Pseudo-Differential
Input Voltage (Full Scale Range)	−10V to +10V, 0V to +10V, −5V to +5V, 0V to +5V. (Optionally, −10.24V to +10.24V, −5.12V to +5.12V, 0V to +5.12V)
Maximum Input Voltage for Proper Operation (signal plus common mode)	−10.24V or +10.24V
Input Current (per channel)	1nA @ 25°C typ.; 40nA @ 70°C
Input Impedance	> 100 Megohms
Input Capacitance	< 10pF for "off" channel; < 100pF for "on" channel
Input Fault Current (power off or MUX failure)	Internally limited to 20mA

ACCURACY

Resolution	12 bits
Relative Accuracy	±0.025% FSR @ 30kHz thru-put rate (includes 5μsec (ext. timing) for MUX settling and S & H acquisition time and 28μsec for A/D conversion time).
Absolute Accuracy	Same as relative accuracy.
Inherent Quantizing Error	±½ LSB
3-sigma Noise (includes reference noise)	0.01% FSR p-p referred to input.
Monotonicity	Guaranteed, 0°C to 70°C

STABILITY

Tempco of Linearity	< 3 PPM FSR/°C
Tempco of Gain	< 15 PPM FSR/°C
Tempco of Offset	< 10 PPM FSR/°C
Power Supply Sensitivity	0.003% FSR/% change in supply voltage.
Recommended Recalibration Interval	6 months

SIGNAL DYNAMICS

Maximum Throughput Rate (12 bits)	30,000 channels/sec single-channel, using external 5μsec delay (includes 5μsec for MUX settling time and S & H acquisition time, and 28μsec for A/D conversion time. Utilizing internal 7μsec delay, multichannel thruput is 27.5kHz.
Sample and Hold Aperture Uncertainty	5 nsec
Crosstalk	80dB down at 1 kHz "off" channels to "on" channel.
Optional Differential Amplifier CMRR	> 70 dB (DC to 1 kHz)
Sample and Hold Feedthrough	80 dB down at 1 kHz
Maximum Error for F.S. to F.S. transition between successively addressed channels	1 LSB

DIGITAL INPUT SIGNALS (See Timing Diagram)

Compatibility	Standard CMOS logic levels, TTL optional. 1 CMOS unit load/line.
MUX Address Inputs (8, 4, 2, 1; Pins 19B thru 22B)	Positive true natural binary coding selects channel for random addressing mode.
MUX ENABLE HI (Pin 18T)	High (logic "1") input enables MUX "HI" output (for inputs 0 thru 7)
MUX ENABLE LO (Pin 17B)	High (logic "1" input enables MUX "LO" output (for inputs 8 thru 15)
$\overline{\text{LOAD ENABLE}}$ (Pin 24B)	High (logic "1") input allows next STROBE command to sequentially advance MUX address register. Low (logic "0") input updates MUX address register according to external address inputs at next STROBE command, and disables counting.
$\overline{\text{CLEAR}}$ (Pin 25B)	Low (logic "0") input resets MUX address to channel "0" overriding LOAD ENABLE.
TRIGGER (Pin 26T)	Negative going transition (logic "1" to logic "0") initiates sample and hold transition to hold state and A/D conversion.
BYTE (N) SELECT Pins 14T, 15B, 17T	Low (logic "0") causes bits within BYTE (N) to be presented at outputs; High (logic "1") causes bits of BYTE (N) to be disconnected.
STROBE	Negative going transition (logic "1" to logic "0") generates delay out pulse after 7μsec max. delay.

DIGITAL OUTPUT SIGNALS (See Timing Diagram)

Compatibility	Standard CMOS logic levels, 2 Low Power TTL Loads.
Parallel Outputs (buffered)	$\overline{\text{B1}}$, B1 thru B12
Coding	Natural binary, two's complement, offset binary, Pin selectable.
Outputs	B1 thru B12 tri-state outputs steered by BYTE (N) SELECT inputs.
Serial Output	NRZ format, binary or offset-binary coding, positive true (see Timing Diagram).
MUX Address Outputs 8, 4, 2, 1; pins 18B, 19T (thru 22T)	Positive true natural binary coding indicates channel selected.
$\overline{\text{EOC}}$ (Pin 27B)	High (logic "1") output during A/D conversion.
DELAY OUT	Negative going pulse generated by strobe pulse after 7μsec max. delay.

ADJUSTMENTS

Offset Adjust	Externally accessible internal adjustment or remote external adjustment calibrates zero offset. Use with RANGE ADJ to calibrate absolute accuracy.
Range Adjust	Externally accessible internal adjustment or remote external adjustment calibrated range. Use with OFFSET ADJ to calibrate absolute accuracy.

CONTROLS

Short Cycle (Pin 28T)	When open, the unit operates with a full twelve bits resolution. When BYTE (N) SELECT inputs are all low and the SHORT CYCLE input is connected to bit N, the unit will operate with N −1 bits resolution.
Channel Selection Mode (MUX) Address Loading Mode)	Random, sequential continuous, and sequential triggered.

POWER REQUIREMENTS

Two power-supply facilities may be used. In one, both ±15V and +5V, supplies are used; in the other, the +5V input is connected to +15V, the digital and analog returns are connected together, and only two voltages are required.

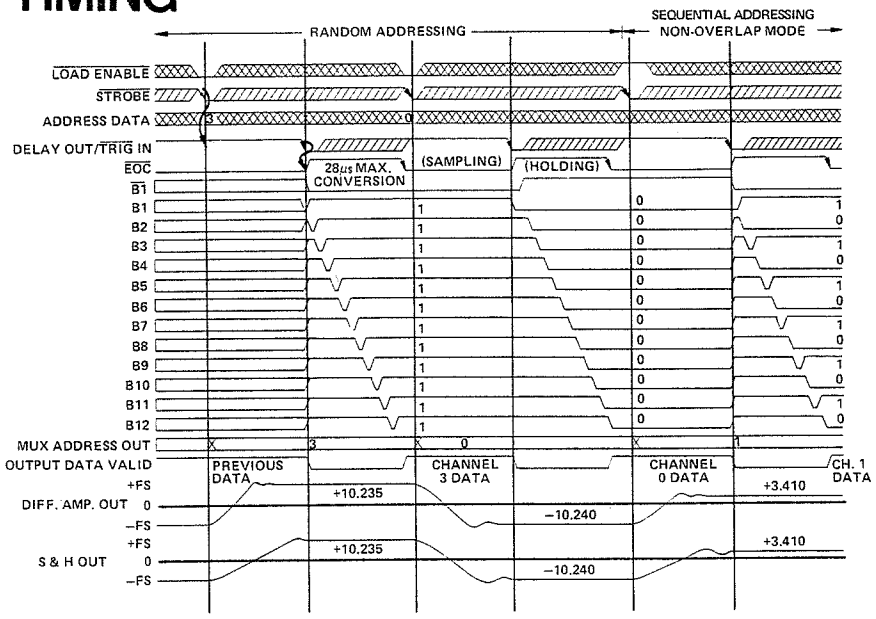
+15V ±3% @ 45 mA −15V ±3% @ 45 mA +5V ±5% @ 25 mA	OR	+15V ±3% @ 85 mA −15V ±3% @ 45 mA

ENVIRONMENTAL & PHYSICAL

Operating Temperature	0° C to 70° C
Storage Temperature	−25° C to +85° C
Relative Humidity	Up to 95% non-condensing
Electrical Shielding	RFI & EMI 6 sides (except connector area)
Packaging	Insulated steel case 3.00 x 4.6 x 0.375 inches.

Analogic may upgrade these specifications at any time.

TIMING



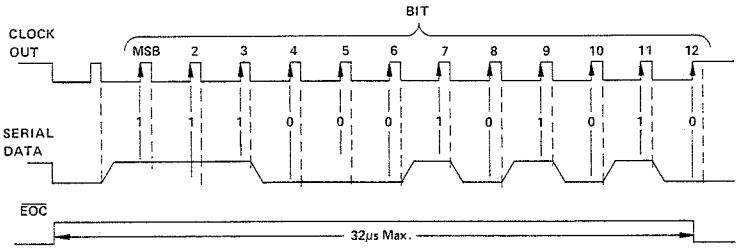
SIGNAL CONDITIONS AND STATUS KEYS FOR FIGURES 1 AND 2.

CH. 2 = –3.415V. CODE 010 101 010 101
CH. 3 = +10.235V. CODE 111 111 111 111
CH. 0 = –10.240V. CODE 000 000 000 000
CH. 1 = +3.410V. CODE 101 010 101 010

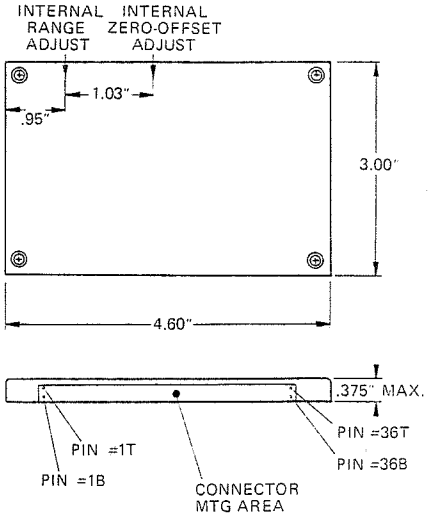
ADC SET UP FOR ±10.24V. INPUT, OFFSET BINARY. (FOR TWO'S COMPLEMENT, USE $\overline{B1}$ FOR M.S.B.)

KEY	INPUTS	OUTPUTS
XXX	MAY CHANGE	DON'T KNOW
///	MAY CHANGE 0 TO 1	CHANGES 0 TO 1
\\\	MAY CHANGE 1 to 0	CHANGES 1 TO 0
OR	MUST BE STABLE	WILL BE STABLE

SERIAL DATA OUTPUT TIMING



DIMENSIONS



BASIC MODULE CONFIGURATION

TERMINATIONS

Table 1 – MP6812 Connector Pin Diagram

+15V	1T	1B	–15V
ANA RTN	2T	2B	ANA RTN
CH 0 IN	3T	3B	CH 8 IN (CH 0 RTN)
CH 1 IN	4T	4B	CH 9 IN (CH 1 RTN)
CH 2 IN	5T	5B	CH 10 IN (CH 2 RTN)
CH 3 IN	6T	6B	CH 11 IN (CH 3 RTN)
CH 4 IN	7T	7B	CH 12 IN (CH 4 RTN)
CH 5 IN	8T	8B	CH 13 IN (CH 5 RTN)
CH 6 IN	9T	9B	CH 14 IN (CH 6 RTN)
CH 7 IN	10T	10B	CH 15 IN (CH 7 RNT)
MUX HI OUT	11T	11B	MUX LO OUT
RANGE SEL	12T	12B	AMP IN LO
S & H OUT (ADC IN1)	13T	13B	AMP OUT
$\overline{ENB}$ 1-4	14T	14B	BIPOLAR OFFSET ADC IN 2
+10V REF	15T	15B	$\overline{ENB}$ 5-8
EXT OFFSET	16T	16B	REF ADJ
$\overline{ENB}$ 9-12	17T	17B	ENABLE LO
ENABLE HI	18T	18B	$\overline{8}$ OUT
8 OUT	19T	19B	8 IN
4 OUT (MUX LINES)	20T	20B	4 IN (MUX ADDRESS LINES)
2 OUT (MUX LINES)	21T	21B	2 IN (MUX ADDRESS LINES)
1 OUT	22T	22B	1 IN
DLY OUT	23T	23B	MSB OUT (UNBUFFERED)
BIT 1 IN	24T	24B	LOAD ENB
$\overline{STROBE}$	25T	25B	CLK ENB
TRIG	26T	26B	CLOCK OUT
SERIAL OUT	27T	27B	$\overline{EOC}$
SHT CYC	28T	28B	MSB (UNBUFFERED)
B1 OUT	29T	29B	B2 OUT
B3 OUT	30T	30B	B4 OUT
B5 OUT	31T	31B	B6 OUT
B7 OUT	32T	32B	B8 OUT
B9 OUT	33T	33B	B10 OUT
B11 OUT	34T	34B	B12 (LSB) OUT
DIG RTN	35T	35B	DIG RTN
+5V	36T	36B	+5V

NOTES ON TIMING. As noted earlier, the MP6812 has a built-in 7μsec delay, to allow inhibition of the start of conversion (after MUX-address loading) until the MUX and Sample-Hold have settled to the rated accuracy. This delay may be introduced into both the free-running mode or the externally triggered mode, and is operative both for externally programmed random or sequential addressing and internally programmed sequential addressing. Note that a complete conversion (measured from HOLD command to EOC) requires about 27μsec (28 max.) at the standard clock rate. Short-cycling the converter will reduce this conversion time (see figure 3). Optionally, the user may generate the required delay externally, for highest attainable throughput rate.

HOW TO ORDER

To order any one of the 8 standard systems, simply specify the model number given in the chart below. For example, Model 6812-S has the standard ranges specified on page 6, the standard Tri-State output buffers (CMOS-compatible levels, 2-TTL low-power loads) *and accepts only 16 single-ended inputs.* All standard models are shipped with a mating right-angle connector.

MODEL NUMBER	RANGES		INPUTS		OUTPUTS	
	10V & 5V Full Scale (Bipolar & Unipolar)	10.24V & 5.12V Full Scale (Bipolar & Unipolar)	16 Single-Ended	8 Differential or 16 Pseudo-Differential	CMOS Tri-State (2-TTL Loads)	TTL Tri-State (10-TTL Loads)
MP6812-S	√	—	√	—	√	—
MP6812-SR	—	√	√	—	√	—
MP6812-D	√	—	√	√	√	—
MP6812-DR	—	√	√	√	√	—
MP6812-ST	√	—	√	—	—	√
MP6812-DT	√	—	√	√	—	√
MP6812-SRT	—	√	√	—	—	√
MP6812-DRT	—	√	√	√	—	√

ACCESSORIES

AN88 contains all necessary facilities (less power supply) for complete check-out and use of the MP6812, and is laid out to minimize input signal interference.

MP6848 expands channel capacity to four times standard. (See page 9 for details.)

TEST PROCEDURES AND DOCUMENTATION

After final assembly and burn-in, every MP6812 is exhaustively tested by a computer-programmed test procedure. The printout (see sample, which is shown here reduced) is shipped with the unit, to verify full compliance with the specifications, at the time of shipment.

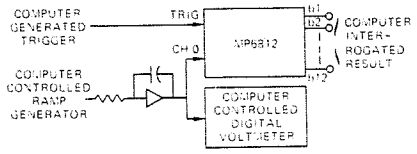
There follows an explanation of the tests performed on an MP6812-DR (see page 7 for capabilities).

DIGITAL SECTION TESTS

1. **MUX Address with Parallel Loading.** The multiplexer address register is parallel loaded with all 16 possible input codes progressing from 1111 to 0000 in a binary sequence. For each code the 5 output lines (1, 2, 4, 8, and $\overline{8}$) are tested for equality to the input code. When all 16 tests have been successfully performed the word "PASS" is printed.
2. **MUX Address with Auto-Sequencing.** The multiplexer address register is parallel loaded with a code of 0000. The multiplexer is then configured in an automatic sequencing mode. Each strobe pulse applied to the unit will cause the register to advance its count in a binary fashion. The 5 output lines are checked for each of the 16 possible counts as the register is sequenced. When all 16 tests have been successfully completed the word "PASS" is printed.
3. **MUX Clear Function.** The multiplexer address register is parallel loaded with a code of 1111. The clear function is applied to the register. The 5 output lines are checked for the channel 0 code; when the test is successfully completed the word "PASS" is printed.
4. **Delay Time.** In this test, the internal-delay pulse duration is measured and printed.
5. **Conversion Time.** In this test, the 12-bit conversion is measured and printed.

ANALOG SECTION TESTS

1. **Channel 0 Accuracy Test.** Using a unique Analogic technique (see diagram), the code-center voltages of 22 critical spots on the transfer characteristic for the converter are measured and listed.



For each measured code, the computer manipulates the input voltage to ramp between the code above the desired code and the code below the desired code. The average input voltage is thus equal to the center voltage of the desired code. This voltage is measured by the DVM and stored in the computer. Each code center reading is a result of several hundred conversions. If the desired code does not appear at the MP6812 output during the test, the word "YES" is printed in response to the missing code question. After the 22 data points have been measured, any range or offset errors present on the ±10.24 Volt range are mathematically removed from the readings before the results are printed. Thus, the printed results show the absolute accuracy to be obtained with proper adjustment of the range and offset controls. The error limits are ±0.025% of full-scale range.

2. **Missing-Code Test.** Using a technique similar to the accuracy test, but without the DVM measurement, the input voltage is slowly moved from + full scale to − full scale while the MP6812 continually converts. The word "PASS" is printed only if all 4096 possible codes occurred during the sweep.
3. **Range and Offset Errors.** Before the MP6812 is tested, the 16-turn range and offset potentiometers are physically centered. During the test, the actual range and offset errors are measured for each of the four programmable voltage ranges. If the errors are within calculated design limits, then the range and offset potentiometers will have ample adjustment capability.
4. **Channel Check.** In this test, a code-center measurement is made at + full scale on each of the 16 MUX channels. The difference between the channel 0 reading and the other 15 channels is listed. Maximum error is ±½ LSB or ±2.5mV.
5. **Slew Rate and Settling Time Test.** In this test, a fixed input near minus full scale is applied to channel zero and a fixed input near plus full scale is applied to channel fifteen. For the first conversion, channel zero is addressed; and, after a long waiting period, a measurement is made. For the second conversion, channel fifteen is addressed, and the MP6812 is configured in the auto-sequence mode. When the trigger pulse is given, the unit will advance to channel zero, slew from + to − full scale, and measure the channel zero input. Any difference between the two conversions is a measure of the slew-rate and settling-time ability. The error limits are ±2 bits.
6. **Differential CMR Test.** Here the MP6812 is connected differentially, with the two inputs for channel zero shorted together. They are first connected to +10, and a conversion is made. They are then connected to −10, and a second conversion is made. The difference between the two conversions is a measurement of the CMR.

```
ANALOGIC CORPORATION        AUDUBON ROAD      WAKEFIELD, MASS   01880
MP6812----------DATA ACQUISITION SYSTEM MODULE----------FINAL DATA
DATE  AUGUST 28, 1975              SERIAL NUMBER: 53502
------------------------DIGITAL SECTION TESTS-------------------------
MUX ADDRESS WITH PARALLEL LOADING                        PASS
MUX ADDRESS WITH AUTO-SEQUENCING                         PASS
MUX CLEAR FUNCTION                                       PASS
DELAY TIME (USEC)                                NOM=006.  0
CONVERSION TIME (USEC)                           NOM=027.50
----------------SHORT CYCLE CONVERSION TIMES (USEC)-----------------
11 BITS=C25.21     10 BITS=022.91      9 BITS=020.63      8 BITS=018.33
 7 BITS=016.04      6 BITS=013.75      5 BITS=011.46      4 BITS=009.17
------------------------ANALOG SECTION TESTS--------------------------

CH 0 ACCURACY TEST                          VOLTAGES REFER TO CODE CENTERS

CODE            THEORETICAL   ACTUAL        ERROR          MISSING CODE?
111111111110     +10.2300     +10.2300      +00.0000           NO
111111111100     +10.2200     +10.2205      +00.0005           NO
111111111000     +10.2000     +10.2013      +00.0013           NO
111111110000     +10.1600     +10.1614      +00.0014           NO
111111100000     +10.0800     +10.0820      +00.0020           NO
111111000000     +09.9200     +09.9220      +00.0020           NO
111110000000     +09.6000     +09.6023      +00.0023           NO
111100000000     +08.9600     +08.9622      +00.0022           NO
111000000000     +07.6800     +07.6819      +00.0019           NO
110000000000     +05.1200     +05.1206      +00.0006           NO
100000000000     +00.0000     +00.0000      +00.0000           NO
010000000000     -05.1200     -05.1166      +00.0034           NO
001000000000     -07.6800     -07.6777      +00.0023           NO
000100000000     -08.9600     -08.9586      +00.0014           NO
000010000000     -09.6000     -09.5990      +00.0010           NO
000001000000     -09.9200     -09.9194      +00.0006           NO
000000100000     -10.0800     -10.0798      +00.0002           NO
000000010000     -10.1600     -10.1602      -00.0002           NO
000000001000     -10.2000     -10.1998      +00.0002           NO
000000000100     -10.2200     -10.2198      +00.0002           NO
000000000010     -10.2300     -10.2300      +00.0000           NO
000000000001     -10.2350     -10.2348      +00.0002           NO
----------------------MISSING CODE TEST-----------------------------PASS
CHECK FOR PRESENCE OF ALL 4096 CODES
---------RANGE & OFFSET ERRORS WITH POTENTIOMETERS CENTERED---------
V RANGE      0 ERROR      R ERROR
+,-10.24     -00.0037     -00.0327
+,-5.12      -00.0053     -00.0160
0-10.24      -00.0119     -00.0381
0-5.12       -00.0081     -00.0200
-----DIFFERENCE BETWEEN CH 0 & CH 1-15 , +FULL SCALE  +,-10.24V------
CH 0=REFERENCE     CH 1=+00.0005      CH 2=+00.0004      CH 3=+00.0010
CH 4=+00.0002      CH 5=+00.0008      CH 6=+00.0005      CH 7=+00.0012
CH 8=+00.0003      CH 9=+00.0008      CH10=+00.0006      CH11=+00.0012
CH12=+00.0004      CH13=+00.0008      CH14=+00.0007      CH15=+00.0013
--------------------SLEW RATE & SETTLING TIME TEST---------------------
# BITS ERROR CAUSED BY 20V SLEW (NOMINAL DELAY TIME)              +00000
--------------DIFFERENTIAL COMMON-MODE REJECTION TEST----------------
OUTPUT DEVIATION WITH 20V COMMON-MODE CHANGE                  -00005 MV
```

SPEED/RESOLUTION TRADEOFF

As noted earlier (page 4, and figure 3), the A/D converter in the MP6812 may be short-cycled, to reduce conversion time, thereby trading off resolution for increased throughput. Table 2 shows the interconnecting-jumper connections required to shorten the cycle. . . . . in other words, for resolution of Bn, connect 28T to B(nth).

ADJUSTMENTS

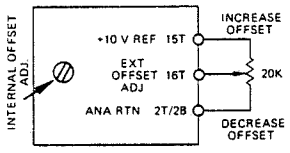
Full range and offset adjustments are provided internally; however, if *remote* range and offset adjustments are required, use the following procedure.

Zero Offset. To recalibrate the OFFSET: Apply the input voltage shown in table 3, and adjust the OFFSET control so that the LSB of the output codes listed in the table alternates equally between "1" and "0". Offset should be readjusted whenever the selected range is changed.

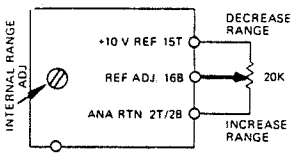
Range (OFFSET should be trimmed before adjusting RANGE).

To recalibrate the RANGE: Apply the input voltage shown in table 4, and adjust the RANGE control so that the LSB of the output code alternates equally between "1" and "0". Range should be readjusted whenever the selected range is changed.

External Trimming Connections



EXTERNAL OFFSET TRIMMING CONNECTIONS



EXTERNAL RANGE TRIMMING CONNECTIONS

RANGE SELECTION

Table 5 describes the simple procedure for range selection.

Table 2

RESOLUTION	CONNECT PIN 28T TO:	RESOLUTION	CONNECT PIN 28T TO:
12 BITS (FULL)	PIN 36B (+5V)	9 BITS	PIN 33B (B10)
11 BITS	PIN 34B (B12)	8 BITS	PIN 33T (B9)
10 BITS	PIN 34T (B11)	etc.	etc.

Table 3

RANGE	INPUT	OUTPUT CODE (B1, B2, . . . B12)			
−10V to +10V	+0.0024V	100	000	000	000/1
0V to +10V	+0.0012V	000	000	000	000/1
−5V to +5V	+0.0012V	100	000	000	000/1
0V to +5V	+0.0006V	000	000	000	000/1

NOTE: for "R" models, multiply inputs by 1.024, for corresponding ranges.

Table 4

RANGE	INPUT	OUTPUT CODE (B1, B2, . . . B12)			
−10V to +10V	+9.9927V				
0V to +10V	+9.9853V	111	111	111	110/1
−5V to +5V	+4.9853V				
0V to +5V	+4.9927V				

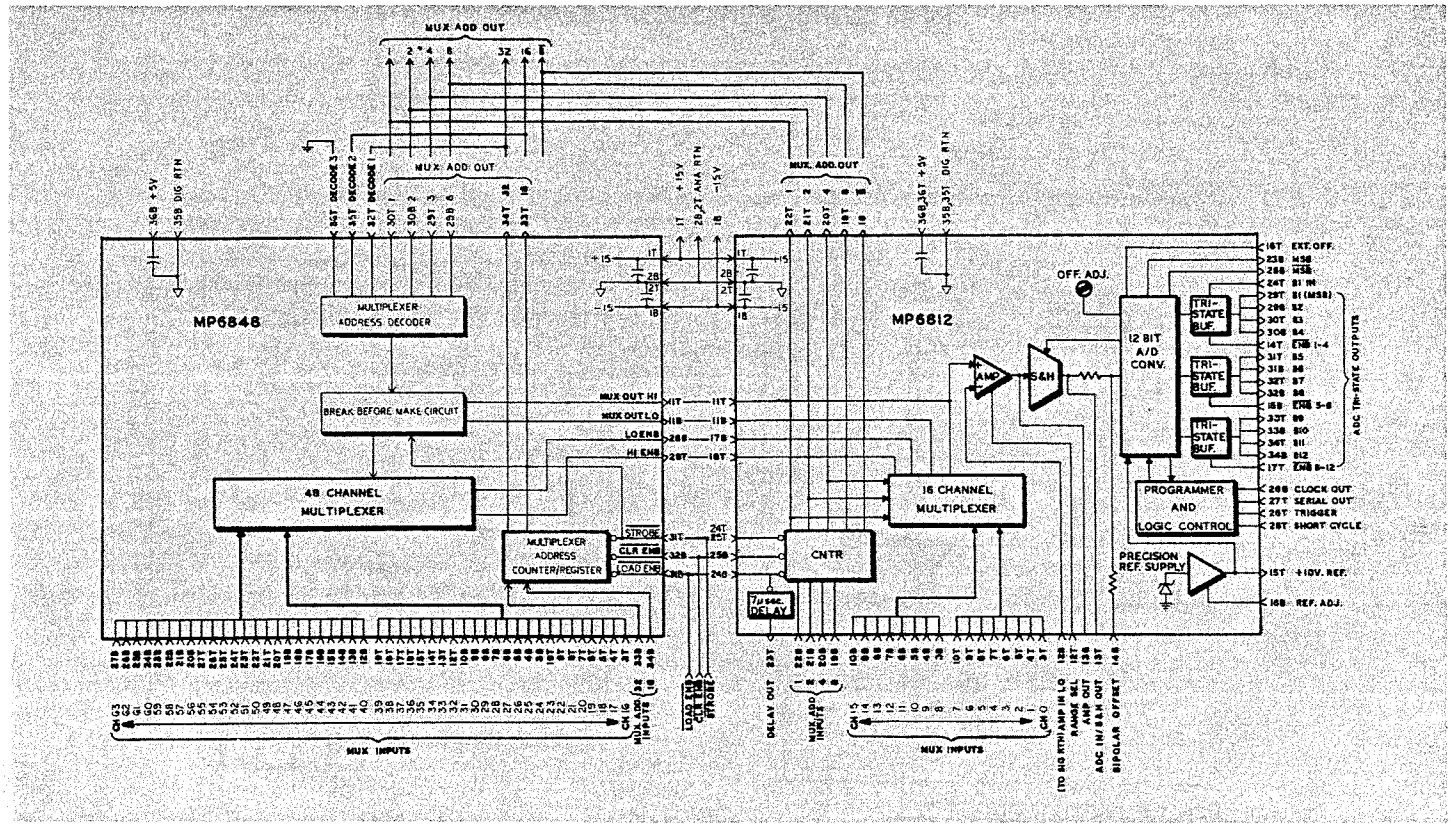
NOTE: For "R" models, use the following input: +10V, +10V, +5V, +5V.

Table 5

MAKE THE FOLLOWING CONNECTIONS		
	SINGLE-ENDED UNITS	DIFFERENTIAL UNITS
0V to +10V	12T to 13B, 13T to 14B	12T to 2T; 13T to 14B
0V to +5V	12T to 2T, 13T to 14B	12T to 13B; 13T to 14B
−10V to +10V	12T to 13B, 14B to 15T	12T to 2T; 14B to 15T
−5V to +5V	12T to 2T, 14B to 15T	12T to 13B; 14B to 15T

MULTIPLEXER EXPANSION

Figure 10 shows the interconnection scheme for expanding the basic multiplexer channel capacity of an MP6812 (16 single-ended/8 differential/16 pseudo-differential) to a total of 32 differential/64 single-ended or pseudo-differential channels, using the MP6848 MUX expander module.

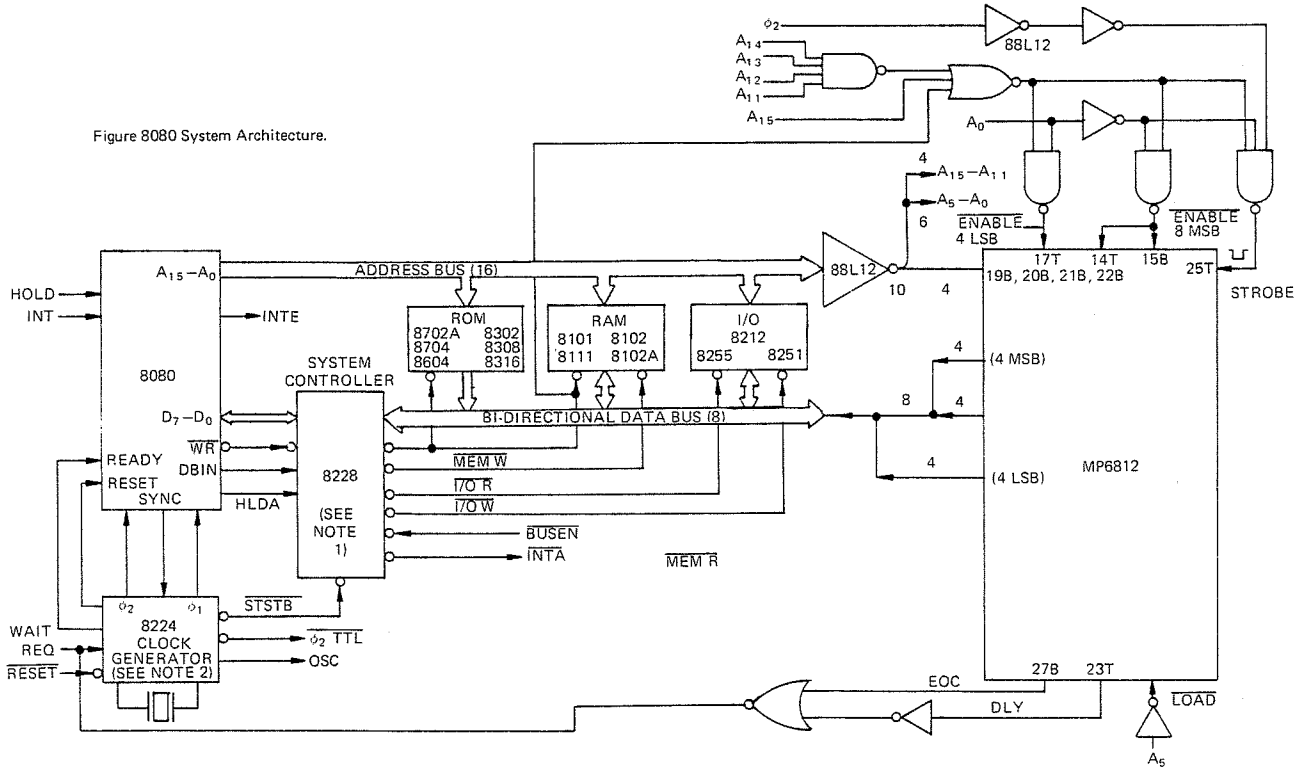


Expanded 64 Channel Single-Ended System

TYPICAL MICROPROCESSOR APPLICATIONS

MP6812 with INTEL 8080

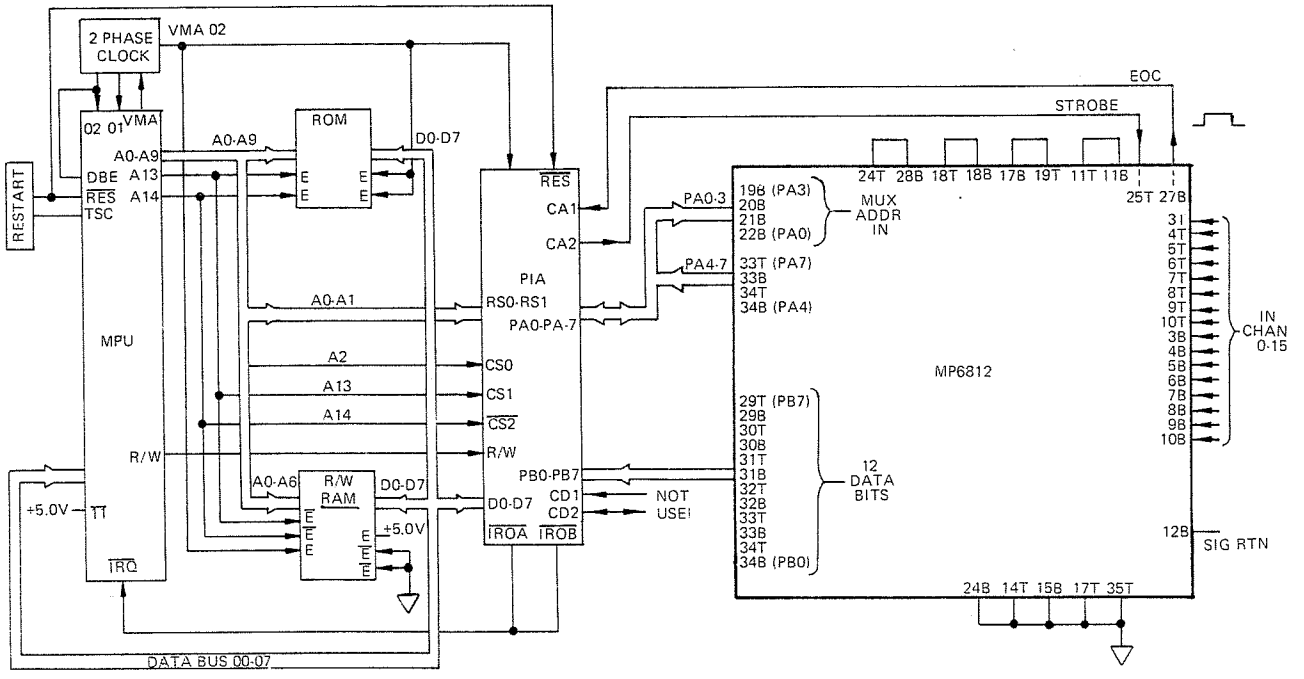
Figure 8080 System Architecture.



MP6812 with MOTOROLA MP6800

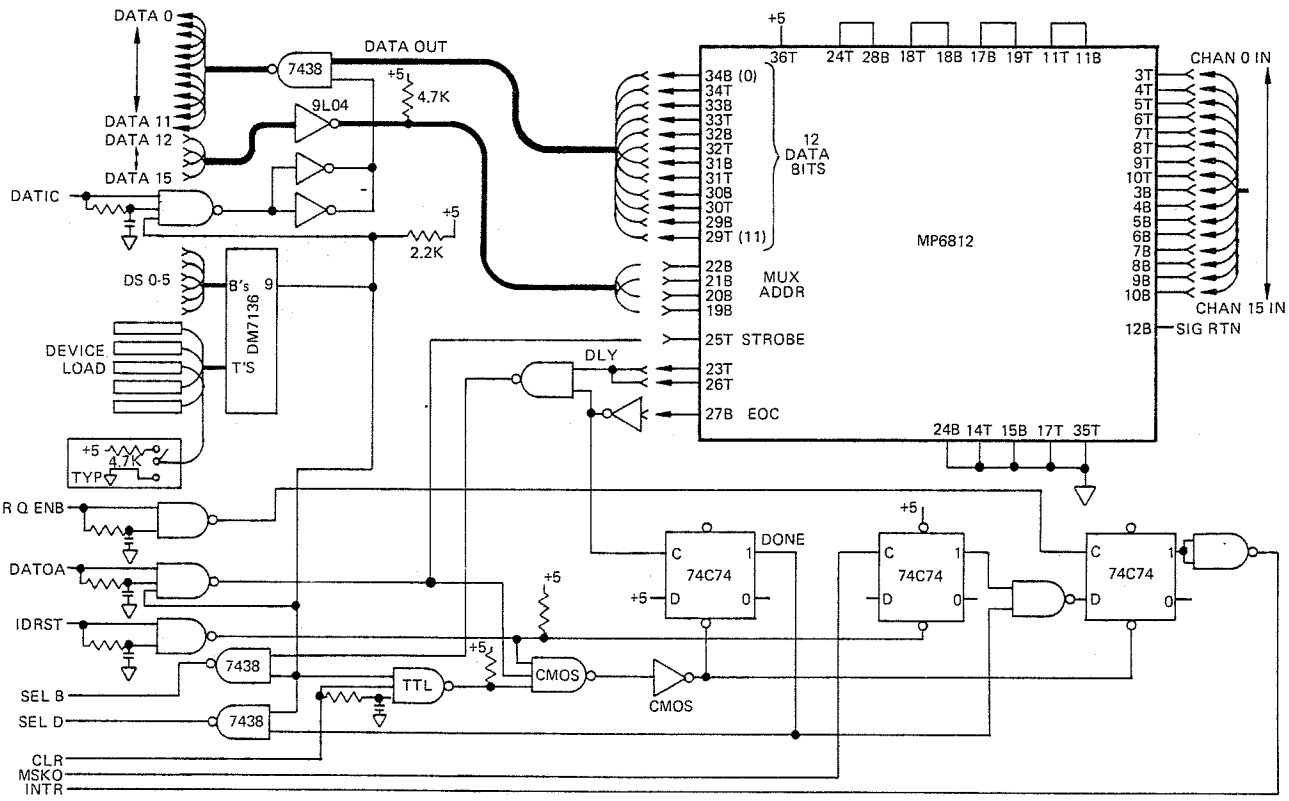
PROGRAM:
PA0-3 AS OUTPUTS
PA4-7 AS INPUTS
PB0-7 AS INPUTS
CA1 TO RESPOND TO NEGATIVE TRANSITION
CA2 AS OUTPUT

SEND CHANNEL = (MUX ADDRESS TO ORA, (RIGHT JUSTIFIED), BITS 0-3 –60
PROGRAM A NEGATIVE PULSE ON CA2 TO START MEASUREMENT
INTERRUPT FROM CA1 INDICATES VALID MEASURED DATA AVAILABLE
READ IN DATA; 8 MSB'S VIA PB0-7
; 4 LSB'S VIA PA4-7, (LEFT JUSTIFIED)

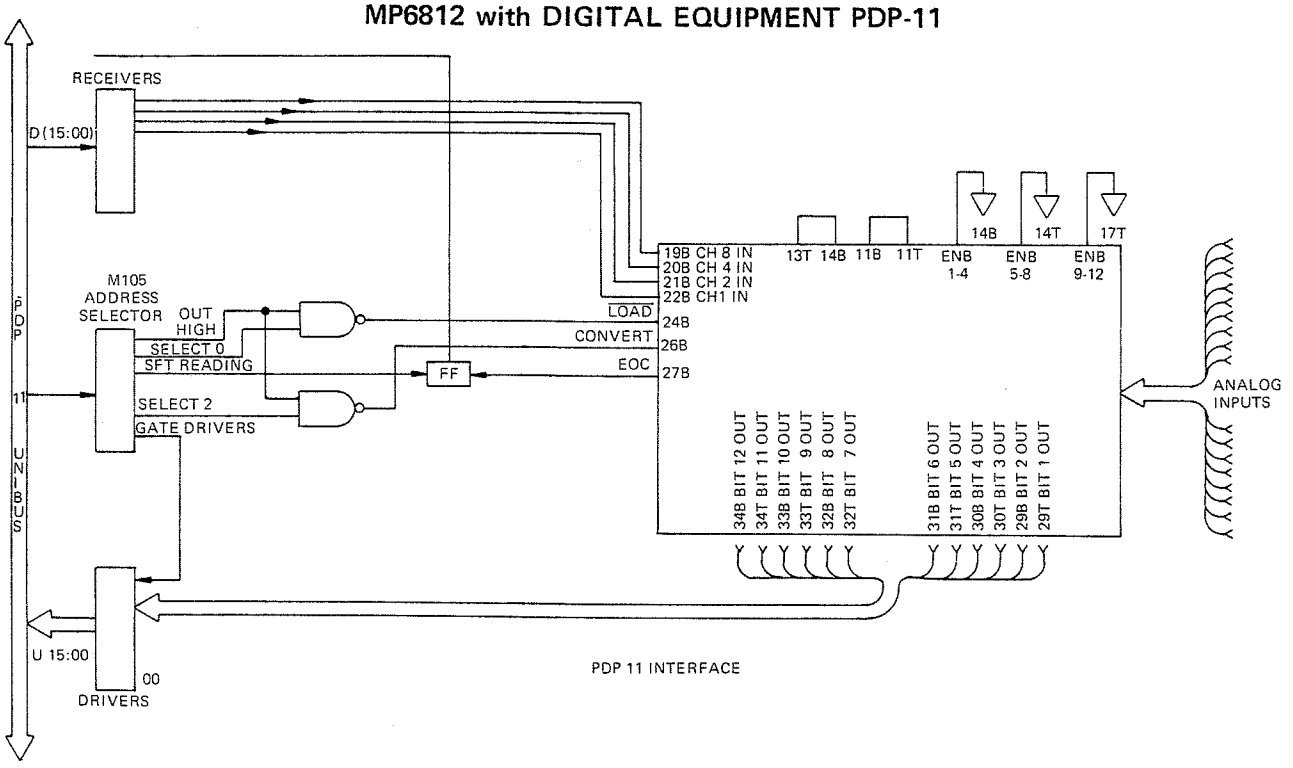


TYPICAL MINICOMPUTER APPLICATIONS

MP6812 with DATA GENERAL NOVA/SUPERNOVA



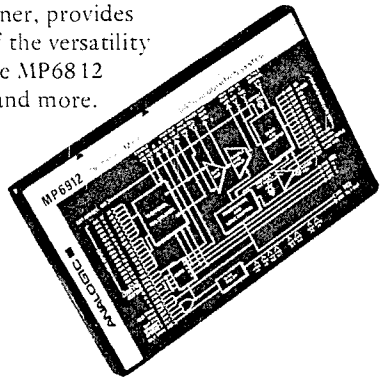
MP6812 with DIGITAL EQUIPMENT PDP-11

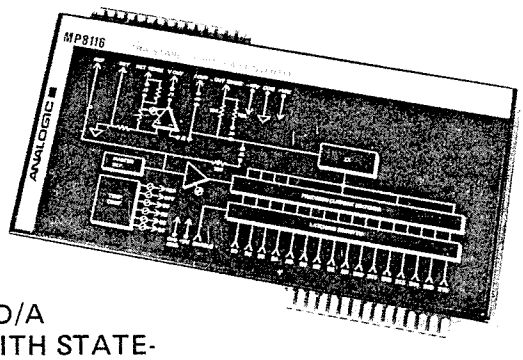


ANALOGIC MANUFACTURES SUBSYSTEMS & COMPLETE SYSTEMS FOR EVERY DATA-ACQUISITION REQUIREMENT

MP6912 HIGH-SPEED MINICOMPUTER-COMPATIBLE SYSTEM.

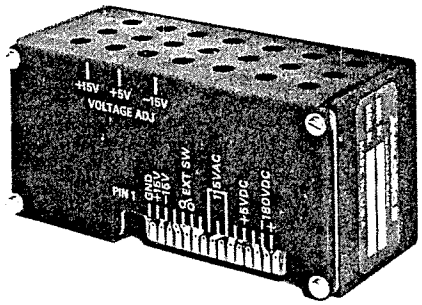
For use within minicomputers and very-high-speed microprocessor systems, the Analogic MP6912 is the smallest, most versatile, completely self-contained high-speed modular 16-channel data acquisition system ever offered to the system designer, provides all of the versatility of the MP6812 . . . and more.





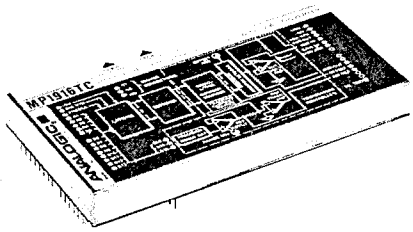
MP8116 16-BIT D/A CONVERTER WITH STATE-OF-THE-ART ACCURACY, STABILITY & LINEARITY.

The Analogic MP8116 is the world's first 16-bit D/A converter in which the worst-case linearities, temperature coefficients, noise levels, and time stabilities have been engineered to be completely consistent with the realization and maintenance of absolute accuracy of better than one part in 2^{16}.



SERIES 5400 AND 5800 COMPUTER-COMPATIBLE A/D/A SYSTEMS WITH UNLIMITED CHANNEL CAPACITY.

Two families of low-cost modular systems, ideal for data conversion applications – from simple MUX-Buffer/ADC combinations to elaborate A/D-D/A interfaces under computer control. True plug-to-plug compatibility is provided for the standard minicomputer specified. A universal motherboard provides space and interwiring for an extremely wide range of functions and capabilities.



CONVERTERS.

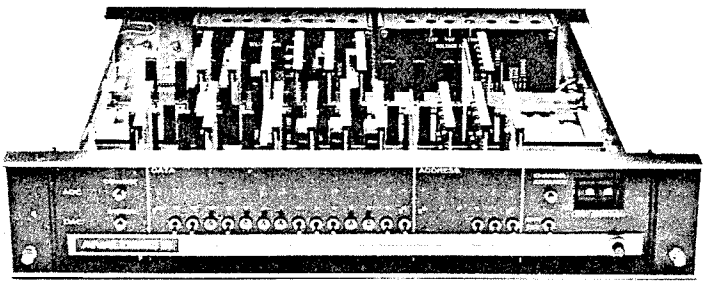
The industry's widest range of A/D and D/A converter modules and IC's. The A/D designs include both integrating and successive-approximation types. Designs available in every price/performance slot, from economy 8-bit to state-of-the-art 16 bit.

POWER SUPPLIES.

Designed to provide all necessary DC power for both analog and digital circuitry of data acquisition systems, this series comes in two basic forms – chassis mount and modular. Both DC-DC and AC-line-powered designs are available in a wide range and variety of voltages and currents.

ACCESSORY MODULES.

A wide range of optimized accessory-circuit modules, including Multiplexers, Sample-Holds, and Operational Amplifiers,(including programmable-gain designs), and Active Filters.



AVAILABLE FROM:

ANALOGIC® Audubon Road ■ Wakefield, Massachusetts 01880 ■ Tel. (617) 246-0300 ■ TWX (710) 348-0425
ANALOGIC INTERNATIONAL ■ Audubon Road ■ Wakefield, Massachusetts 01880 ■ Tel. (617) 246-0300 ■ TWX (710) 348-0425
ANALOGIC LIMITED ■ 68 High Street ■ Weybridge, Surrey, KT13 8BN ■ England ■ Tel. Wey 41251 ■ Telex (851) 928030
Bulletin No. 16-100052 REV 1

INTERCONNECTION GUIDE

MP6812
Complete Subminiature
Data-Acquisition System

ANALOGIC

INPUT CONFIGURATIONS

The –S, –SR, –ST, and –SRT versions of the MP6812 are dedicated to 16 single-ended inputs and do not require pin interconnections. The –D, –DR, –DT, and –DRT versions of the MP6812 offer a choice of three input configurations: (1) 16 single-ended inputs, (2) 8 true-differential inputs, or (3) 16 pseudo-differential inputs, by properly interconnecting pins on the module. These interconnections are summarized below.

INPUT CONFIGURATION	ANALOG INPUT CONNECTIONS	ANALOG INPUT RETURN CONNECTIONS	JUMPER CONNECTIONS
16 Single-Ended Inputs	3T thru 10T 3B thru 10B	All returns to 2B or 2T	11B to 11T 12B to 2B 17B to 19T 18B to 18T
8 True Differential Inputs	3T thru 10T	3B thru 10B	11B to 12B
16 Pseudo-Differential	3T thru 10T 3B thru 10B	Common input to 12B	11B to 11T 17B to 19T 18B to 18T

1. Connect all unused analog inputs to 2B or 2T.
2. See Figures 1a, 1b, and 1c in MP6812 Brochure.

GROUNDING CONSIDERATIONS. In order to minimize noise pickup, ground loop currents, and ground-path voltage drops, careful attention must be paid to how the electrical returns and voltage reference points are connected. (The MP6812 provides internal connections for ANA RTN and DIG RTN.) A typical system using the MP6812 has several "grounds" which include:

(1) ±15V Return
(2) +5V Return
(3) Signal Returns
(4) Computer Ground
(5) Chassis
(6) Third-Wire Ground

Each of these must be connected correctly to the system. The following rules generally apply:

1. If the ±15V power supply is floating (a good idea for optimum analog accuracy), connect its return to ANA RTN (Pin 2B or 2T). If the ±15V power supply is **not** floating, connect its return to DIG RTN (Pin 35T or 35B).

2. Connect the +5V supply return to DIG RTN (Pin 35T or 35B). If this supply also powers additional equipment (i.e., a computer), run **separate, parallel returns** to the equipment ground and to DIG RTN (Pin 35T or 35B).

3. To minimize signal grounding problems, single-ended input signals should only be returned to ANA RTN (Pin 2B or 2T). If this is not possible, then connect the input signals in either the "true differential" or the "pseudo-differential" configuration (see Figure 1, MP6812 Brochure).

4. Connect computer ground, generally the return for the digital I/O signals,to DIG RTN (Pin 35T or 35B). Use heavy wire (#14AWG) or ground planes.

5. The computer chassis should be connected to the computer and power supply grounds at only one point. If this is not done, a ground loop will exist. Its effect can be minimized by assuring that the components of the loop (i.e., chassis to MP6812 ground, MP6812 to ±15V supply ground, and the chassis to ±15V supply ground) are physically as close as possible.

6. Connect the third-wire ground from main AC power input to the computer power supply return.

SELECT MUX ADDRESS-LOADING MODE

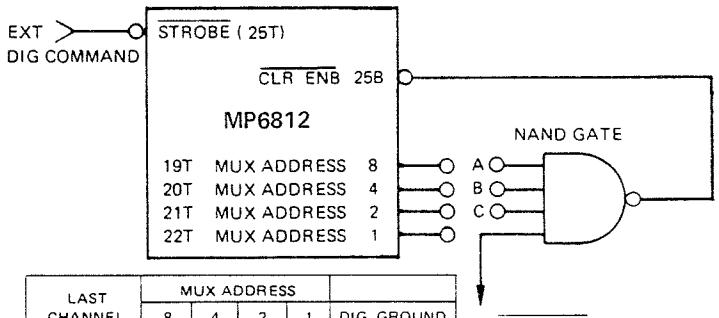
The method of addressing the multiplexer can be selected by connecting the MP6812 as follows:

RANDOM. Set Pin 24B ($\overline{\text{LOAD ENB}}$) to logic "0". The next falling edge of $\overline{\text{STROBE}}$ will load the address presented to Pins 19B thru 22B (8, 4, 2, 1). The code on these lines must be stable during, and for 100ns after, the falling edge of $\overline{\text{STROBE}}$.

SEQUENTIAL FREE RUNNING. Set to logic "1" Pins 24B ($\overline{\text{LOAD ENB}}$) and 25B ($\overline{\text{CLR ENB}}$). Connect Pin 27B ($\overline{\text{EOC}}$) to Pin 25T ($\overline{\text{STROBE}}$). Connect Pin 23T ($\overline{\text{DLY OUT}}$) to Pin 26T ($\overline{\text{TRIG}}$). To provide a run/stop control, a Nand gate should be introduced between Pins 23T and 26T; one input can be used to enable or disable conversion.

To shorten scanning sequence of multiplexer channels, make the appropriate connections, (as shown in the chart) between an external NAND gate and MUX ADDRESS terminals 19T to 22T.

MUX SCAN-CONTROL CONNECTIONS



LAST CHANNEL	MUX ADDRESS 8	4	2	1	DIG. GROUND
1	X	X	X	A	X
2	X	X	B	X	X
3	X	X	B	A	X
4	X	C	X	X	X
5	X	C	X	A	X
6	X	C	B	X	X
7	X	C	B	A	X
8	C	X	X	X	X
9	C	X	X	A	X
10	C	X	B	X	X
11	C	X	B	A	X
12	B	C	X	X	X
13	B	C	X	A	X
14	A	C	B	X	X
15	X	X	X	X	A

X = NO CONNECTION

If $\overline{\text{LOAD ENB}}$ is also used, connect this input to it (to 24B). This gives loading preference over clearing.

Note: For initial channel = M, connect gate output to $\overline{\text{LOAD ENB}}$ (24B) and code channel in 8, 4, 2, 1 to address M; however, this precludes random addressing.

SEQUENTIAL TRIGGERED. Set to logic "1" Pins 24B ($\overline{\text{LOAD ENB}}$) and 25B ($\overline{\text{CLR ENB}}$). Connect Pin 25T ($\overline{\text{STROBE}}$) to external triggering source. The multiplexer address register will automatically advance by one channel whenever a $\overline{\text{STROBE}}$ command is received. The initial channel can be selected by setting Pin 24B ($\overline{\text{LOAD ENB}}$) to logic "0" during only one $\overline{\text{STROBE}}$ command. The multiplexer address will then be determined by the logic levels on Pins 19B thru 22B (the external MUX address lines). Channel "0" can be selected as the initial channel by setting Pin 25B ($\overline{\text{CLR ENB}}$) to logic "0" during only one $\overline{\text{STROBE}}$ command. The last channel can be selected by following the procedure presented above.

SELECT OUTPUT RESOLUTION

a. Full 12 bit resolution: connect Pin 28T to Pin 36T.
b. Bn (Bn <12 bits) bit resolution: connect Pin 28T to Pin Bn +1. Example: For Bn = 8 bits (Bn +1 = B9 OUT), connect 28T to 33T.

SELECT INPUT VOLTAGE FULL SCALE

The basic input range is selected by ordering –S, –ST, –D, or –DT for 10 volts or –SR, –SRT, –DR, or –DRT for 10.24 volts. The input full-scale range is selected by implementing the appropriate interconnections, as listed below.

	MAKE THE FOLLOWING CONNECTIONS	
	For –S, –SR, –ST, –SRT Versions	For –D, –DR, –DT, –DRT Versions
0V to +10V	12T to 13B, 13T to 14B	12T to 2T; 13T to 14B
0V to +5V	12T to 2T, 13T to 14B	12T to 13B; 13T to 14B
–10V to +10V	12T to 13B, 14B to 15T	12T to 2T; 14B to 15T
–5V to +5V	12T to 2T, 14B to 15T	12T to 13B; 14B to 15T

SELECT OUTPUT CODING

Unipolar Binary 23B to 24T
Offset Binary 23B to 24T
2's Complement 28B to 24T
B1 output is at pin 29T.

TRI-STATE ENABLE

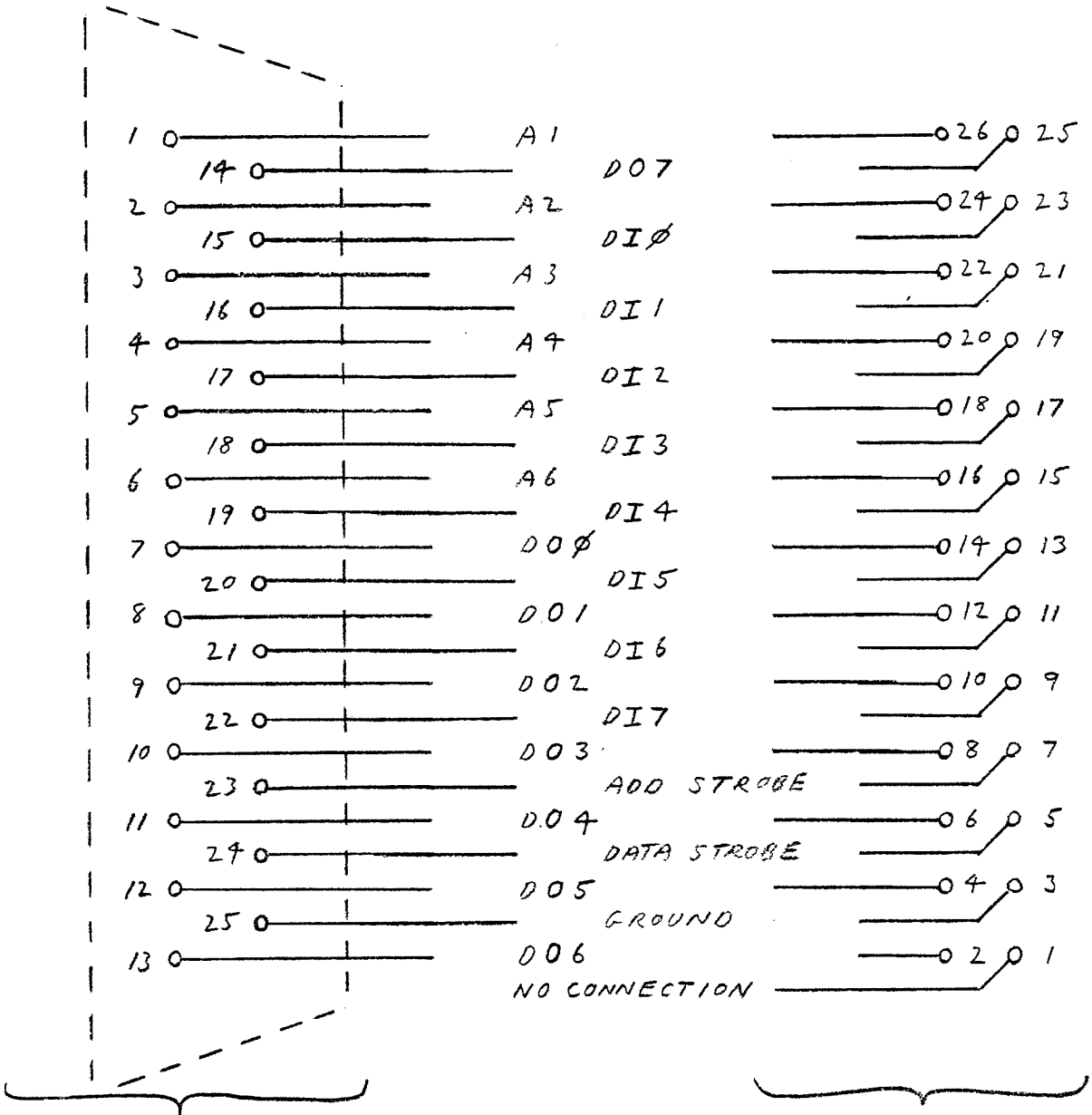
Pins 14T, 15B, and 17T control 4-bit bytes of the 12-bit output word. Pin 14T, when grounded to Pin 35T, presents bits 1-4 on the respective output lines. Pins 15B and 17T present bits 5 through 8 and 9 through 12, respectively, when grounded.

HOUSEKEEPING 64-CHANNEL ADC MULTIPLEXOR

Front Panel to PC Board Cabling

ADC Channel No.				Signal	Analog Ground	Chassis Ground	
P-1	P-2	P-3	P-4	Pin No.	Pin No.	Pin No.	Group
0	16	32	48	7	8	6	2
1	17	33	49	13	14	12	4
2	18	34	50	19	20	18	6
3	19	35	51	25	26	24	8
4	20	36	52	31	32	30	10
5	21	37	53	37	38	36	12
6	22	38	54	43	44	42	14
7	23	39	55	49	50	48	16
8	24	40	56	4	3	5	1
9	25	41	57	10	9	11	3
10	26	42	58	16	15	17	5
11	27	43	59	22	21	23	7
12	28	44	60	28	27	29	9
13	29	45	61	34	33	35	11
14	30	46	62	40	39	41	13
15	31	47	63	46	45	47	15

Note: P-1 through P-4 are 50-pin ribbon connectors from the front panel BNC's to PC board.



25 PIN "D" PLUG TO CONTROL MODULE. MODULE. VIEW LOOKING INTO MODULE.

I/O BOARD CONNECTOR. LOOKING AT COMPONENT SIDE OF BOARD.

DI ⇒ DATA INPUT TO INTERDATA

DO ⇒ DATA OUTPUT FROM INTERDATA

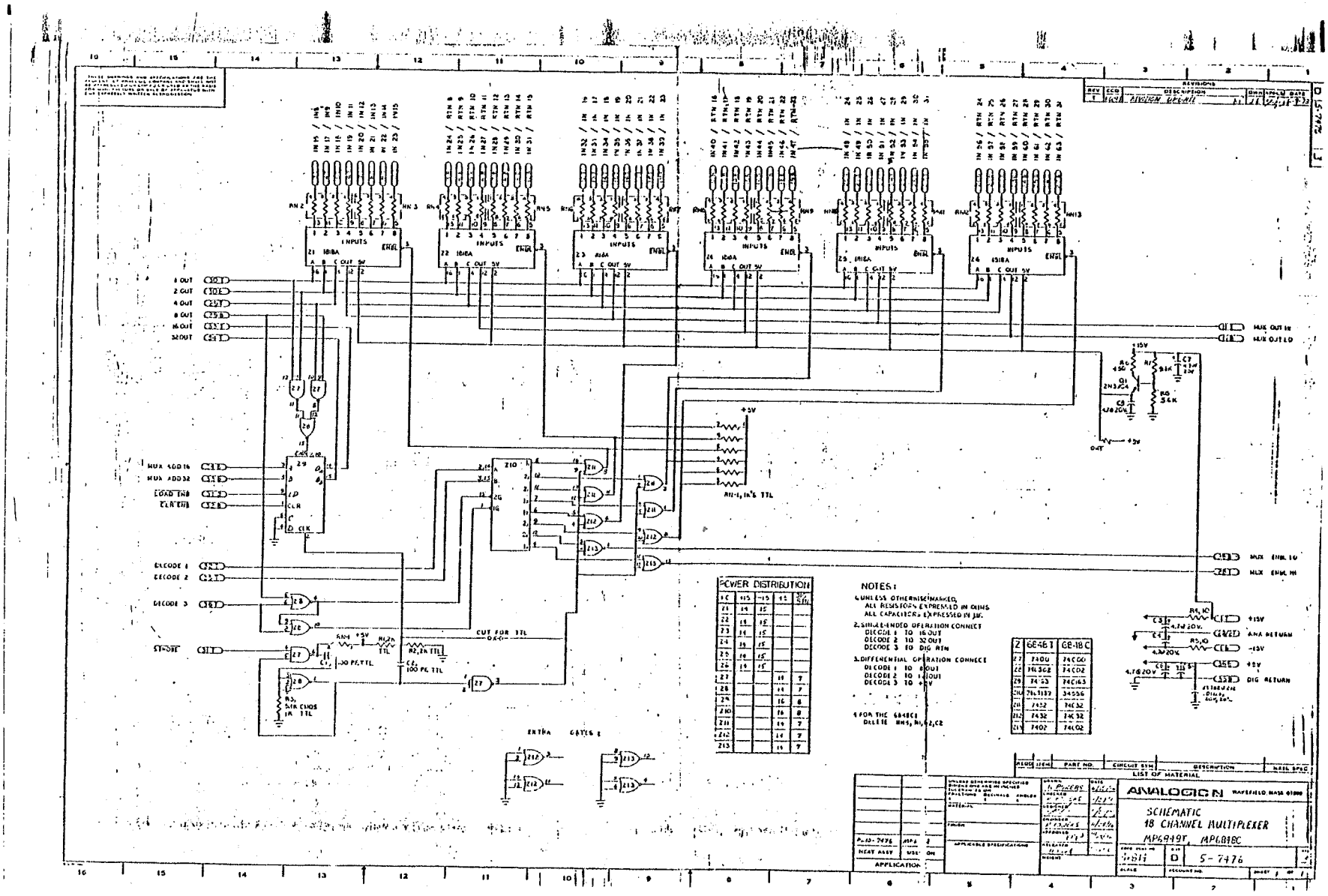
BIT #Ø IS LEAST SIGNIFICANT

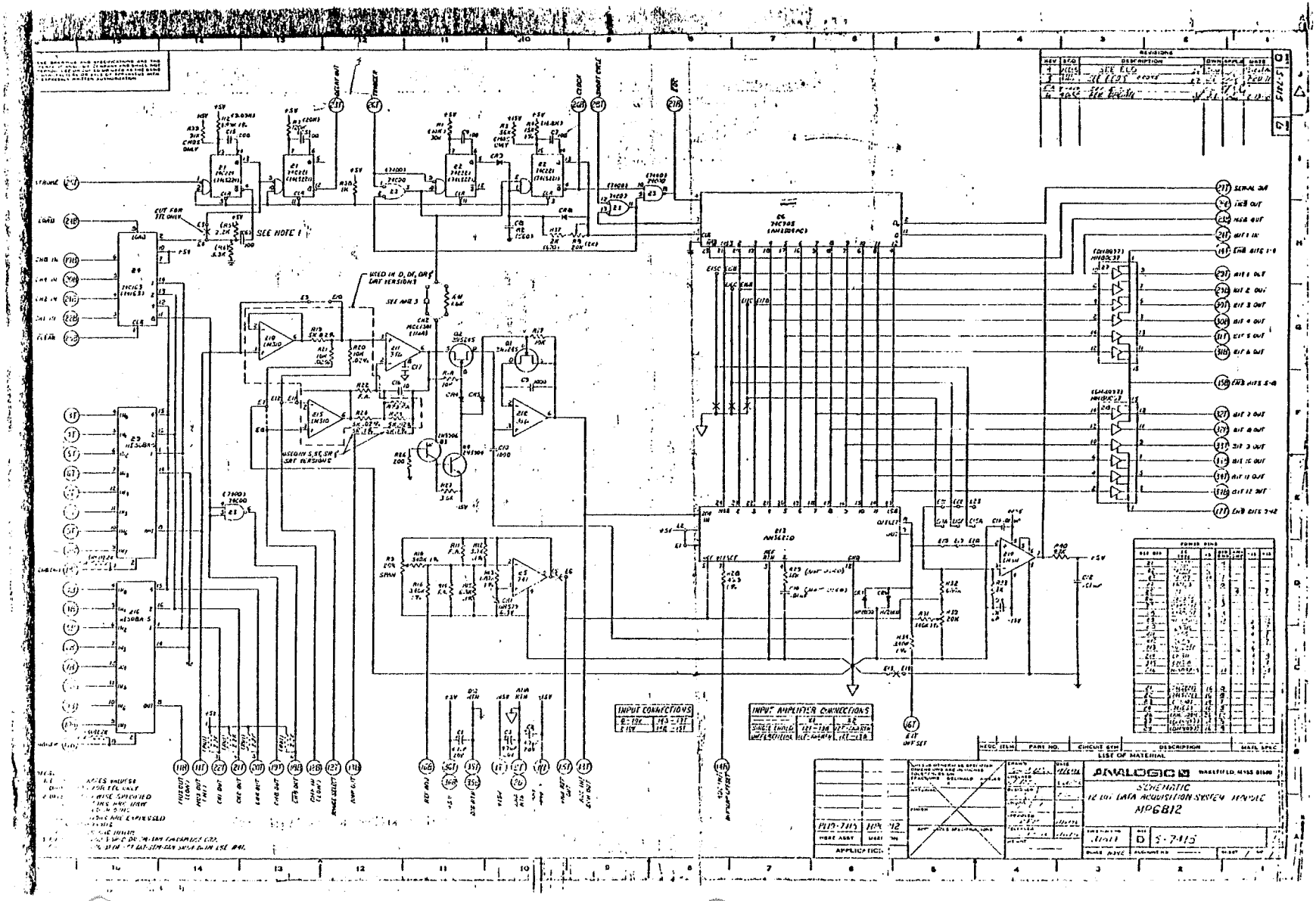
HF SOUNDER

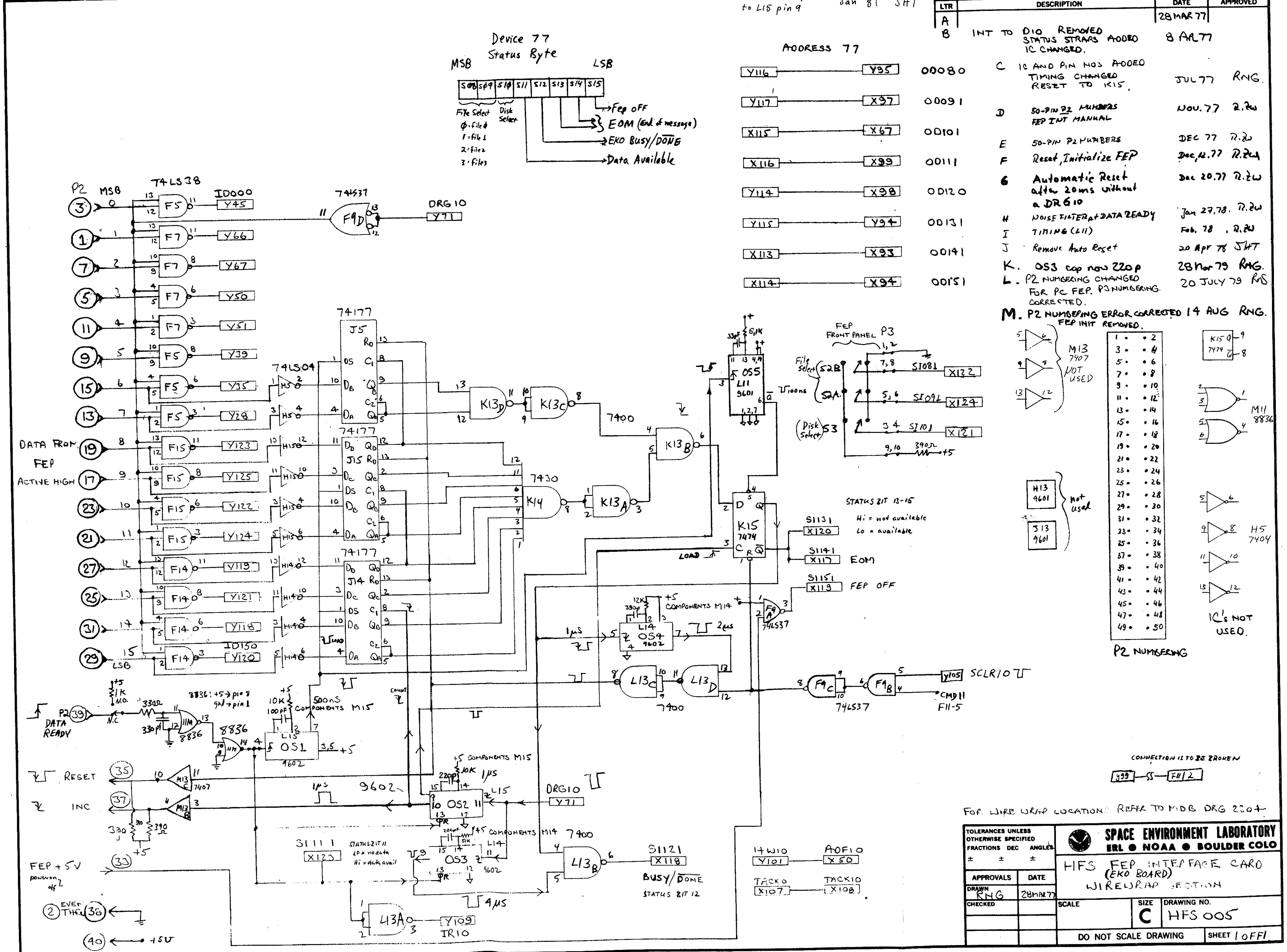
ISSUE 2

2-21-79

HFS 009.


REVISIONS
DESCRIPTION
ANALOGIC
SCHEMATIC
18 CHANNEL MULTIPLEXER
MP6949T MP6818C
5-7476
LIST OF MATERIAL
NOTES:
1. UNLESS OTHERWISE MARKED, ALL RESISTORS EXPRESSED IN OHMS ALL CAPACITORS EXPRESSED IN μF.
2. SINGLE-ENDED OPERATION CONNECT
DECODE 1 TO 16 OUT
DECODE 2 TO 32 OUT
DECODE 3 TO DIG RTN
3. DIFFERENTIAL OPERATION CONNECT
DECODE 1 TO 8 OUT
DECODE 2 TO 1 OUT
DECODE 3 TO +5V
4. FOR THE 6846CJ DELETE RN4, R1, C2, C8
POWER DISTRIBUTION
EXTRA GATES
CUT FOR TTL OPT.
STROBE
DECODE 1
DECODE 2
DECODE 3
MUX ADD 16
MUX ADD 32
LOAD THR
CLR THR
MUX OUT HI
MUX OUT LO
MUX ENBL LO
MUX ENBL HI
+15V
ANA RETURN
-15V
+5V
DIG RETURN


ANALOGIC
SCHEMATIC
12 BIT DATA ACQUISITION SYSTEM MODULE
MP6812
SEE NOTE 1
USED IN D, DF, DR, DRF VERSIONS
INPUT CONNECTIONS
INPUT AMPLIFIER CONNECTIONS
LIST OF MATERIAL



REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A		28 MAR 77	
B	INT TO D10 REMOVED STATUS STRAPS ADDED IC CHANGED.	8 APR 77	
C	IC AND PIN NOS ADDED TIMING CHANGED RESET TO K15.	JUL 77	RNG.
D	50-PIN P2 NUMBERS FEP INT MANUAL	NOV. 77	R.Z.W.
E	50-PIN P2 NUMBERS	DEC 77	R.Z.W.
F	Reset, Initialize FEP	Dec. 12. 77	R.Z.W.
G	Automatic Reset after 20ms without a DRG10	Dec 20. 77	R.Z.W.
H	NOISE FILTER at DATA READY	Jan 27. 78	R.Z.W.
I	TIMING (L11)	Feb. 78	R.Z.W.
J	Remove Auto Reset	20 Apr 78	JHT
K.	OS3 cap now 220p	28 Mar 79	RNG.
L.	P2 NUMBERING CHANGED FOR PC FEP. P3 NUMBERING CORRECTED.	20 JULY 79	RNG
M.	P2 NUMBERING ERROR CORRECTED FEP INIT REMOVED.	14 AUG	RNG.

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS ± DEC ± ANGLES ±

SPACE ENVIRONMENT LABORATORY
ERL ● NOAA ● BOULDER COLO

HFS FEP INTERFACE CARD (EKO BOARD) WIREWRAP SECTION

APPROVALS	DATE
DRAWN RNG	28 MAR 77
CHECKED	

SCALE | SIZE C | DRAWING NO. HFS 005

DO NOT SCALE DRAWING | SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-5766

ISSUE B 18 NOV 76
C 28 MAR 77
D 16 MAY 77
E SEPT 77
F 15 NOV 77
G 5 DEC 77
H 20 APR 78
I 1 APR 79 P1 change
J 4 DEC 80 15F change

Device 37₁₆ Status Byte

MSB							LSB
S08	S09	S10	S11	S12	S13	S14	S15
X	EOC	X	TSG Busy/Done	X	X	X	X

ADDRESS STRAP (37)
DEVICE CONTROLLER 1

Y116	00080	Y95
Y117	00090	X96
X115	00101	X67
X116	00111	X99
Y114	00120	X98
Y115	00131	Y94
X113	00141	X93
X114	00151	X94

S11Ø1 X121 — 11F pin 15 CMD 151 LSB OF CMD BYTE — 15F 7403

P3 P2

7407 +5 300Ω
10F DATST 3 → (3) (3)
10F ADQST 5 → (5) (5)
(7) (7)

Y105 SCLRIØ
Y1Ø ROR2Ø

7407 +5 0.1 390Ω

OUTPUT DATA REGISTER 2

		P3	P2
X18	LSB	26	26
Y4		24	24
Y19		22	22
X2		20	20
X17		18	18
Y5	MSB	16	16
X16	LSB	14	14
Y6		12	12
Y17		10	10
X5		8	8
X12		6	6
X9		4	4
X11		2	2
Y9	MSB	25	25

LD

+5 12K 100pf 13F OS3 +5 .5µs 96502
+5 12K 220pf 13F OS2 +5 1µs 96502
+5 12K 1000pf 14F OS1 +5 .5µs
OAG1Ø X111 — Y12 LOR 2Ø

12K 470pf 14F OS4 +5 1.7µs

ORG1Ø ROIR2Ø Y71 — Y106
LIR2BØ Y52
LIR2AØ Y86

INPUT DATA REGISTER 2

7407 +5 P3 P2

		P3	P2
Y87	LSB 1K 390	23	23
X88		21	21
X86		19	19
X87		17	17
X78		15	15
X69		13	13
Y78		11	11
Y69		9	9
X35		33	
X37		31	
X39		29	
Y38	MSB 1K 390	27	

8 bit

X55 X53 Y56 Y54

HWI Ø Y1Ø1 — X5Ø ADF1 Ø
Y39 — // — pin 2 - 11F BREAK

RACK2Ø IACK1Ø TACK2Ø TACK Ø
Y2 — X1Ø8 Y1 — X1Ø7
INTERUPT PRIORITY STRAP

DEVICE CONTROLLER 1
INTERUPT CONTROL

+5 1K +5 1K 74132 IR1Ø
P2 (45) EOCINT
P1 (15) TSG INT (TSG Busy/Done) INT MANUAL N.C. NO.
15F 15F 1K +5
X123 S1111
X124 S1Ø91

DIO ADDRESS OUT
X126 X118 X119 X117 X122 — X125

DEVICE CONTROLLER 2
INTERUPT CONTROL.

ADDRESS STRAP. 47

Y64	00080	Y95
X65	00091	X97
X63	00100	X42
Y65	00110	X100
X64	00120	X98
Y63	00131	Y94
X62	00141	X93
Y62	00151	X94

DIO DATA OUT

Device 47₁₆ Status Byte

MSB							LSB
S08	S09	S10	S11	S12	S13	S14	S15
FEP PWR	FEP OVF	ANL OVL	+15 OVL	X	X	X	X

P1 (2) (16) DIO DATA IN.
+5OVL ANLOVL FEP OVF FEP PWR
7420 9J 9J IR2Ø Y43
1K +5 1K +5 1K
X74 Y72 Y75 X71
S2111 S2101 S2091 S2081
X73 Y73 Y74 X72 — X75

P1, P2, P3 PIN POSITIONS:

1	2
3	4
5	6
7	8
9	10
11	12
13	14
15	16
17	18
19	20
21	22
23	24
25	26
27	28
29	30
31	32
33	34
35	36
37	38
39	40
41	42
43	44
45	46
47	48
49	50

REFER TO MDC DRG 2204 SHEET 1 FOR WRAP PIN LOCATIONS eg X111

S.E.L.

SCALE:	APPROVED BY:	DRAWN BY
DATE:		REVISED

HFS DIO I/O CARD LOGIC SHEET 1 OF 2
WIREWRAP SECTION
DRAWING NUMBER HFS 006

17X22 PRINTED ON NO. 1000H-10 CLEARPRINT

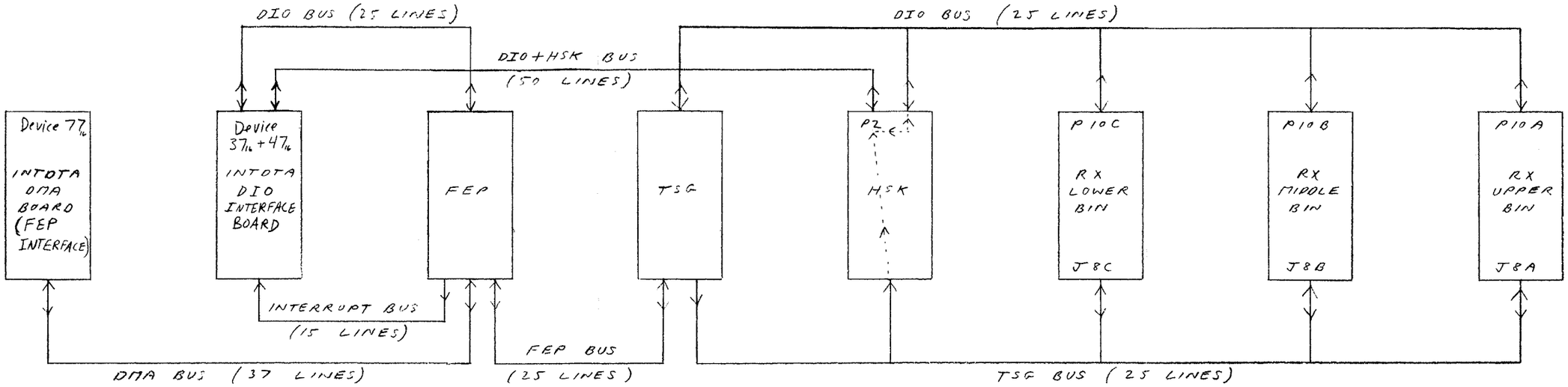
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	18 NOV 76		
B	23 NOV 76 CORRECTION.		
C	5 DEC 76 CORRECTION 4A.		

	11	10	9	8	7	6	5	4	3	2	1
A								7420		74177	7404
B	74177		7400				7474	7410		74177	7400
C	74177		7474	7430				7410		74177	7438
D	7403		7403	7403	74177		74177				74H04
E	7403		7403	7403	7403		7403			74177	74H10

2ND CONTROLLER OPTION AND I/O REGISTERS 2 SEE MOB SYSTEMS DRG 2304-3 SHEETS 2 AND 4

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	SPACE ENVIRONMENT LABORATORY ERL ● NOAA ● BOULDER COLO	
APPROVALS / DRAWN	DATE	HFS. DIO I/O CARD LOGIC PC SECTION ADDITIONAL IC's
CHECKED		SCALE / SIZE C / DRAWING NO. HFS 006
		DO NOT SCALE DRAWING / SHEET 2 OF 2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



DIO BUS

RX P10A,B,C		FUNCTION
1	0	LSB
2	1	ADDRESS
3	2	
4	3	
5	4	
6	5	MSB
7	0	LSB
8	1	
9	2	DATA TO RX CONTROL MODULE
10	3	
11	4	
12	5	
13	6	
14	7	MSB
15	0	LSB
16	1	
17	2	DATA FROM RX CONTROL MODULE
18	3	
19	4	
20	5	
21	6	
22	7	MSB
23		ADDRESS STROBE
24		DATA STROBE
25		GROUND

TSG BUS

RX J8A,B,C	FUNCTION
1	TX ENABLE (L.P.)
2	RESET
3	RX DISABLE
4	TX KEY
5	ϕ1 — TX ϕ CODE
6	ϕ2 — TX ϕ CODE
7	ϕ3 RX ϕ CODE
8	A — FAST ATTN
9	B — FAST ATTN
10	TX ENABLE (HA)
11	GROUND
12	OVERLOAD — INTERRUPTS
13	RESET — INTERRUPTS
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	GROUND

FEP BUS

	FUNCTION
1	7 — FEP ADDRESS BITS
2	5 — FEP ADDRESS BITS
3	3 — FEP ADDRESS BITS
4	1 — FEP ADDRESS BITS
5	
6	
7	FEP MEM RESET ($\overline{FMR}$)
8	TSG BUSY/$\overline{DONE}$
9	GROUND
10	GROUND
11	FEP BUSY/$\overline{DONE}$
12	
13	
14	6 — FEP ADDRESS BITS
15	4 — FEP ADDRESS BITS
16	2 — FEP ADDRESS BITS
17	0 — FEP ADDRESS BITS
18	MEMORY SELECT (FMS)
19	FEP $\overline{START}$ ($\overline{FST}$)
20	FEP WRITE ENABLE (FW)
21	200 KHz (Φ_1)
22	100 KHz
23	200 KHz $\phi\phi$
24	200 KHz
25	$\overline{200\ KHz}$

INTERRUPT BUS

	FUNCTION		FUNCTION
1	GROUND	9	
2	FEP PWR FAIL	10	
3	FEP OVF	11	
4		12	
5		13	
6	TSG DONE	14	
7		15	
8			

DMA BUS

	FUNCTION
1	GROUND
2	DATA READY
3	RESET
4	INCREMENT
5	
6	FEP-ON FLAG
7	
8	
9	
10	15 — MSB
11	14
12	13
13	12
14	11
15	10
16	9 — OUTPUT DATA BITS FROM FEP TO INTDTA
17	8
18	7
19	6
20	5
21	4
22	3
23	2
24	1
25	0 — LSB
26	
27	
28	
29	
30	
31	
32	
33	+5V FOR FEP SIMULATOR
34	
35	
36	
37	GROUND

DIO +HSK BUS

HSK P2	FUNCTION		HSK P2	FUNCTION
1			2	
3	GND		4	32 — CHANNEL SELECT DATA IN FROM BUS
5	DATA STROBE		6	16
7	ADDRESS STROBE		8	8
9	B5 128 — CHANNEL SELECT DATA OUT TO BUS — ADC OUT		10	4
11	B6 64		12	2
13	B7 32		14	1
15	B8 16		16	6 — MUX INPUT, ADC OUTPUT, ADD. DECODER
17	B9 8		18	5
19	B10 4		20	4
21	B11 2		22	3
23	B12 1		24	2
25			26	1
27	B1 — ADC OUT		28	
29	B2		30	
31	B3		32	
33	B4		34	
35			36	
37			38	
39	OVERLOAD — INTERRUPTS		40	
41	RESET — INTERRUPTS		42	
43			44	
45	EOC		46	
47			48	
49			50	

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
± ± ±

APPROVALS	DATE
DRAWN JEJ	2/2/78
CHECKED	

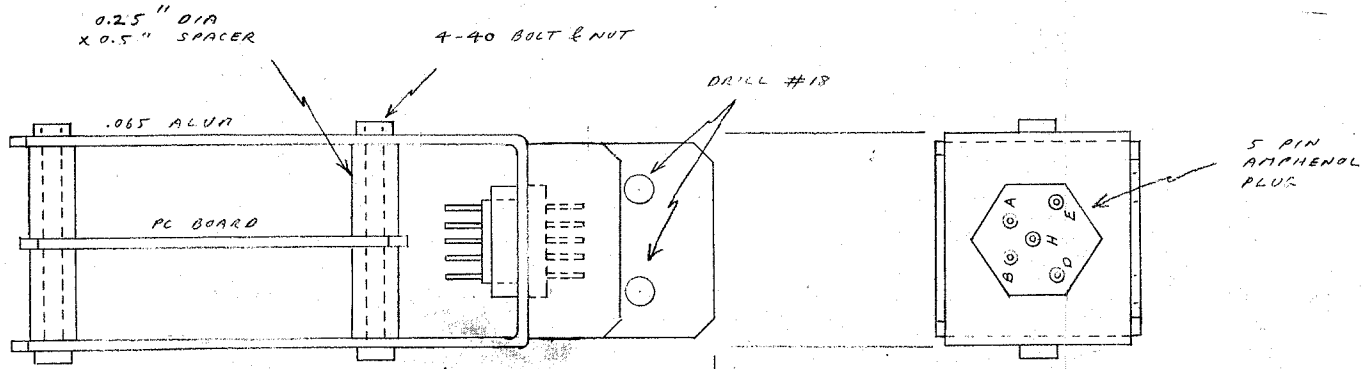
SPACE ENVIRONMENT LABORATORY
ERL ● NOAA ● BOULDER COLO

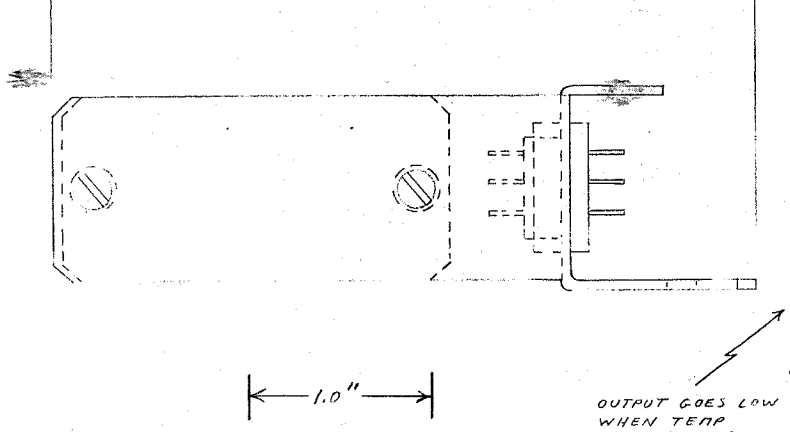
IONOSONDE BUS CONNECTIONS

SCALE	SIZE	DRAWING NO.
	C	008
DO NOT SCALE DRAWING		SHEET

A-2-4

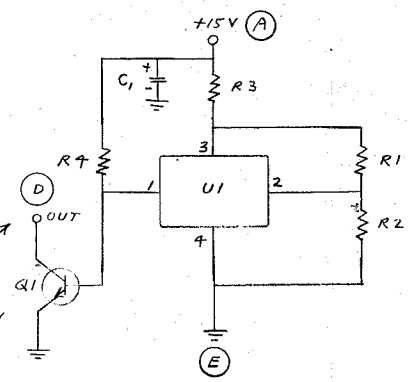
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	CIRCUIT DIAGRAM, PARTS LIST, MECH DRAWING REVISED.	4-4-79	
B	Q1 ADDED	6-27-79	
C	SENSOR OUTPUT NOTES REVISED	3-11-80	





CIRCUIT DIAGRAMS

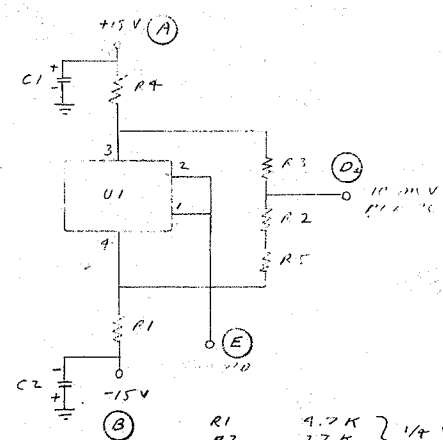
TC BOARD



OUTPUT GOES LOW WHEN TEMP EXCEEDS 100 °C

R1	28.0K ≃ 30 K SERIES TOTAL (ADJ. FOR TEMP.)	1/4 W 1% METAL FILM
R2	22.1K	
R3	7.5K	1/4 W 5% METAL FILM
R4	1.0 11	1/4 W 5% CARBON
C1	1.0 MF	SOLID TANTALUM
U1	NATIONAL SEMICONDUCTOR LX5700	
Q1	2N3904	

TM BOARD



R1	4.7K	1/4 W 5% METAL FILM
R3	2.7K	
R4	12 K	
R2, R5	≃ 4.5 K SERIES TOTAL, FOR TEMP ADJUST	1/4 5% OR 1% M.F.
C1, C2	1.0 MF	SOLID TANTALUM
U1	NATIONAL SEMICONDUCTOR LX 5700	

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN JJ	6-27
CHECKED	79

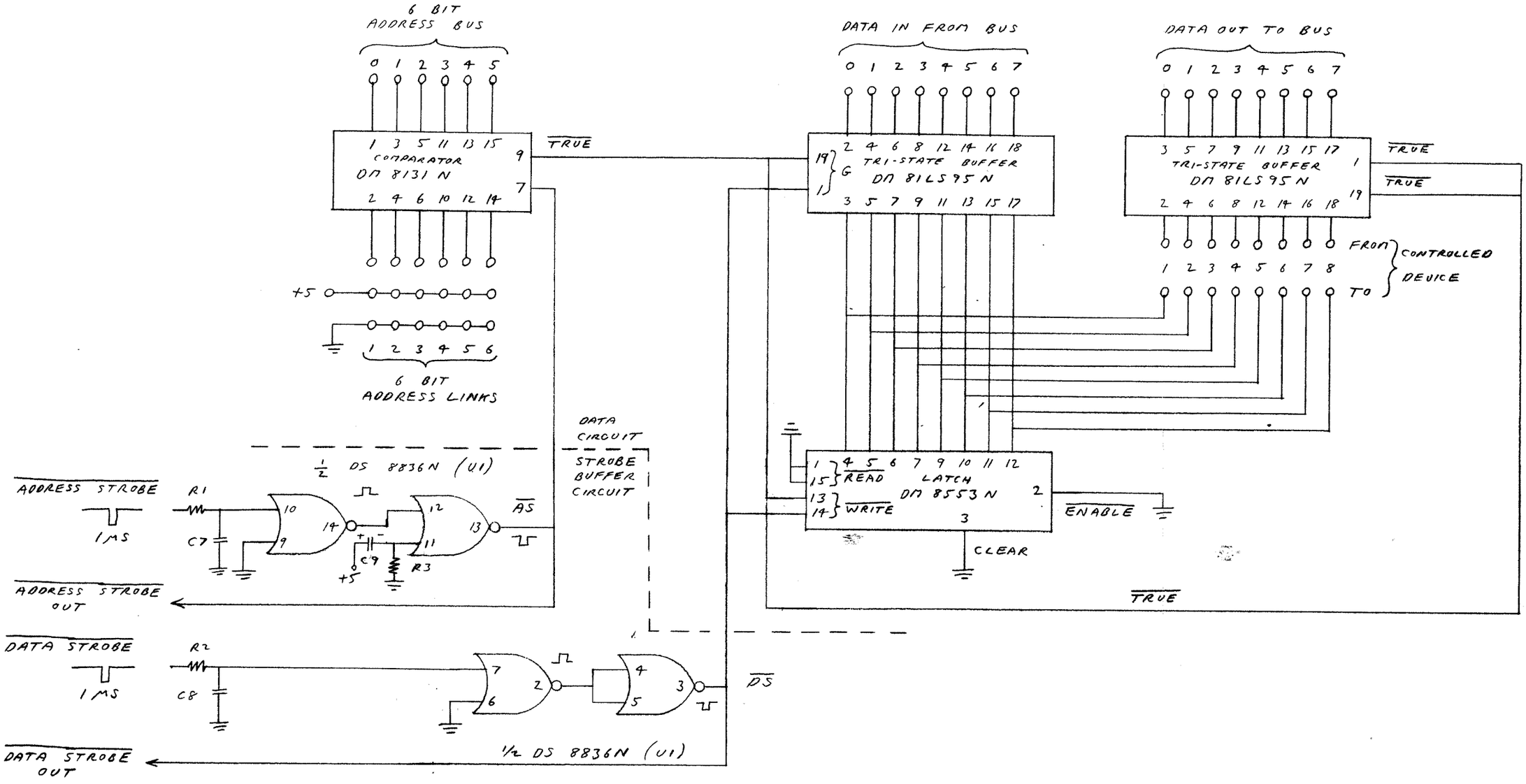
SPACE ENVIRONMENT LABORATORY
ERL ● NOAA ● BOULDER COLO

TEMPERATURE SENSOR

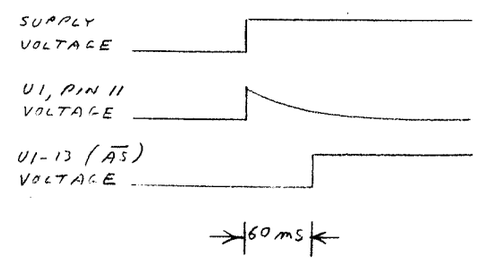
SCALE	SIZE	DRAWING NO.
	C	HFS-113

DO NOT SCALE DRAWING — SHEET

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



POWER ON RESET :



TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN	
CHECKED	

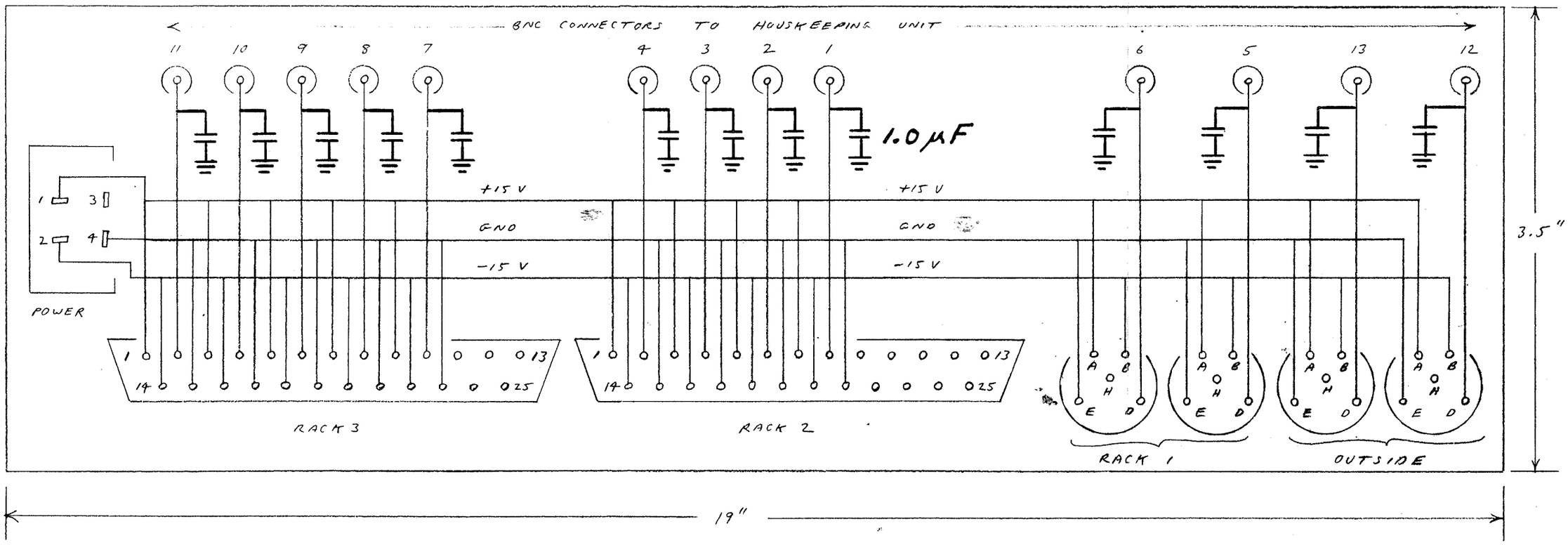
SPACE ENVIRONMENT LABORATORY
ERL ● NOAA ● BOULDER COLO

DIO STROBE BUFFER, DATA CIRCUITS, BLOCK DIAGRAM

SCALE	SIZE	DRAWING NO.
7-20-78	C	HFS-134

DO NOT SCALE DRAWING | SHEET

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	1 MF CAPS ADDED	8-19-81	J. J.



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DEC ± ANGLES ±		SPACE ENVIRONMENT LABORATORY ERL ● NOAA ● BOULDER COLO	
APPROVALS	DATE	TEMPERATURE MONITOR PANEL	
DRAWN JJ	12-8-77		
CHECKED		SCALE	SIZE C
		DRAWING NO.	IHF3-112
		DO NOT SCALE DRAWING	SHEET

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

P2
26 24 22 20 18 16
Mux Input Address
A1 A2 A3 A4 A5 A6

Bus Comparator
+5
DM 8131
B1 B2 B3 B4 B5 B6
Vcc STR
Gnd OUT
T6 T5 T4 T3 T2 T1
Wire Wrap Pins

DIO 33 (Hex) ⇒ 1 1-0 0 1 1

P2
Channel Select Out
1 2 4 8 16 32

81LS95 F

DIG RTN
ANA RTN
DIG RTN
MUX ADD OUT

MP6848
MULTIPLEXER ADDRESS DECODER
BREAK BEFORE MAKE CIRCUIT
48 CHANNEL MULTIPLEXER
MULTIPLEXER ADDRESS COUNTER/REGISTER
MUX INPUTS

MP6812
16 CHANNEL MULTIPLEXER
CNTR
OFF ADJ
12 BIT A/D CONV
S&H
TRI-STATE BUF
PROGRAMMER AND LOGIC CONTROL
PRECISION REF SUPPLY
MUX INPUTS

TO ANA RTN

P2
P2-7
Address STR
(½) DS8836
ADR STB
10uF
4.7KΩ

P2
P2-5
Data STR
(½) DS8836
DAT STB

DS8836

STANDARD SPS-30-5
[3A]
.01uF
+5 volts
10uF
DIG GD

LAMBDA LZD-22
[3B]
10uF
+15 volts
ANA COMMON
-15 volts
10uF

81LS95 A
Channel Select In
4 6 14 12 10 8
P2

P2
ADC Output Address
A1 A2 A3 A4 A5 A6
Bus Comparator
DM 8131
Wire Wrap Pins

DIO 34 ⇒ 1 1-0 1 0 0 (HEX)

81LS95 D
2048 ADC 27
1024 829
512 Output 31
256 33
P2
DATA ENBL

81LS95 E
128 ADC 9
64 11
32 Output 13
16 15
P2

(½) 7438
G
R1 2.2K
EOC
45 - P2

Connector P2

1		2	
3	GND	4	32 DIO DATA OUT
5	Data Strobe	6	16 Channel
7	Address Strobe	8	8 Select
9	B8 128 DIO DATA IN	10	4 In
11	B7 64	12	2
13	B6 32 ADC	14	1
15	B5 16 Output	16	A6 DIO ADDRESS OUT
17	B4 8 Channel	18	A5 Function
19	B3 4 Select	20	A4 Select
21	B2 2 Out	22	A3
23	B1 1	24	A2
25		26	A1
27	B1 2048 ADC	28	
29	B2 1024 Output	30	
31	B3 512	32	
33	B4 256	34	
35		36	
37	ANL OVL	38	
39	+15 OVL (Reset)	40	
41	EOC	42	
43		44	
45		46	
47		48	
49		50	

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		SPACE ENVIRONMENT LABORATORY ERL ● NOAA ● BOULDER COLO	
APPROVALS	DATE	HF Sounder Housekeeping ADC/MUX	
DRAWN [illegible]	9/24/75		
CHECKED		SCALE	SIZE D DRAWING NO. HFS 400
		DO NOT SCALE DRAWING	SHEET

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