HF RADAR MANUAL

VOLUME 6

Transmitter Power Amplifier

Prepared by

Instrument Development Group

Space Environment Laboratory

Environmental Research Laboratories

National Oceanic and Atmospheric Administration

Boulder, Colorado 80303

Original Issue: November 1978
Revision 1: April 1979
Revision 2: October 1979

IMPORTANT NOTICE

The voltages and stored energies in the high power transmitter under operating conditions are potentially LETHAL. Work carried out on this system with the cabinet door interlock defeated or particularly with transmitter or power supply panels removed must be carried out by experienced personnel taking all applicable safety precautions. The Space Environment Laboratory disclaims responsibility for safety under these conditions.

CONTENTS

LIST OF FIGURES

LIST OF DRAWINGS

TRANSMITTER POWER AMPLIFIER

1. GENERAL

The transmitter power amplifier rack contains two amplifier systems and miscellaneous control and filter systems. Figure 1 is an overall block diagram.

The whole amplifier system is linear (although keyed) and receives its RF input at the frequency to be transmitted, within the band 0.1-30 MHz, from the transmitter drive module in the low power RF system at a nominal +3 dBm level. This signal is first attenuated as required to control the output power level or to compensate for gain variations over the band by a 0-31 dB attenuator. This is selectable in 1 dB steps under DIO control. The signal is then passed to a commercial solid-state class A wide band amplifier (ENI A300). This is capable of a saturated power output of > 300 W over the range 0.3-35 MHz. The units used in the HF radar are modified by the manufacturer to provide > 100 W down to 0.1 MHz. The rated harmonic distortion in the 0.3-35 MHz range is < -35 dB for the second at 300 W and < -25 dB for the third at 250 W. These levels are too high for direct radiation from an antenna, and it is recommended that the amplifier always be driven at a level giving 200 W output or lower into its rated 50 Ω load. Basically the amplifier is capable of CW operation. To reduce its power consumption and dissipation, SEL has modified the amplifiers for keyed power supply operation when used with RF pulses. However, the amplifier may be keyed on continuously if CW or quasi-CW long pulse operation is desired.

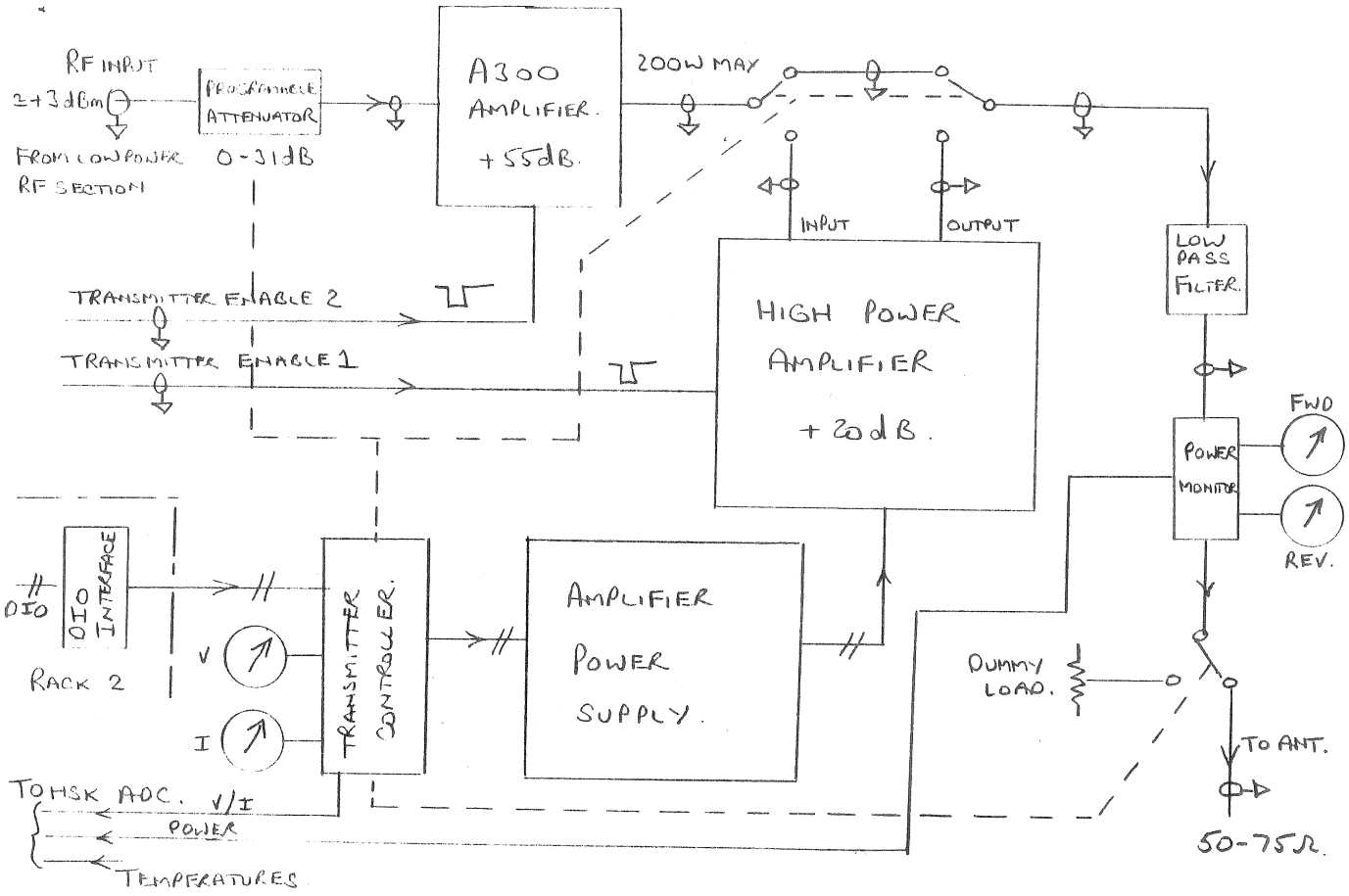
Coaxial relays permit the A300 output to be used directly if the second amplifier, a nominal 10 kW pulsed vacuum tube amplifier is not energized. Before reaching the output, the signal forward and reflected power is monitored by a wide band reflectometer bridge. The monitoring meters are driven by fast charge, slow discharge peak reading circuits to permit essentially correct readings under normal pulse conditions.

It should be noted that the meter on the A300 itself, which is also modified for peak reading operation, monitors only the voltage across the amplifier output, although it is calibrated in power into 50 Ω.

A low pass filter with a cutoff frequency of 35 MHz is used to attenuate out of band harmonics and minimize the possibility of interference to television receivers and other VHF telecommunications.

The second High Power Amplifier (HPA) is a keyed class A vacuum tube amplifier. It is capable of ≈ 10 kW linear output for 100 W of drive from the A300. The duty cycle is limited by plate dissipation considerations to about 4% on time. Less than 30 μs is required for the amplifier to be fully keyed.

FIGURE 1. TRANSMITTER POWER AMPLIFIER. RACK GENERAL BLOCK DIAGRAM.



The operation of this second amplifier is monitored closely by a transmitter controller which permits application of high voltage only if safety and other operating condition parameters are within preset limits. The controller provides computer control and monitoring of the high power amplifier.

The components of the system will now be described in more detail.

2. THE A300 SOLID-STATE POWER AMPLIFIER

The commercial manual for this unit should be consulted for specifications, descriptions of the design, and schematics. The unit is modified by SEL to permit keying of the power supplies and to provide peak power metering. Appendix 1 gives the details. The power supply keying is basically accomplished by switching the reference voltages of the integrated circuit regulators.

3. HIGH POWER AMPLIFIER AND POWER SUPPLY

Figure 2 shows the basic configuration of the high power amplifier. It is a push, pull class A amplifier using a cascode configuration to minimize coupling from the output back to the input of the amplifier. The operating conditions of the bottom pair of tubes is chosen to minimize grid loading. The grids are driven directly from the terminated secondary of a 50 Ω to 200 Ω balanced transformer. The most difficult problem in the design is that of the output transformer which must operate at the 10 kW level over the 0.1-30 MHz frequency range. It is very difficult to make a conventional transformer with tightly coupled windings to do this because the necessary voltage can only be sustained with magnetic materials whose high frequency losses are low if the electrical length of the windings is too long for the transformer to operate correctly at the high frequency limit. The only type of transformer fundamentally free of this limitation is the transmission line type due to Ruthroth (Ref. 1). Figure 3 shows the basic 4:1 impedance versions for inverting and noninverting configurations. At high frequencies, the balanced mode voltages in the equal length transmission lines are combined in series on the high impedance side and in parallel on the low impedance side. Where necessary, the line is wound on a magnetic core to suppress common mode currents. At low frequencies, it is desirable that a common core is used to balance the flux due to the overall common mode anode curent pulse and for the system to revert to a normal transformer. This can be achieved by correctly assigning the number and sense of the transmission line windings on the common core. For convenience, the lower winding in the phase inverting half of the transformer is wound on the outer legs of a double E core structure, since it requires half the flux turns product of the two upper windings. The lower section of the nonphase inverting half has no common mode voltage and serves only to equalize delays at high frequencies. This section of line is air wound. The transmission line used is nominal 300 Ω impedance. The transformer operates satisfactorily with nominal load resistors of 50 or 75 Ω. The transmission line type output transformer offers no inherent DC isolation. The power supply system is therefore arranged so that the positive high voltage terminal is basically at ground. However to allow for current monitoring and ground fault protection, the positive return is isolated for low voltage and the RF output is coupled through low voltage block mica capacitors. The detailed schematic of the high power amplifier is given in HFS 500 and its power supply in HFS 501 and 502.

The major practical complications present in the transmitter are the arrangements for the high voltage isolated keying and bias supplies. Keying is accomplished by a 350 V, 20 A switching Darlington

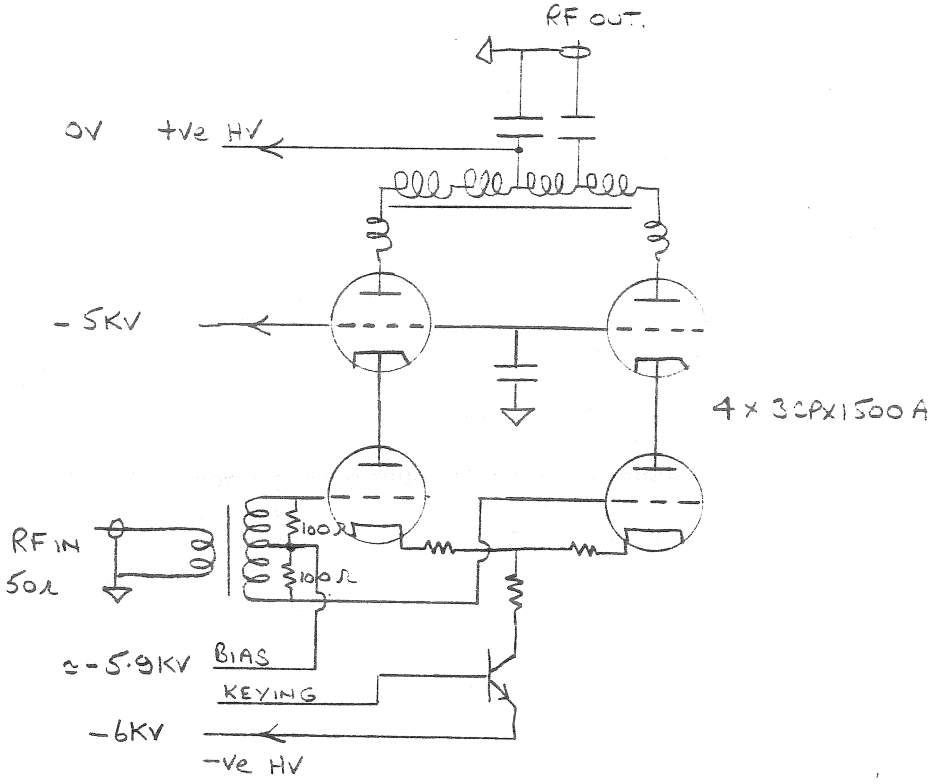


FIGURE 2. GENERAL ARRANGEMENT
HIGH POWER AMPLIFIER

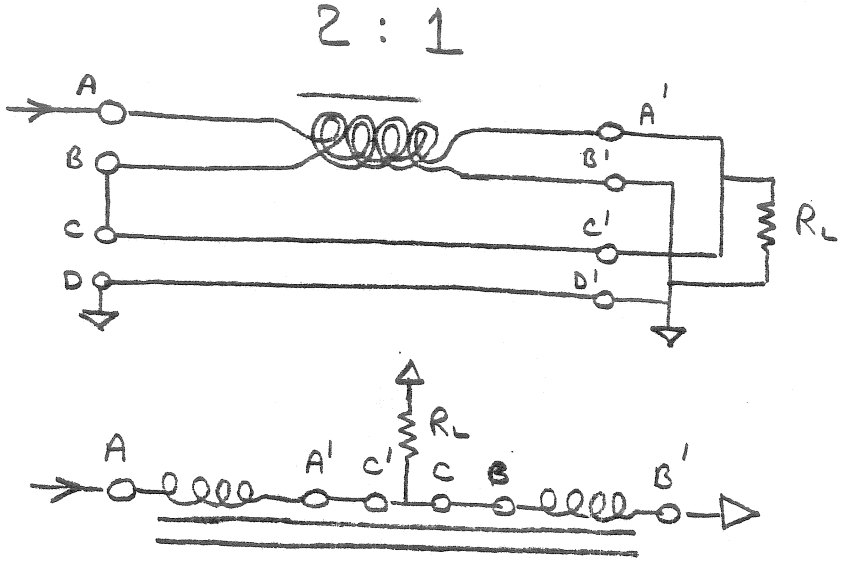


FIG 3(a) NON INVERTING TRANSMISSION LINE TRANSFORMER AND LF EQUIVALENT.

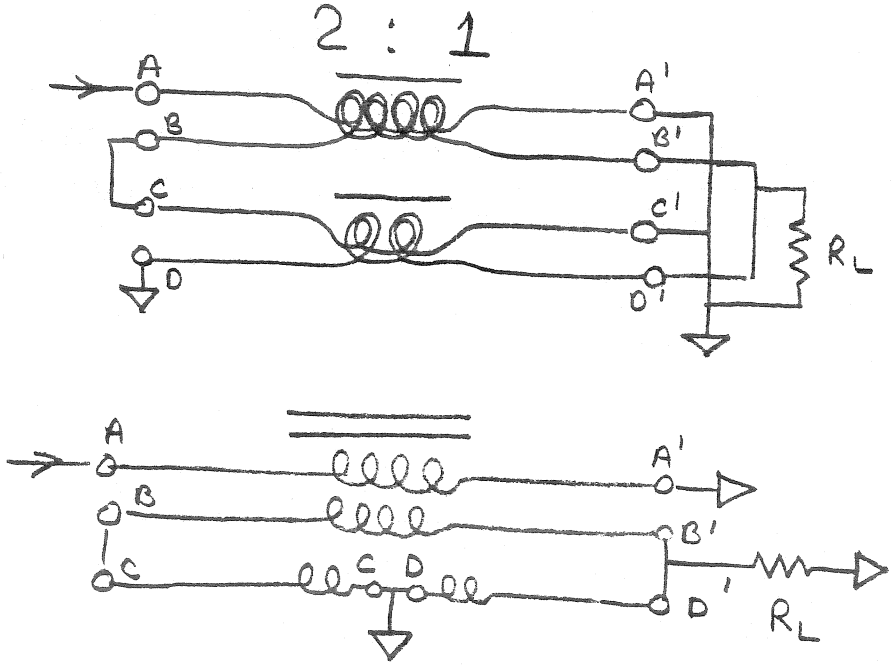


FIG 3(b) INVERTING TRANSMISSION LINE TRANSFORMER AND LF EQUIVALENT.

transistor Q8 in the cathode circuit of the amplifier. The on current is controlled and balanced by resistors R69, R70, and R71 and set by the variable 0-150 V positive bias supply. Control of the keying is accomplished across the HV interface by the IR optical coupler formed by the LED D12 and photo transistor Q5. Both these devices have narrow transmission angles obtained by using lenses and a current transfer ratio of > 0.4 is obtained for ≃ 0.5 inch spacing which because of the insulated construction of the lamp is adequate to stand off the transmitter HV. The LED is pulsed to ≃ 100 mA by a complementary emitter follower driver. Monostables IC2 in the driver (schematic HFS 504) limit the possible maximum pulse length to 400 μs and the period to a minimum of 9 ms to prevent damage to the transmitter by external keying line faults.

The positive bias supply for the grids of the lower pair of tubes is provided by an isolated 150 V winding on the heater transformer. Half wave rectification is used from a variable autotransformer which sets the output voltage. A separate rectifier provides an independent fixed supply for the transistors in the keying circuit.

The bias for the grids of the upper pair is supplied by a varistor stabilizer string which provides ≃ 1200 V positive with respect to the power supply -ve line.

Revised: December 27, 1979

4. TRANSMITTER CONTROLLER

The transmitter controller card contains the logic necessary to provide computer control and fault monitoring of the transmitter power amplifier system. The control logic assumes that the A300 amplifier is powered when the rest of the system is powered. If no action is taken to turn-on the high power amplifier, the system will run in the low power mode with the A300 output connected either to the antenna or to the dummy load depending on the control bit for this relay on DIO address 30.

The schematic of the controller is shown in drawing HFS 503. Basic on/off control is exercised through bits 0, 1, 2, and 3 of DIO address 30. As shown in Figure 1, the actual DIO interface is located in rack 2 and the DC control and status monitoring lines brought through a multiway cable to rack 3 where they are RF filtered before connecting to the controller.

Three classes of fault are recognized by the controller which takes local action to shut down the high power transmitter as well as providing status reading to the computer to indicate the type of fault and an interrupt line which can be employed to change the course of the operating program if desired.

The classes of faults are:

1. Temperature or cooling faults

    (a) Final tube cooling air flow low

    (b) Final tube cooling air exit temperature high.

Both these faults completely inhibit turn-on, including tube filaments, or if the transmitter is operating, cause a complete shut-off of power.

2. Potentially lethal faults

    (a) Ground current fault

    (b) Interlock violated.

These faults inhibit high voltage turn-on or, if occurring during operation, turn off the high voltage and dump the charge on the high voltage capacitors in $\simeq$ 100 ms.

3. Operating faults

These faults do not inhibit turn-on for an initial 1 second period. During operation after this period, they cause the high voltage to be turned off.

(a) Peak current in excess of normal

(b) Average current in excess of normal

(c) High voltage above or below normal value.

Faults 1(a), 1(b), and 2(b) are presented to the controller as shorts to ground and are buffered by logic gates U1A, B, and C. Ground current faults are sensed across the 10 Ω resistor which connects the positive HV return to ground, by comparator U2A. This is set at a threshold of 120 mV corresponding to a current of 12 mA. A filter time constant of 1 ms avoids transient noise problems.

The mean and peak currents are sensed by differential integrators U3B and U2B with time constants of 160 ms and 100 μs, respectively. Comparators U3C and U3A check the mean value from U3B and the peak value held by the fast charge slow discharge circuit U2C. The limits set are approximately 0.5 A and 20 A, respectively. U4A amplifies slightly and conditions the high voltage monitored from the bottom of the power supply bleeder resistor. Comparators U4B and C monitor over and under voltage conditions, respectively. The limits are 5 kV and 8 kV, respectively.

All faults are latched by SR flip-flops U5, 6, 7, and 8. The faults are OR'd, both from the latches and directly in the three groups by U9A, B, and U12, respectively. Outputs from the latches provide status flags to the Interdata via the DIO bus.

Analog outputs from the average and peak current sensors and the high voltage monitors are indicated by front panel meters and made available to the housekeeping ADC.

Figure 5 shows the computer turn-on sequence required via DIO address 30. Initially a reset is required via bit 2 to ensure that all fault latches are reset and via monostable U20, X20 and latched relay K3 (drawing HFS 501) via Driver E, make 24 V power available for the filament, HV and antenna changeover relays.

Filament power may then be applied by taking bit 0 low provided no faults in group 1 are present. This action starts the 90 second

monostable U17, X17 which inhibits HV turn-on. After the completion of this cathode warm-up delay and providing no group 2 faults are present, HV may be applied by first resetting to clear any fault latches and triggering the fault hold-off delay of 2 seconds U14, X14. This latter inhibits group 3 faults to permit the HV low fault to be bypassed. A further set pulse must be sent after 1 second to reset the HV low latch before the termination of the fault hold delay. Closing of the HV contactors automatically switches the amplifier bypass relays to connect the high power amplifier between the A300 and the antenna and also applies power to the LED driver which optically couples the transmit enable pulses to the transmitter cathode keying circuit.

Transmitter operation is visually monitored with the LED front panel indicators shown in drawing HFS-503A. The indicators are divided into five groups: control, relay, status, fault, and dB attenuation. The following explanations tell what condition is occurring when the LED indicator is lit.

1. Control

   FIL OFF: The filaments are commanded to be off (TTL high input).

   HV OFF: The high voltage supply is commanded to be off (TTL high input).

   DL: The antenna-dummy load relay is commanded to connect the dummy load (TTL high input).

   SET: The set pulse (TTL low input) is occurring.

   RESET: The reset pulse (TTL low input) is occurring.

2. Relay

   FIL OFF: The filament relay is open causing the filament to be off.

   HV OFF: The high voltage relay is open causing the high voltage to be off.

   DL: The antenna-dummy load relay is open causing the transmitter to be switched to the dummy load.

   DUMP: The dump relay is closed discharging the high voltage capacitors.

   RV RES: A latching relay is being energized for one second to enable the +24 volt supply after a power interruption.

3. Status

   HV HOLD: The high voltage is being held off for a 90 second filament warm-up period.

   FAULT HOLD: Voltage and current abnormalities are being ignored for two seconds after high voltage turn-on to allow the power supply time to stabilize.

   RV OFF: The +24 V relay voltage is off until a reset pulse occurs, following a power interruption.

   INTRPT: A fault has occurred and an interrupt (TTL low output) is being sent to the computer.

4. Fault

   INTLK: The transmitter cabinet door interlock has been violated.

   GND: A ground fault has occurred.

   TEMP: The transmitter exhaust air is too hot.

PRES: The transmitter cooling air flow has stopped.

PK I: Peak current has exceeded 20 A.

AV I: Average current has exceeded 0.5 A.

HV MAX: The high voltage has exceeded 8.0 kV.

HV MIN: The high voltage has dropped below 5.0 kV.

5. dB Attenuation

The attenuator relays are energized adding 1, 2, 4. 8, or 16 dB attenuation to the transmitter drive level.

A wiring diagram for the connections inside the transmitter controller box is shown in drawing HFS-503B. The chassis connectors listed in the left column are located at the bottom of the box. Each line from the chassis connectors to the PC board passes through a low pass filter consisting of a 1500 pF feedthrough capacitor and two ferrite beads. Function and DIO address are listed for each line. The LED indicator panel is connected to the PC board through a 34-line ribbon cable which connects P3 to P4. For testing, the controller PC board can be accessed by removing the front panel.

Transmitter Controller Test Procedure:

A. Function Tests With High Voltage Disabled

1. With the PC board installed, make sure that the edge connectors P1 and P2 make proper contact with their sockets J1 and J2.

2. The indicator panel should be connected so that the ribbon cable between P3 and P4 has no 180° twists when the panel is right side up.

3. Connect all plugs and sockets at the bottom of the controller.

4. Connect the control module to the DIO simulator and connect the simulator to +5 V.

5. With the transmitter disconnected from its power supply and the high voltage disabled, turn on the power supply main circuit breaker.

6. Set the DIO simulator address to 30 (Hex), data to FF, address strobe low, and data strobe low. (In these tests, it is convenient to leave the strobes low so that data can be changed without requiring a strobe.) The indicator panel will come up in a random pattern.

7. Set the address to 31 and data to FF. All attenuation indicators should go out. Switch data bits 0, 1, 2, 3, and 4 low sequentially. The indicators for 1, 2, 4, 8, and 16 dB should go on sequentially.

8. Set the address to 30 and data to FF, and switch RESET (bit 2) momentarily low. All fault indicators should be out while RESET is low.

When RESET returns high, the HV MIN indicator should go on, since there is no high voltage present. If any other fault indicators go on, the transmitter status is abnormal must be corrected before further testing can be done.

9. Switch RESET low. While RESET is low, the following pattern should be indicated.

CONTROL:	FIL OFF HV OFF DL RESET
RELAY:	FIL OFF HV OFF DL RV RES
STATUS:	FAULT HOLD
FAULT:	No Indications
dB ATTENUATION:	Whatever setting at which the attenuators were left.

10. Switch RESET high again. The following changes should occur on the front panel:

CONTROL:	RESET - Goes out immediately
FAULT:	HV MIN - Goes on immediately
RELAY:	RV RES - Goes out immediately or one second after the RESET low transition, whichever occurs later
STATUS:	FAULT HOLD - Goes out immediately or two seconds after the RESET low transition, whichever occurs later.

11. Switch the filaments on (bit 0 low). The filament relay should close and the amber filament pilot light should go on. The indicator panel should show the following:

CONTROL:	FIL OFF - Goes out immediately
RELAY:	FIL OFF - Goes out immediately
STATUS:	HV HOLD - Goes on immediately, then goes out after 90 seconds.

12. After the STATUS: HV HOLD indicator has gone out, turn on the high voltage, using RESET followed within one second by bit 1 low. The following indications should occur:

CONTROL:	HV OFF - Goes out immediately
RELAY:	HV OFF - Goes out immediately
	RV RES - Goes out one second after RESET low transition
STATUS:	FAULT HOLD - Goes out two seconds after RESET low transition.

The high voltage relay should close and the red high voltage pilot light should go on. When the two second FAULT HOLD expires, the high voltage relay opens because the voltage is below the lower limit. For normal operation, the HIGH VOLTAGE ON command must be followed by a SET command (bit 3 low pulse). Without the SET, the high voltage will turn off when the FAULT HOLD expires.

13. Switch from antenna to dummy load (bit 4). Bit 4 high selects the dummy load, which is indicated by:

CONTROL:	DL
RELAY:	DL

14. With the filaments and high voltage turned off, check the zeroes on the high voltage, peak current, and average current meters. Errors are corrected as follows:

High Voltage:	Adjust the ratio of R19 and R20, keeping their sum constant
Peak and Average Current:	Adjust the ratio of R9 and R10, keeping their sum constant.

B. Function Tests With High Voltage Enabled

1. Connect the transmitter to the power supply, using a variac in the high voltage transformer primary circuit to control the voltage. Set the variac to zero voltage. Set the transmitter bias for zero current.

2. Turn on the main power.

3. Turn on the filaments.

4. After the high voltage hold expires, turn on the high voltage (RESET, HV, SET, sequence). The high voltage will go off after two seconds because of the HV MIN fault.

5. Increase the variac setting to about 20% of full voltage and again turn on the high voltage. Compare the front panel reading with a direct measurement of the voltage. The high voltage should again turn off after 2 seconds.

6. Continue increasing the variac setting until the voltage is within the allowable range.

7. When the voltage is within the allowable range, it should stay on. Compare the front panel reading with the direct measurement. Accuracy should be within $\pm$ 5%.

8. When the transmitter is operating normally into the antenna with no attenuation, all front panel LED indicators will be out.

C. Fault Simulations

1. Turn on the transmitter with the HV at 7 kV, average current at zero, antenna selected, and no attenuation. Under these conditions, all indicators should be out.

2. Interlock Fault. Open the back door of the cabinet, or otherwise open the interlock switch momentarily. The high voltage should go off and the indicator panel should show:

RELAY:	HV OFF DUMP
STATUS:	INTRPT
FAULT:	INTLK HV MIN

The HV MIN fault occurs as the high voltage drops following the interlock fault. All faults produce an interrupt. Interlock and ground faults cause a dump. When a dump occurs, the HV meter should instantly drop to zero.

3. Ground Fault. With the transmitter operating as before, push the red ground fault simulator button at the back of the transmitter power supply. The indicator panel should show:

RELAY:	HV OFF DUMP
STATUS:	INTRPT
FAULT:	GND HV MIN

4. Temperature. Disconnect the temperature sensor from the back of the power supply. Both the filament and high voltage relays should open and the indicator panel should show:

RELAY:	FIL OFF HV OFF
STATUS:	INTRPT
FAULT:	TEMP

This procedure tests only the transmitter controller. To test the temperature sensor, a local heat source must be applied to the transducer inside the transmitter at the air exhaust. The sensor output should go low at 100°C.

5. Pressure. Disconnect the pressure sensor from the back of the power supply. Both the filament and high voltage relays should open and the indicator panel should show:

RELAY:	FIL OFF HV OFF
STATUS:	INTRPT
FAULT:	PRES

To test the pressure sensor, momentarily interrupt the transmitter exhaust air flow which should cause the sensor output to go low.

6. High Voltage Limits. Turn on the high voltage to 6 kV. Slowly redice the variac output. At 5 kV, the HV should go off and the indicator panel should show:

RELAY:	HV OFF
STATUS:	INTRPT
FAULT:	HV MIN

After HV shutoff, the HV meter should drop slowly, since there is no dump.

To avoid the danger of increasing the voltage to 8 kV, the upper limit is simulated by applying a voltage across the high voltage sensing resistor, with the transmitter power supply off. The simulated fault should occur when the front panel meter reaches 8 kV, and the indicator panel should show:

RELAY:	HV OFF
STATUS:	INTRPT
FAULT:	HV MAX

7. Peak and Average Current. With both filaments and high voltage off, connect a power supply across the 0.1 ohm current sensing resistor. Increase the current until the indicator panel shows that the 0.5 A maximum average current has been exceeded as follows:

RELAY:	HV OFF
STATUS:	INTRPT
FAULT:	AV I

The 20 A required to test the peak current limit must be applied momentarily or the resistor may be overheated. The fault is indicated as follows:

RELAY:	HV OFF
STATUS:	INTRPT
FAULT:	PK I.

D. Flag Checks

1. Each front panel indicator is also flagged to the DIO. Operate the transmitter so that each indicator at some time displays both the on and off condition. Check the flag addresses 30, 31, 32, and 35 to see that the corresponding LED indicator on the DIO simulator box displays the same condition as the indicator panel.

PARTS LIST — Transmitter Controller — MODULE

LABEL	PART NAME	DESCRIPTION
R1	Resistor	1 K 1/4 W 5% Metal Film
R2	"	4.7 K " " " " "
R3	"	1 K " " " " "
R4	"	11.5 K 1/4 W 1% Metal Film
R5	"	4.7 M 1/4 W 5% Carbon
R6-R7	"	10.0 K 1/4 W 1% Metal Film
R8*	"	11.5 K
R9*	"	162 Ω
R10*	"	40.2 Ω
R11	"	4.7 M 1/4 W 5% Carbon
R12*	"	162 K 1/4 W 1% Metal Film
R13	"	162 K " " " "
R14-R15	"	4.02 K " " " "
R16-R17	"	10.0 K " " " "
R18	"	9.76 K " " " "
R19*	"	5.62 K " " " "
R20*	"	8.25 K " " " "
R21	"	40.2 Ω " " " "
R22	"	162 Ω " " " "
R23	"	100 K " " " "
R24	"	1.00 K " " " "
R25	"	39.2 K " " " "
R26	"	10 K 1/4 W 5% Metal Film
R27	"	1.0 K " " " "
R28	"	2.00 K 1/4 W 1% Metal Film
R29	"	3.00 K " " " "
R30	"	10.0 K " " " "
R31	"	2.21 K " " " "
R32	"	2.43 K " " " "
R33	"	604 Ω " " " "
R34	"	2.00 K " " " "
R35-R56	"	220 Ω 1/4 W 5% Metal Film
R57**	"	2.2 Ω 1/4 W 5% Carbon
R58**	"	7.5 M " " "
R59**	"	1.0 M " " "
R60-R62	"	1.0 K 1/4 W 5% Metal Film
R63-R67	"	470 Ω " " " "
R68	"	120 Ω 1/2 W 5% Carbon
R69-R70	"	62 Ω " " "
R71	"	82 Ω " " "
R72	"	47 Ω " " "
R73	"	2.2 K 1/4 W 5% Metal Film
C1-C3	Capacitor	0.1 µF Monolithic
C4	"	1500 pF Plastic
C5-C8	"	1.0 µF Monolithic
C9	"	0.01 µF Ceramic Disc
C10-C13	"	1.0 µF Monolithic

Added: December 27, 1979

PARTS LIST — Transmitter Controller — MODULE

LABEL	PART NAME	DESCRIPTION
C14-C31	"	0.1 µF Monolithic
C32	"	1.0 µF "
C33	"	10 µF 35 V Tantalytic
C34	"	1.0 µF Monolithic
C35-C37	"	0.01 µF Ceramic Disc
C38-C40	"	4.7 µF 25 V Tantalytic
C41	"	47 µF 20 V Tantalytic
C42	"	1500 pF Plastic
C43	"	1.0 µF Monolithic
D1-D2	Diode	HP 2800
D3-D29	LED	Monsanto MV 5023
D30	Zener Diode	Motorola 1N4563, 6.8 V, 50 W
Q1-Q5	Transistor	Motorola MJE340
U1	Quad NAND	7400
U2-U4	Quad OP Amp	National Semiconductor LM 324
U5-U8	Quad NAND	7400
U9	Dual 4 Input NAND	7440
U10-U11	Hex Buffer	7407
U12	8 Input NAND	7430
U13	Hex Inverter	7406
U14	Timer	Signetics NE 555
U15	Quad NOR	7402
U16	Hex Inverter	7406
U17	Timer	NE 555
U18	Quad NAND	7400
U19	Hex Buffer	7407
U20	Timer	NE 555
U21	Quad NOR	7402
U22	Hex Buffer	7407
F1-F59	Filter	1000 pF Feedthrough Capacitor
J1-J2	Socket	60 Pin Amphenol 261-10030-2
P1-P2	Plug	Part of PC Board B1
P3	Plug	34 Pin Wire-Wrap
J10	Plug	50 Pin Amp 200277-1
P11	Socket	5 Pin Amphenol
J12	Plug	6 Pin Jones
J13	Plug	9 Pin Amphenol
J14	Plug	9 Pin Amphenol
J15	Plug	6 Pin Jones
J16	Socket	BNC Panel
B1	PC Board	7.30" x 9.40" Double Sided
CB1	Chassis Box	10" x 12" x 3" Alum

Added: December 27, 1979

5. POWER MONITOR

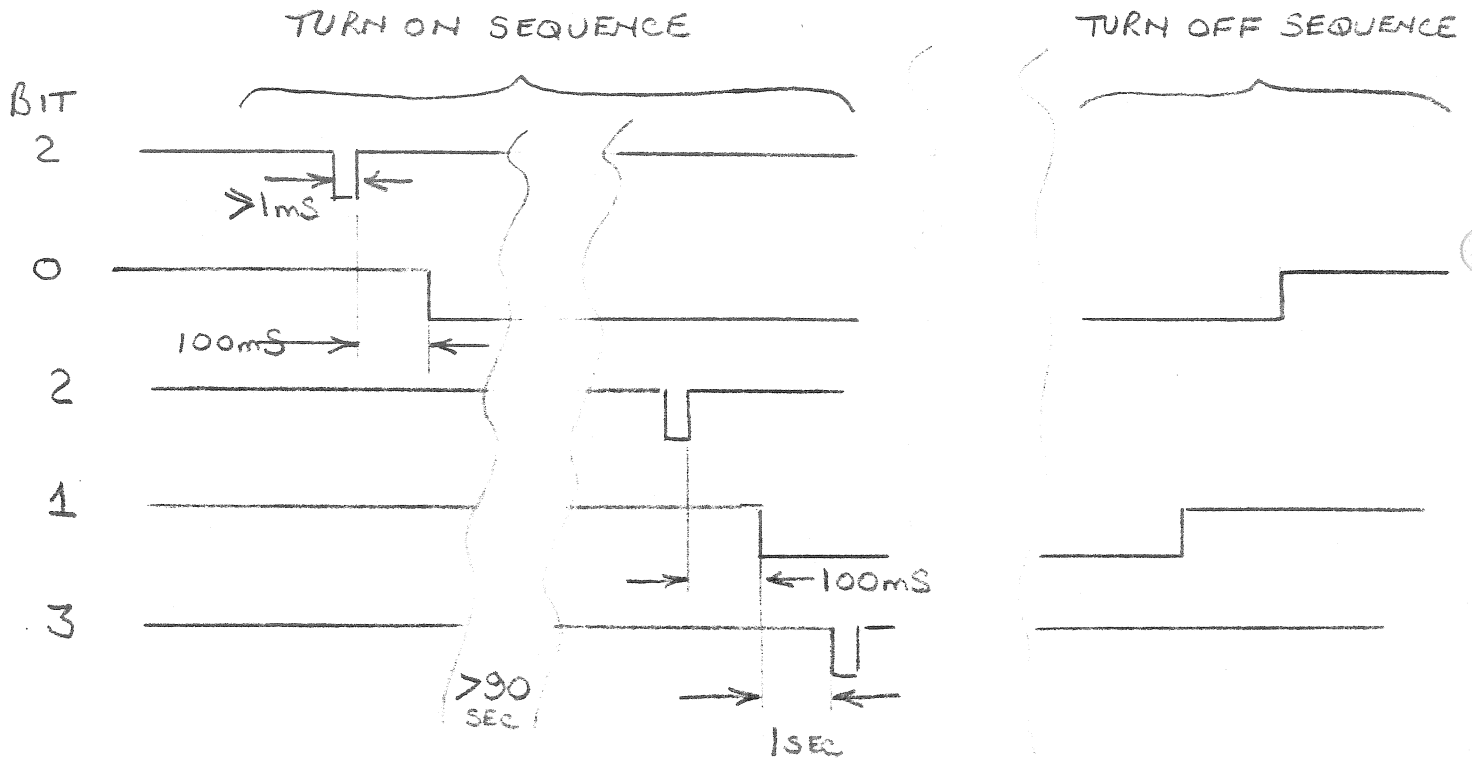
The power monitor circuit is shown in drawing HFS 505. A standard reflectometer bridge using a center tapped current transformer and resistive voltage sensing provides rectified voltages proportional to forward and reverse power. These are passed to fast-charge slow-discharge peak sensing buffers which provide output voltages for the front panel meters and also for monitoring via the housekeeping ADC. A separate resistive voltage divider provides a scope monitor point for the RF envelope and a peak reading rectified output for computer monitoring.

The reflectometer is balanced for a nominal 50 Ω load. The frequency response at both ports is within $\pm$ 1 dB over the frequency range 0.1-30 MHz. The balance is better than -30 dB over the same frequency range. The system is calibrated at a nominal 0.5% duty cycle.

HP. TRANSMITTER ON/OFF DIO TIMING SEQUENCE.

DIO ADDRESS 30_{16} LSB

0	FILEMENT ON/OFF
1	HV ON/OFF
2	RESET
3	SET.



NOTE TIME NOT TO SCALE

FIGURE 5.

6. LOW PASS FILTER

The schematic of the filter is in drawing HFS 506. It is a three section Zobel filter with m derived end sections. In a 50 Ω system, the filter is < 1 dB down at ≈ 30 MHz, 3 dB down at 33 MHz, 15 dB down at 35 MHz, > 60 dB down at 40 MHz, and > 55 dB down at > 40 MHz.

7. TRANSMITTER POWER AMPLIFIER PERFORMANCE AND OPERATION

Test data for the power amplifier are shown in Figure 4. At low frequencies (< 300 kHz) and at low levels giving linear operation (< 5 kW), the frequency response of the overall system is primarily controlled by the A300 amplifier. The loss of output power can be compensated to some extent by profiling the drive level to the A300 with the input attenuator, but saturation occurs in both the A300 and in the output transformer of the High Power Amplifier at a little below 10 kW output. The response at high frequencies is predominantly controlled by the output transformer in the High Power Amplifier. Curve 2 is typical of overall linear operation for frequencies > 300 kHz. The input attenuator default setting is selected so that the mid band power output is ≈ 10 kW into 50 Ω. The difference between curves 2 and 3 represents, at low frequencies, the A300 rolloff, and at high frequencies the effect of grid circuit impedance variations at the input to the High Power Amplifier. Although the overall frequency response is not as ideal as might be desired, the performance is in practice quite adequate for normal sounding applications.

An important consideration in amplifiers for this kind of application is their performance with the nonideal load presented by a typical wide band sounding antenna. The VSWR of antennas is seldom as good as 2:1 and may be much worse even at the transmitter end of a long transmission line. The output impedance of the A300 is less than 50 Ω, and its distortion changes little with a wide range of load impedances.

However, the High Power Amplifier is essentially a constant current source. The output power rises as the load impedance is increased until the pk-pk voltage swing becomes limited by saturation in the output tubes. In this amplifier, this has been designed to occur at > 3 times the nominal 50 Ω load impedance. It is important in practice not to run into saturation because the third harmonic distortion will rise very rapidly and cause unnecessary interference to other users of the spectrum. If the antenna impedance variations are such that saturation occurs, then the drive level should be reduced by increasing the input attenuator setting. Advantage can be taken of this "headroom" that the design provides to give greater power outputs at specific frequencies where the load impedance can be closely controlled to the order of 150 Ω. 30 kW or more should be available at low distortion. The nominal drive level at mid band is such that the plate current is nearly fully modulated. Thus it is not possible to get more power into the nominal or lower load impedances by increasing the drive without large and undesirable increases in distortion. The oscilloscope monitor point on the power monitor can be used to inspect the RF waveform for distortion.

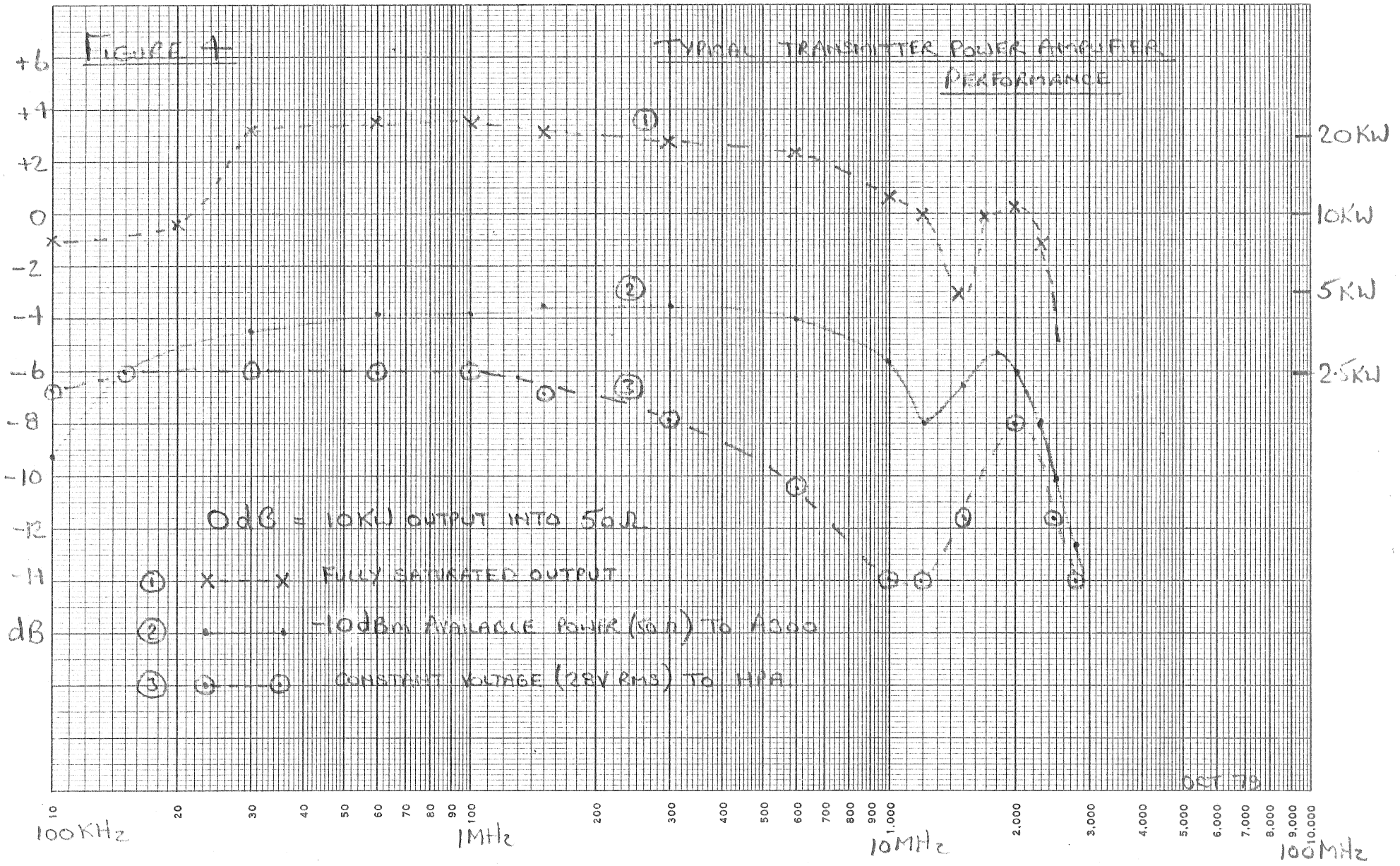


FIGURE 4
TYPICAL TRANSMITTER POWER AMPLIFIER PERFORMANCE
+6
+4
+2
0
-2
-4
-6
-8
-10
-12
-14
dB
20KW
10KW
5KW
2.5KW
0dB = 10KW OUTPUT INTO 50Ω
① FULLY SATURATED OUTPUT
② -10dBm AVAILABLE POWER (50Ω) TO A300
③ CONSTANT VOLTAGE (28V RMS) TO HPA
OCT 78
10
20
30
40
50
60
70
80
90
100
200
300
400
500
600
700
800
900
1,000
2,000
3,000
4,000
5,000
6,000
7,000
8,000
9,000
10,000
100KHz
1MHz
10MHz
100MHz
Frequency in Cycles per Second

APPENDIX 1

MODIFICATION OF THE A300 AMPLIFIER

1. Power Supply Switches

The amplifier is used primarily as a pulse amplifier. Therefore it is reasonable to switch on and off the power supply to reduce heat dissipation. The rise and fall time should be not much longer than 100 microseconds. The amplifier is built out of eight 40 W modules. Each module has its own power supply. The output voltage of each power supply is regulated by an IC 723 (see Figure 1). The resistors R23, R39, R49; R28, 38, 48; R27, 37, 47; R23, 33, 43; R24, 44; R26, 36, 46; R21, 31, 41; R22, 32, 42 determine the value of the output voltages.

It is possible to switch the power supplies on and off easily at Pin 9 of the IC 723, Figure 2 and Figure 3. When this point is connected to ground, the output voltage is zero. This can be done with the transistor 2N2219, Figure 1. A low on the base of the transistor switches the transistor off, the diodes 1N4153 are switched off, and the power supply is switched on. A high on the base causes a voltage of about 0.7 V on Pin 9 of the regulator 723, so the power supplies are switched off.

To make the rise time faster, the capacitance C21, 22, 23, 24, 26, 27, 28, 29 must be reduced from 50 microfarads to 4.7 microfarads.

The a-c current through the capacitance may not be higher than the specification.

$$\frac{dv}{dt} = \frac{i}{c}$$

$$i = \frac{27.0}{100.10^{-6}S} \cdot 4.7\ 10^{-6}F = 1.27\ A.$$

The duty cycle is $\frac{\pi}{f} = \frac{200.10^{-6}}{5.10^{-3}} = 0.04.$

The average current is $(1.27\ A) \cdot (0.04) \approx 50$ mA. According to the specifications of the used capacitance, the maximum ripple voltage can be 10 V at 200 Hz. The impedance of the capacitance

$$\frac{1}{2\pi\ fc} = 169\ \Omega.$$

Therefore the rms current $= \frac{U}{R} = \frac{10}{165} \approx 60$ mA is possible.

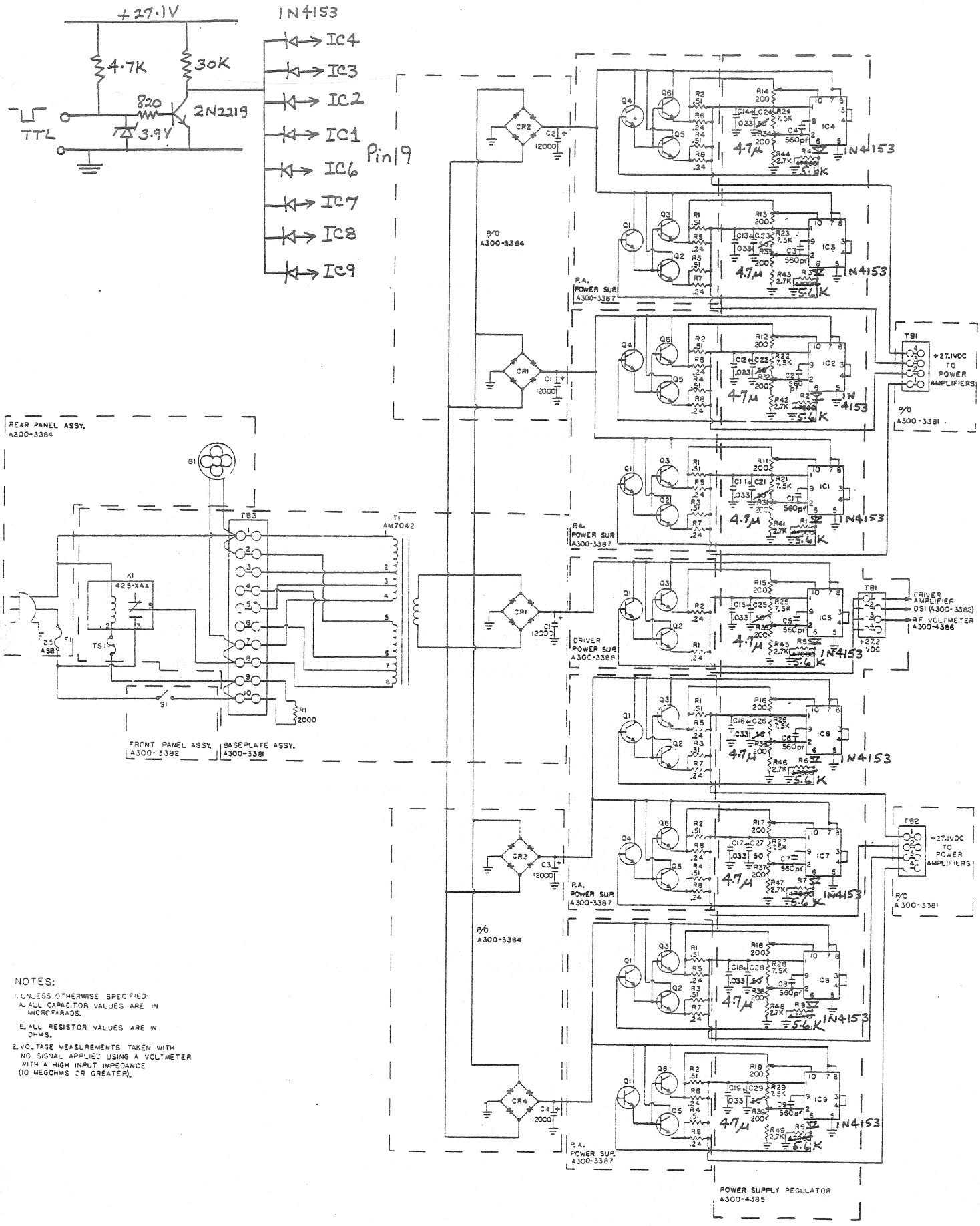


Figure 1. Power Distribution (A300-2381)

μA723
PRECISION VOLTAGE REGULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

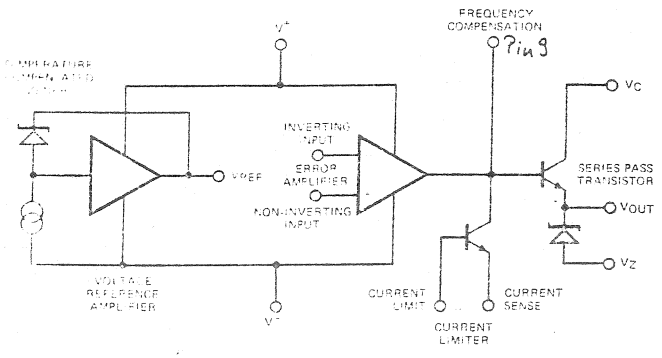
GENERAL DESCRIPTION – The μA723 is a monolithic Voltage Regulator constructed using the [illegible] Planar* epitaxial process. The device consists of a temperature compensated reference [illegible], error amplifier, power series pass transistor and current limit circuitry. Additional NPN or [illegible] pass elements may be used when output currents exceeding 150 mA are required. Provisions are [illegible] for adjustable current limiting and remote shutdown. In addition to the above, the device [illegible] low standby current drain, low temperature drift and high ripple rejection. The μA723 is [illegible] for use with positive or negative supplies as a series, shunt, switching or floating regulator. [illegible] applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic [illegible] regulators, small instrument power supplies, airborne systems and other power supplies for digital [illegible] circuits.

- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- .01% LINE AND LOAD REGULATION
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS
- OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

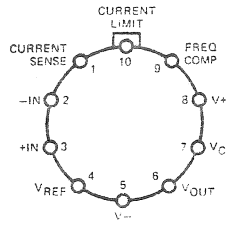
Pulse Voltage from V+ to V– (50 ms) (μA723)	50 V
Continuous Voltage from V_+ to V_-	40 V
Input/Output Voltage Differential	40 V
Differential Input Voltage	±5 V
Voltage Between Non-Inverting Input and V_-	+8 V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation (Note 1)	
Metal Can	800 mW
DIP	1000 mW
[illegible] Temperature Range	–65°C to +150°C
[illegible] Temperature Range	
Military (μA723)	–55°C to +125°C
Commercial (μA723C)	0°C to +70°C
Lead Temperature (Soldering, 60 s)	300°C

EQUIVALENT CIRCUIT



…es on following pages.

CONNECTION DIAGRAMS
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5F
PACKAGE CODE H

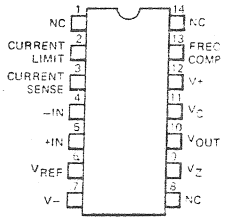


Note: Pin 5 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA723	μA723HM
μA723C	μA723HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



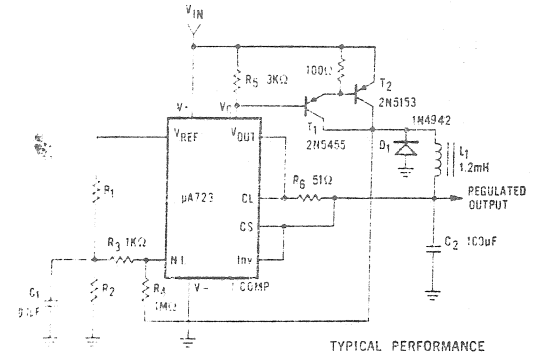
ORDER INFORMATION

TYPE	PART NO.
μA723	μA723DM
μA723C	μA723DC
μA723C	μA723PC

*Planar is a patented Fairchild process

Figure 2

POSITIVE SWITCHING REGULATOR



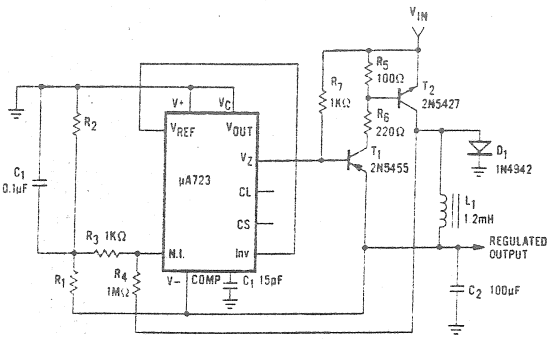
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 30 V)	10 mV
Load Regulation (ΔI_L = 2 A)	80 mV

Note 2

Fig. 9

NEGATIVE SWITCHING REGULATOR



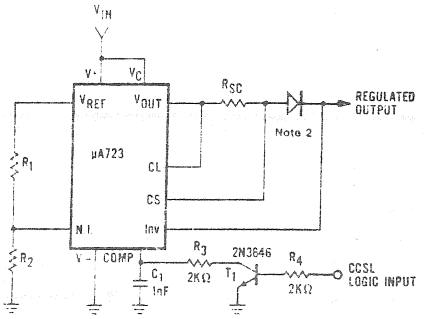
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation (ΔV_{IN} = 20 V)	8 mV
Load Regulation (ΔI_L = 2 A)	6 mV

Notes 2, 6

Fig. 10

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



*1 Current limit transistor may be used for shutdown if current limiting is not required.

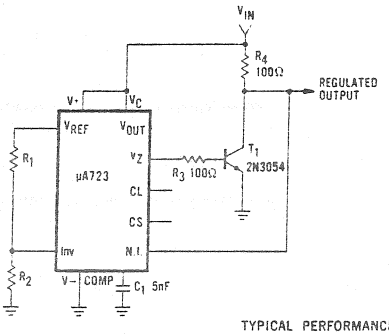
2 Add if $V_{OUT} > 10$ V

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Fig. 11

SHUNT REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 10 V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV

Note 6

Fig. 12

OUT. VOLTAGE ADJUST

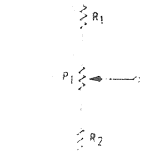
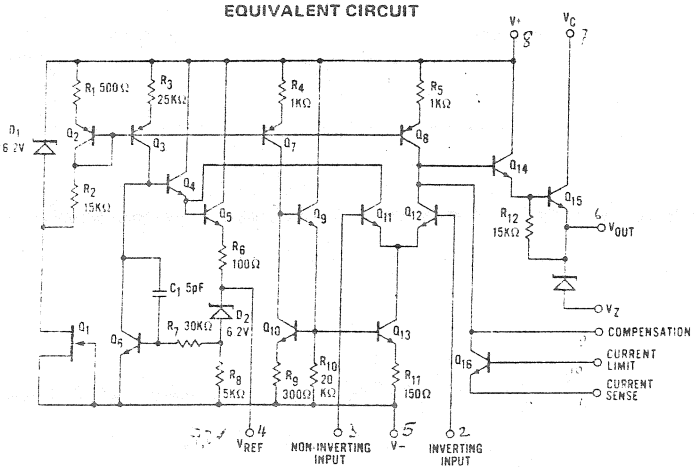


Fig. 13

EQUIVALENT CIRCUIT

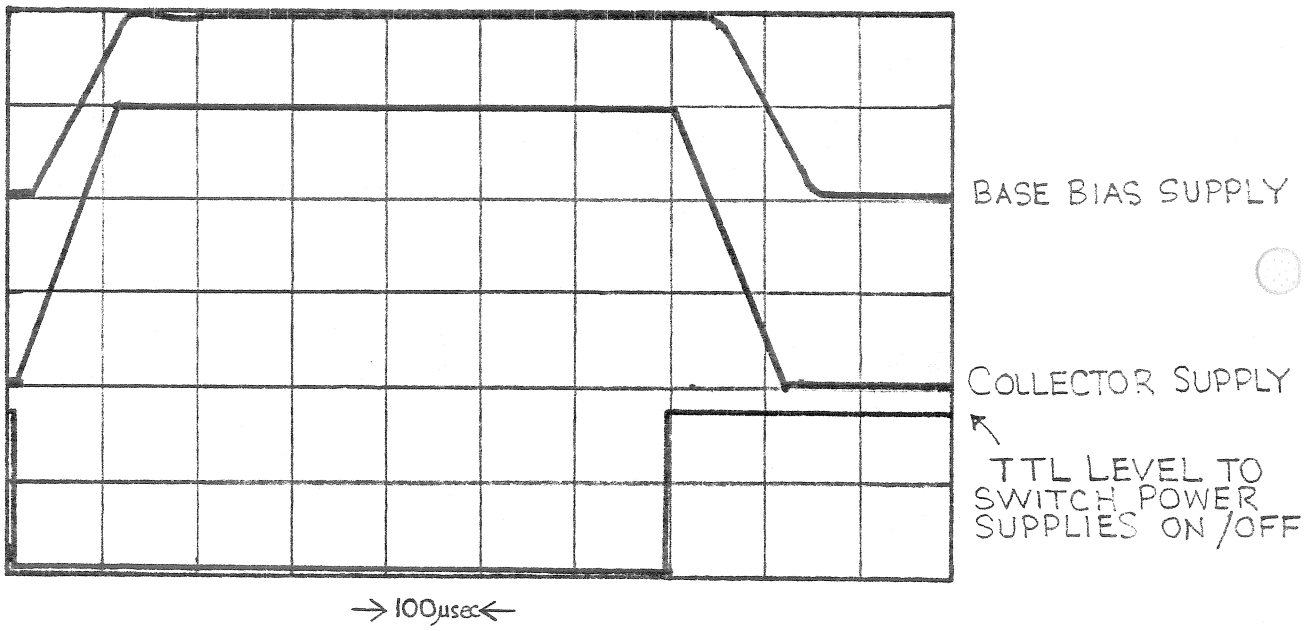


14-27 15mA max

Figure 3

In addition, a diode is used in series to the output of the power supply to protect the output transistor of the IC 723. The resistors R1, 2, 3, 4, 6, 7, 8, 9 are reduced from 47 kΩ in order to make the output resistance of the regulator smaller. This improves the settling time. The bias regulators have to be modified in the same way, i.e., the capacitance has to be smaller. Especially the capacitance C_1 - 10 microfarad at the voltage divider of the reference voltage to the input of the OP AMP in the IC 723 has to be only 10 nF.

The photo shows the rise and fall times of the voltages after the modifications.



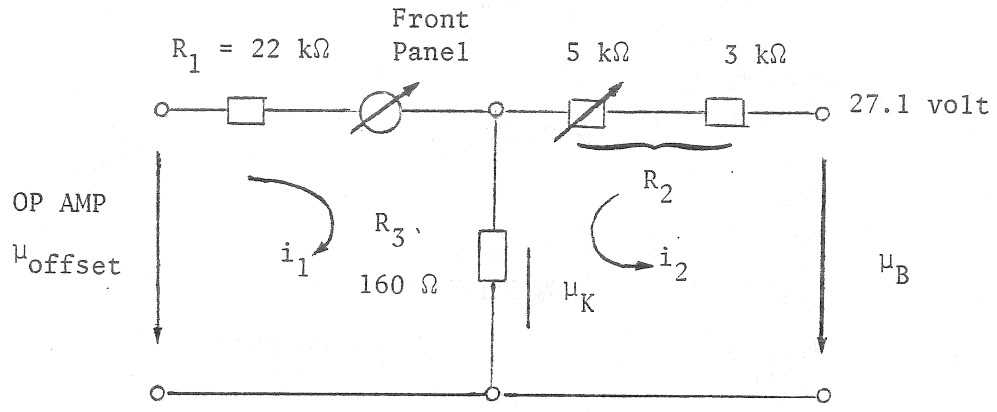
The settling time on the base is about 200 microseconds.

2. Meter Circuit

The output voltmeter supplied by ENI cannot work at the typical duty cycle of $\frac{200\ \mu s}{20\ ms} = .01$. The time constant is too short. The modified voltmeter, Figure 4, has now a rise constant of 4.7 kΩ · 0.33 µF = 1.55 ms and delay constant of 0.33 µF · 20 MΩ = 6.5 sec.

The voltage divider 510 Ω and 4.7 kΩ divides the output peak voltage $\sqrt{300\ W \cdot 50\ \Omega} \cdot \sqrt{2} = 173.2$ V to 16.9 V. This voltage can be handled by the diode HP2800 and the OP AMP LM324. The 20 MΩ in parallel to the capacitance provides the discharge time constant. A disadvantage of this high resistor value is high offset voltage. The bias current can be some 10 nA, so the output voltage of the OP AMP can be some 100 mV, even if no a-c voltage is at the input of the wattmeter.

A resistor of 160 Ω and current through 5 kΩ can eliminate this offset voltage. The adjustment is made with a short at the input of the amplifier.



$$\mu_{offs} = R_1\ i_1 + \mu_K \qquad (1)$$

$$\mu_B = R_2\ i_2 + \mu_K \qquad (2)$$

$$i_1 = 0 \text{ if } \mu_K = \mu_{offs} \qquad (3)$$

(3) → (2) $\mu_B - \mu_{offs} = R_2\ i_2$

$$R_2 = \frac{\mu_B - \mu_{offs}}{i_2}$$

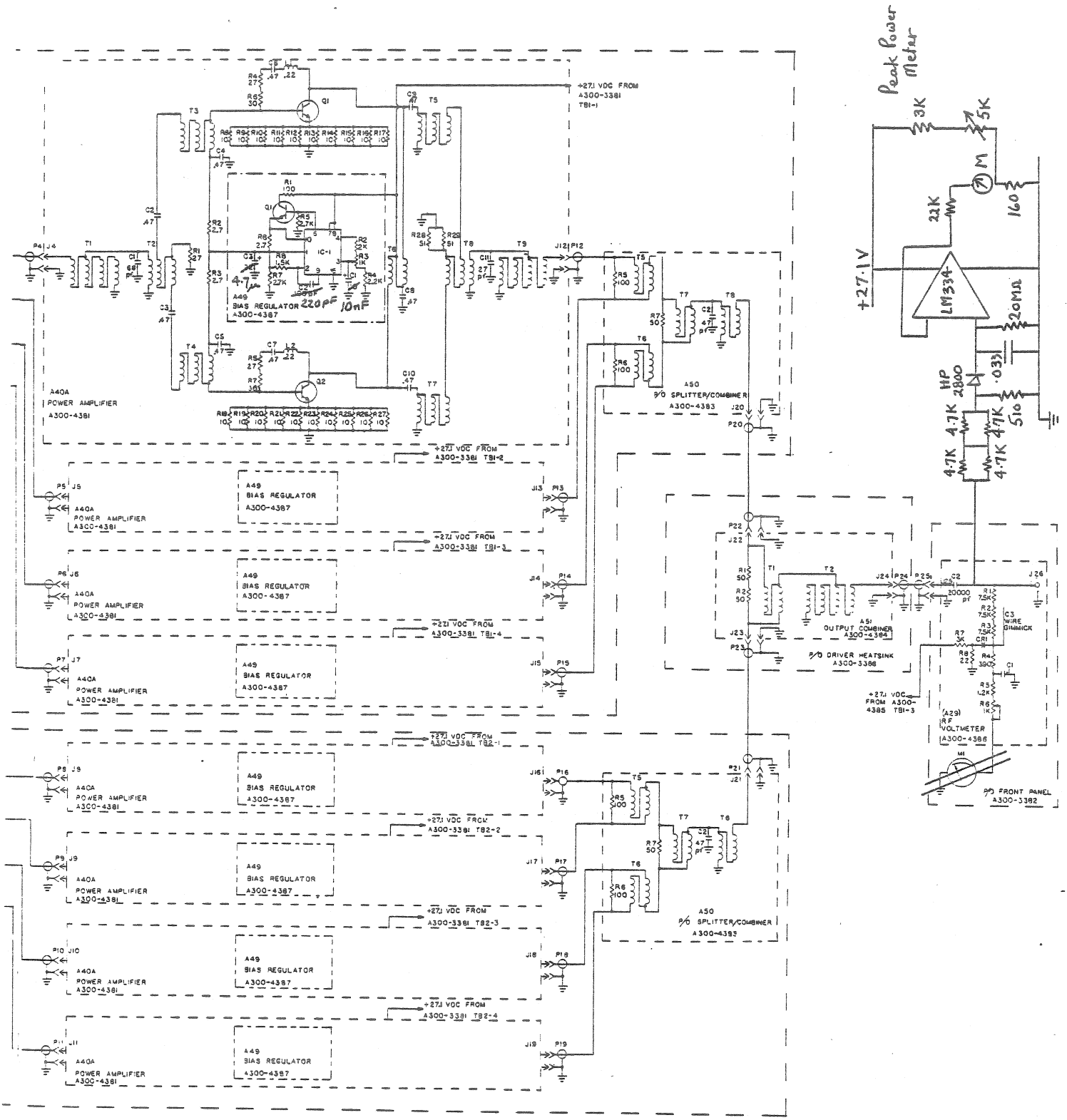


Figure 4. RF Power Amplifier Schematic Diagram

with i_2 = 5 mA, R_2 5200 Ω, $\mu_K = i_2 R_3 \frac{0.8}{5\ mA}$ = 160 Ω.

The bias current of the OP AMP LM 324 is reasonably independent of the termperature, so that the compensenation is stable.

The peak wattmeter follows the peak of the a-c voltage but doesn't follow a single pulse.

Figure 5 shows the frequency behavior of the peak wattmeter.

Figure 6 shows the accuracy is a function of the duty cycle.

Figure 7 shows the linearity.

In Figure 8, the frequency response of the power amplifier is shown. The response is about $\pm$ 1.5 dB between 0.1 and 30 MHz.

Figure 9 shows phase shift $\Delta\phi$ between input and output of the power amplifier depending upon the output power. About 100 watts are required to drive the high power transmitter. $\Delta\phi$ is about 4° at this point between 25 and 30 MHz but only 1° from 0.1 to 20 MHz. $\Delta\phi$ is increasing with the output power up to 20°. This phase shift does not enter directly into most measurements made by the system.

Figure 10 shows the harmonics as a function of the frequency.

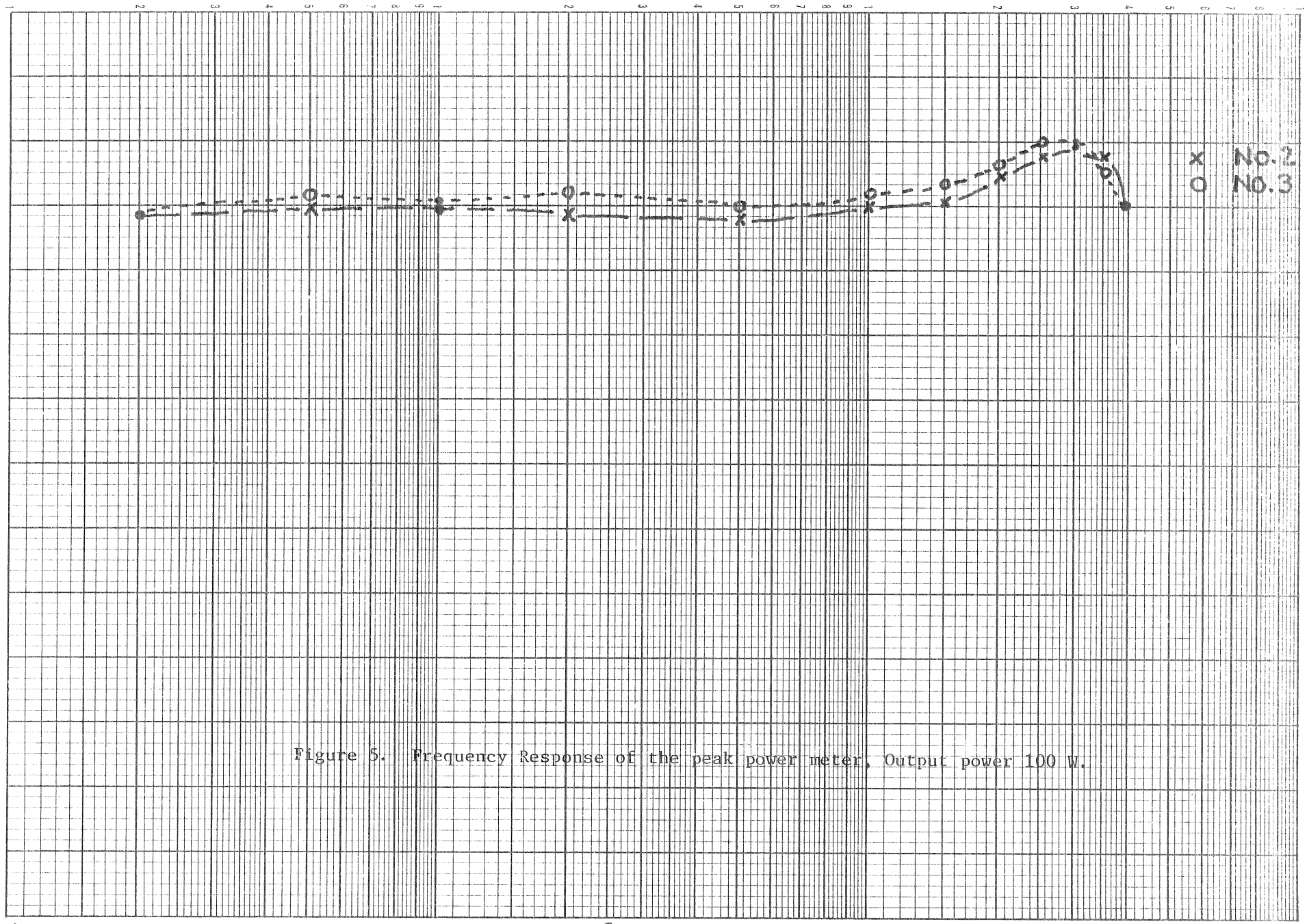


Figure 5. Frequency Response of the peak power meter, Output power 100 W.

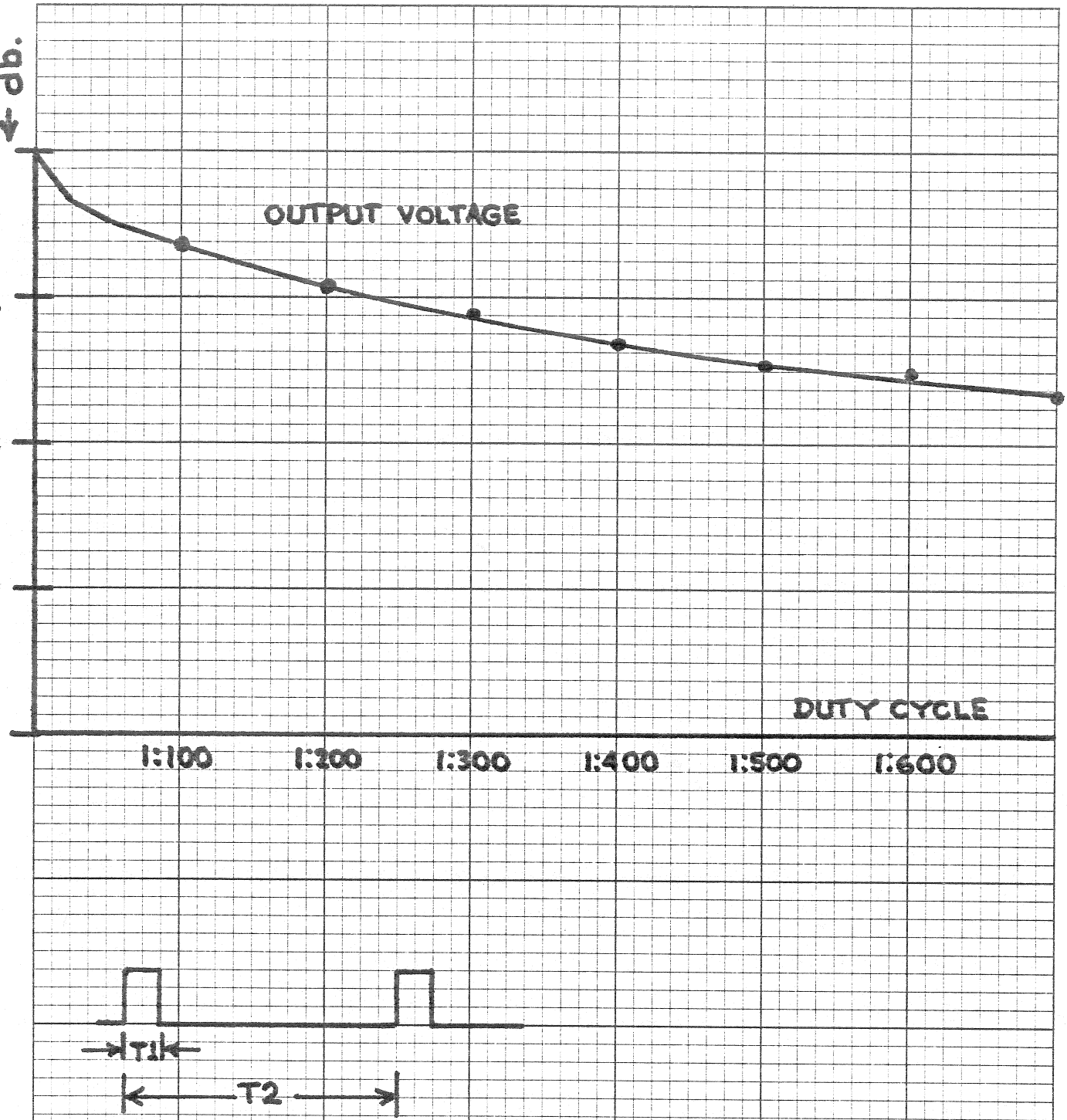


Figure 6. Output voltage of the peak power meter as a function of the duty cycle.

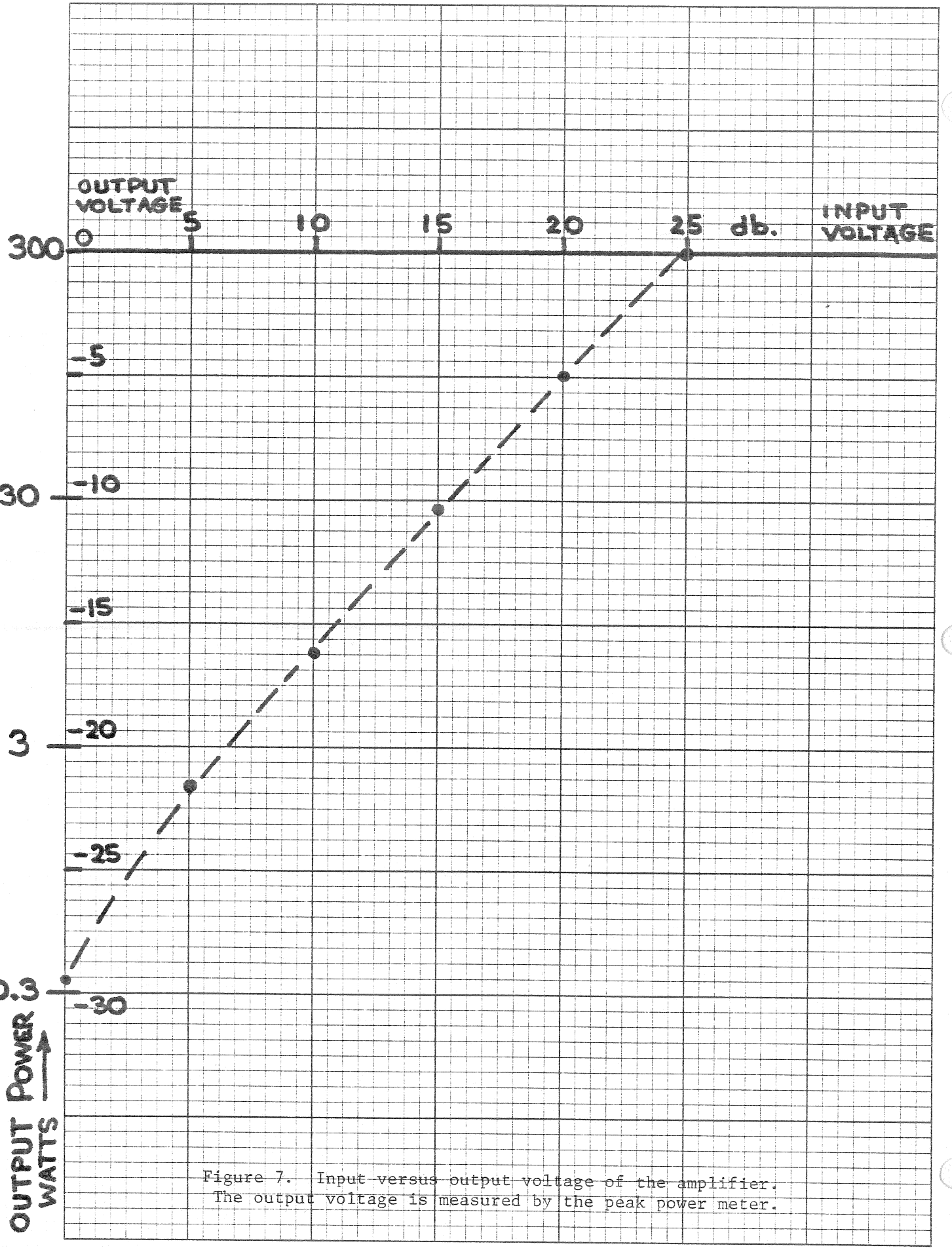


Figure 7. Input versus output voltage of the amplifier. The output voltage is measured by the peak power meter.

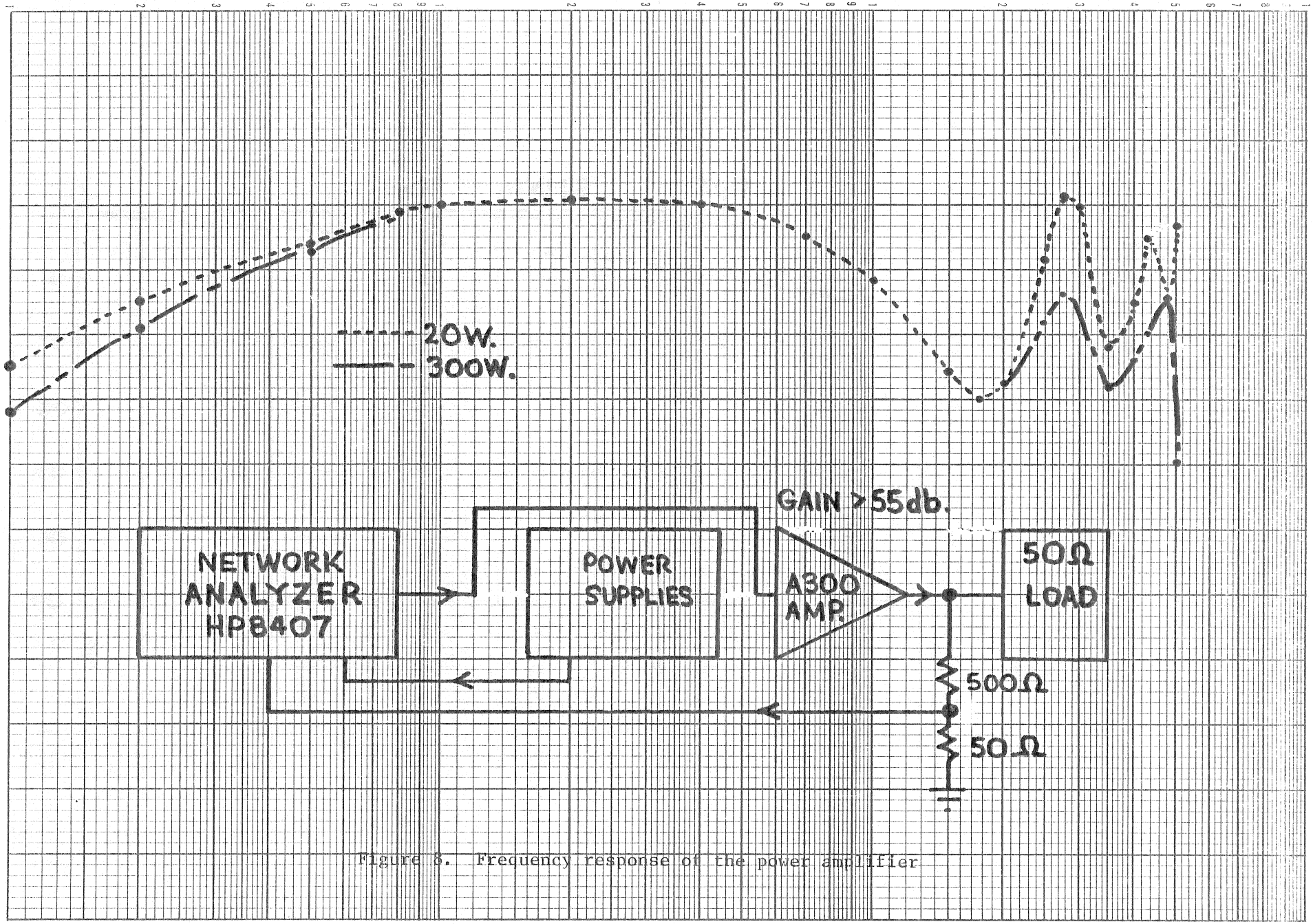


Figure 8. Frequency response of the power amplifier

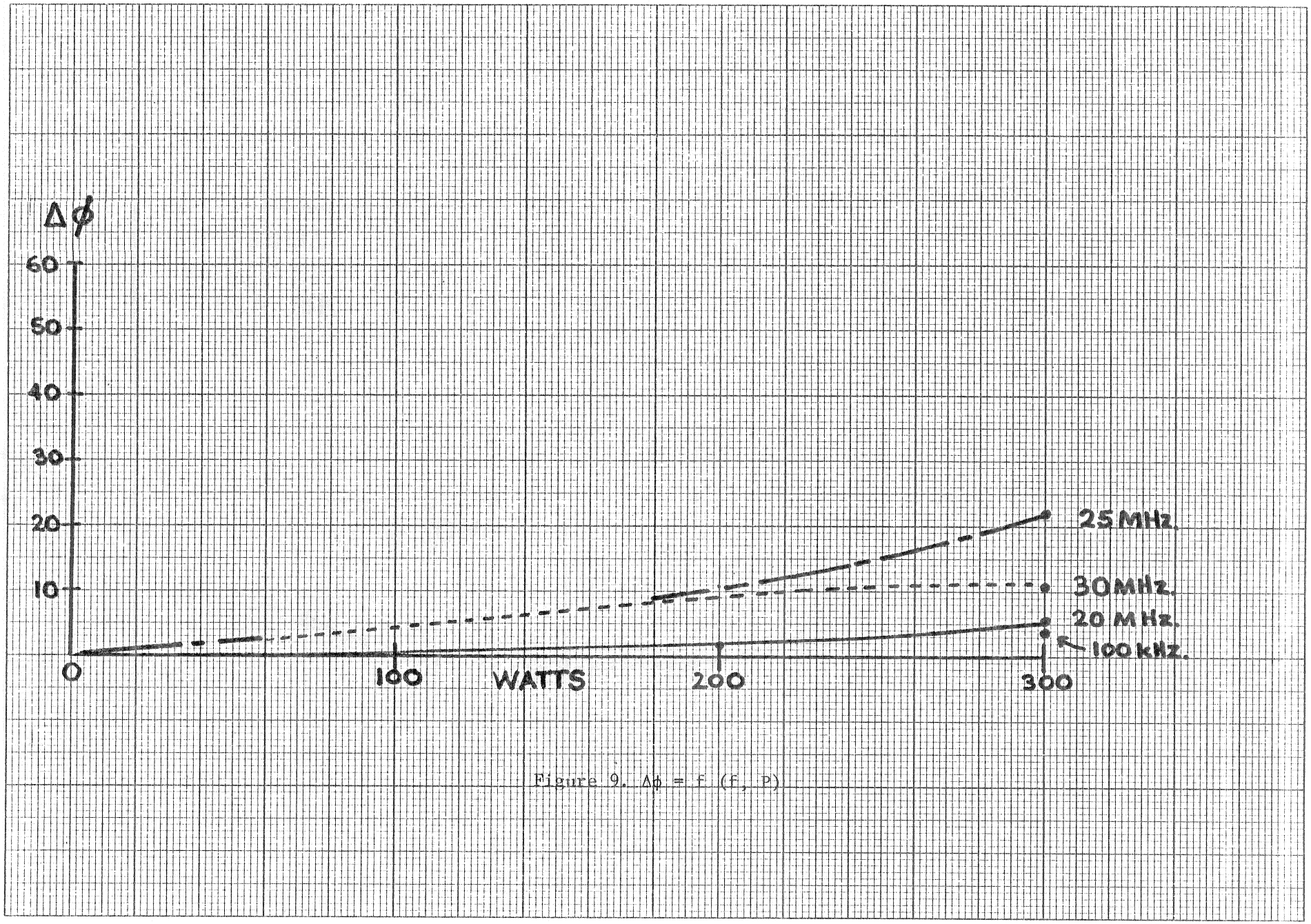


Figure 9. $\Delta\phi = f(f, P)$

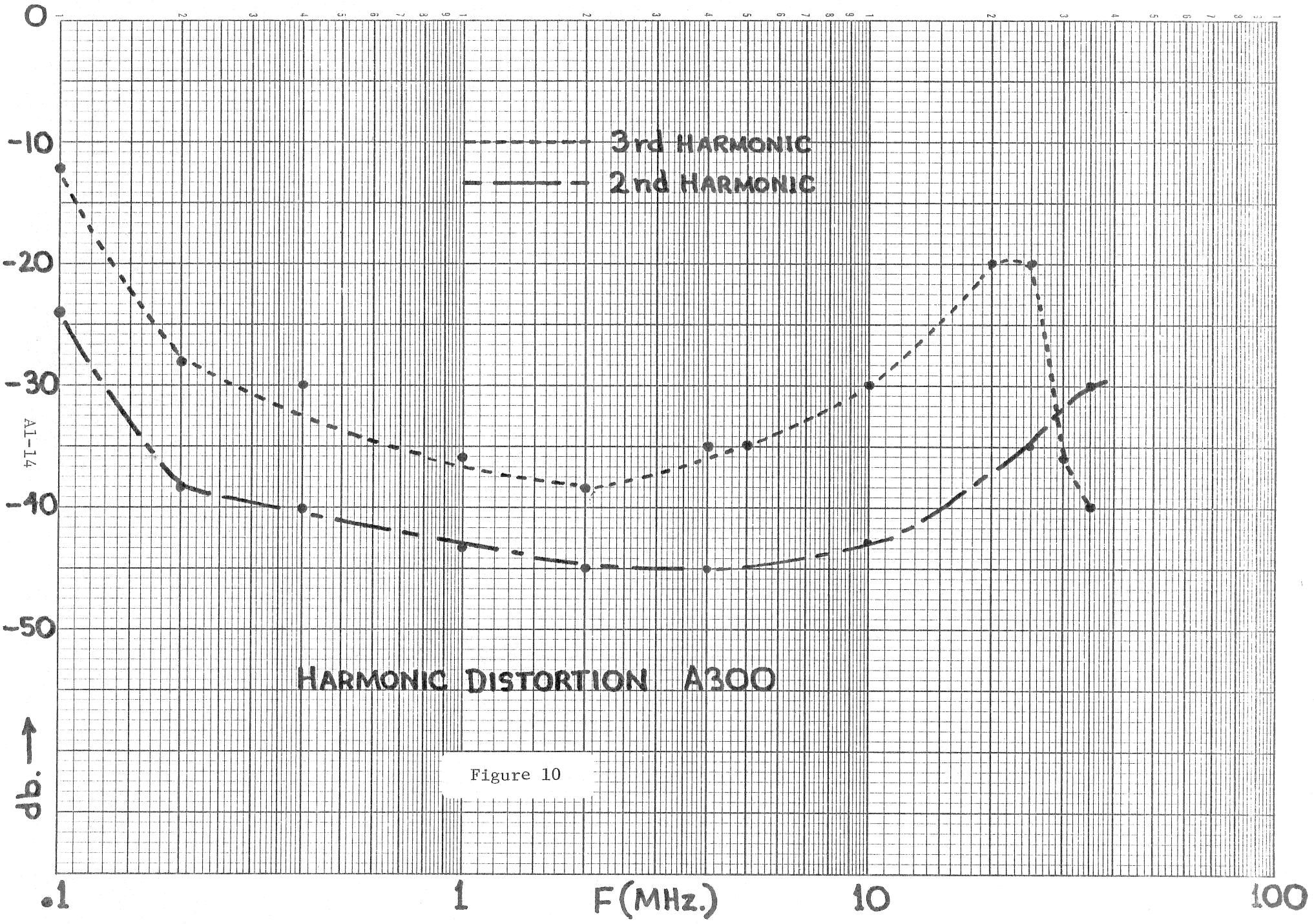


Figure 10

Table 1. Transmitter Rack Interconnections

J#	Pin#	Description
J-1	Key	Ground
	Brass	220 V AC to Filter
	Brass	220 V AC to Filter
J-2	Copper	Tap of Variac
	Brass	To Shorting Plug or Variac
	Brass	To Shorting Plug or Variac
J-3	Round Blade	Ground
	Copper	220 V DC to Lower Rack Blower
	Silver	220 V DC to Lower Rack Blower
J-4	Round Blade	Ground
	Copper	220 V DC to Upper Rack Blower
	Silver	220 V DC to Upper Rack Blower
J-5	1	Power to Power Pilot Lamp
	2	Power to Power Pilot Lamp
	3	Power to Fil. Pilot Lamp
	4	Power to Fil. Pilot Lamp
	5	Power to HV Pilot Lamp
	6	Power to HV Pilot Lamp
	7	N/C
	8	N/C
J-6	A	Ground
	B	To Pin A of J-14
	D	N/C
	E	N/C
	H	N/C
J-7	A	Ground
	B	N/C
	D	To Pin D of J-14
	E	N/C
	H	N/C
J-8	A	Ground
	B	N/C
	D	N/C
	E	To Pin C of J-14
	H	N/C
J-9	A-B	220 V AC to HPA Fil.
	C-D	220 V AC to HPA Fil.
	E	220 V AC to HPA Blower
	F	220 V AC to HPA Blower
	G-H	Ground
	I	+24 V to HPA
	J	+ 5 V to HPA
	K	+24 V to HPA

Table 1 (cont.). Transmitter Rack Interconnections

J#	Pin#	Description
J-10	1	To +24 V
	2	To Pin 3 J-13
J-11	1	+ 5 V
	2	+24 V Switched
	3	+24 V
	4	Ground
J-12	1	To +24 V Switched
	2	Ground
J-13	1	To Fil. Relay from Cont.
	2	To HV Relay from Cont.
	3	To Ant/Load Coax Relay
	4	To Dump Relay from Cont.
	5	To Reset Relay from Cont.
	6	Ground
J-14	A	To Pin B of J-6
	B	To Ground Fault
	C	To Pin E of J-8
	D	To Pin D of J-7
	E	To Current Mon.
	F	To HV Mon.
	K	Ground
J-15	A-B	+ 5 V to Controller
	D-E	Ground to Controller
	H	+24 V to Controller
J-16	-	Rowe Conn. -7 kV to HPA
J-17		VHF Conn. + HV to HPA
J-18		Millen UBG 10 HV Return
J-19	Copper	220 V AC to Power Supply Blower
	Brass	220 V AC to Power Supply Blower