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TECHNICAL OPERATING REPORT

Block 5D-3

Operational Linescan System (OLS)

CDRL Item 054A2
Contract No. F04701-83-C-0048

April 1989

Prepared for

DEPARTMENT OF THE AIR FORCE
Space Division
Los Angeles, California

By

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18 May 1990

Letter No. 048-1046

United States Air Force
Space Division
P. O. Box 92960
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Attention: CWD (DMO)

Subject: F04701-83-C-0048, CDRL 054A2, Technical Operating Report (TOR) (Revision/Change Pages) Bus 2120 Rev A dated April 1989

Reference: F04701-82-C-0148, CDRL 054A2, Technical Operating Report (TOR) Commanding and Telemetry Operation Reference Manual dated October 1986

Enclosure: Ten (10) copies of the Subject CDRL

Gentlemen:

In accordance with the terms of the subject contract, enclosed herewith are ten (10) copies of CDRL 054A2 entitled Technical Operating Report (TOR) (Revision/Change pages) for your review and retention.

If I can be of assistance, please call me at (301) 765-1996.

Very truly yours,

WESTINGHOUSE ELECTRIC CORPORATION

Michael L. Wierzbic
Contracts Representative

cc: 1000 SOG (15 copies)

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1. INTRODUCTION

The Defense Meteorological Satellite Program (DMSP) exists to provide timely, high quality meteorological data in support of United States military operations worldwide. The 5D-3 Operational Linescan System (OLS) is the primary sensor instrument in the Space Segment of that program. This Technical Operating Report (TOR) provides a description of that instrument for use by program engineering personnel involved in procurement, test, and operation of the OLS as an individual instrument and as a part of the integrated space segment. The description provided in the TOR is intended to be complementary to other documentation such as the System Summary Report Block 5D-3 (CDRL 051A2, Contract F04701-82-C-0148), the Program Maintenance Manual (CDRL 014A1, Contract F04701-81-C-0033 - updated for 5D-3 on CDRL 18A2, Contract F04701-82-C-0148), and equipment drawings and schematics.

The TOR contains three main sections. The first of these, Section 2, provides functional and physical descriptions of the overall instrument and its individual subsystems. The second, Section 3, describes the operational control of the system including commanding characteristics, general descriptions of memory load contents and the characteristics of system monitoring functions available through the equipment status and processor telemetry channels. In the third major section, appendices are provided containing an operator's manual, a derivation of scan angle vs video sample determination, and a complete telemetry mnemonic listing. These segments are provided for the specific use of personnel who have requirements for detailed understanding in these areas.

The first portion of the functional description in Section 2 is concerned with instrument concepts, methods of operation, and reliability improvement. The section contains descriptions of the various subsystems of the instrument including electro-optical, signal processing, power, scanner drive, and system

control processor. The interconnection and configuration capabilities as well as functional characteristics of these systems are described. The second portion of this section provides physical descriptions of the instrument and its individual subsystems. Functional allocation to various physical packages, interconnections between packages, spacecraft location, and thermal concerns are described in this portion of the TOR.

The second major section, Section 3, is concerned with operational control of the instrument as a part of the total satellite. This section describes the OLS central processor including its structure and instruction set. A general description of the software, including development and validation procedures and the major tasks accomplished by it, is also provided. Program control including command structures, memory load contents, and detailed telemetry characteristics are a part of this section.

The appendices contain a complete operator's manual providing in fine detail the information required for real-time commanding, memory loading, and updates of the uplink memory section. For those involved in primary data analysis, an accurate method for determination of scan angle from video data sample is derived and presented.

2. SYSTEM DESCRIPTION

The Block 5D-3 Operational Linescan System (OLS) consists of an oscillating scan radiometer and a data processing and storage system which is designed to provide pictorial meteorological data (cloud cover) for contiguous global coverage. The line scanner has near constant scene geometric resolution. The OLS sensor employs a moving telescope technique to scan the earth in the cross track direction, while the forward motion of the satellite provides the along track incremental motion. The scanning telescope moves in a precisely controlled sinusoidal manner, driven by a high-Q mechanically resonant scanning mechanism. This motion causes the telescope to dwell longer at the edges of useful scan and has a high ratio of active scan time to total scan time.

The OLS is the primary data acquisition system on the Defense Meteorological Satellite Program (DMSP) spacecraft. This system gathers, outputs in real time, and/or stores multi-orbit day and night visual and infrared spectrum data from earth scenes. It provides such data, together with appropriate calibration, indexing, and other auxiliary signals, to the spacecraft for transmittal to ground stations. The data is collected, stored and transmitted in either fine or smoothed resolution.

Thermal fine (TF) resolution data is collected continuously, day and night by the infrared detector; light fine (LF) resolution data is collected continuously during daytime only by the silicon diode detector. Fine resolution data has a nominal linear resolution of 0.3 nm. Because of the quantity of data collected, it is not possible to store nor to transmit all of the fine resolution information. Therefore, smoothing (as described below) or selective collection is required. Storage capacity and transmission constraints limit the quantity of fine resolution data which can be provided in the stored data fine (SDF) mode to a total of 40 minutes of LF or TF data per 10 minute command readout station (CRS) readout.

Data smoothing permits global coverage in both thermal smoothed (TS) and light smoothed (LS) data to be stored on the primary tape recorders in the stored data smoothed (SDS) mode. This smoothing is accomplished by analog averaging of the fine resolution input from five resolution cells which are contiguous in the across track direction, then digitally averaging five such 1 by 5 cell samples in the along track direction. A nominal linear resolution of 1.5 nm results. Four-hundred minutes of LS and TS data may be transmitted during a single 10 minute CRS readout.

In addition, a photomultiplier tube allows collection of light smoothed (LS) data under half-moon or brighter nighttime conditions at 1.5 nm nominal linear resolution.

A combination of either fine resolution data and the complementary smoothed resolution data (i.e., "LF and TS" or "TF and LS") can be provided directly to remote sites in the real-time data (RTD) mode. In this mode, only the analog, across-track smoothing is provided before transmission. Along-track smoothing is done by the ground processing equipment.

The OLS provides a choice of four independent data outputs and four additional back-up outputs to the spacecraft transmitters.

The 5D-3 OLS design for reliability is based on "functional module redundancy." The 5D-3 OLS system is subdivided into functional modules which are made redundant and independently selectable as to the use of the primary module or the redundant module. This approach allows selection of functioning units until both modules of a required function have failed.

2.1 OLS Functional Description

The 5D-3 OLS is described functionally in the subparagraphs which follow. Many of the functions exist in each of two redundant circuit blocks such that there are nearly two OLS systems in parallel. However, reliability is improved beyond two parallel single string systems by incorporating selectability of each functional module.

An overview of the OLS from a functional viewpoint is shown in figure 2.1.0-1, 5D-3 OLS Functional Block Diagram Primary Data Flow is indicated by the heavier lines which show the processing path from the received scene radiant energy to the formatted digital data streams forwarded to the spacecraft for transmission to the ground. Scene energy is collected by the optics and focused on three detectors for conversion to electrical signals. The detector outputs are amplified and filtered in the analog signal processing. The formatters then convert the analog signal to a digital signal and format the results into three separate data streams. The output data multiplexer provides these data streams to the selected data storage within the OLS or to the selected transmitter on the spacecraft by way of data security (encryption) if commanded.

Supporting this primary data flow are the digital signal processing functions in the processor, operational program memory, and the input/output (I/O) circuitry. The software stored in the operational program memory in conjunction with the hardware in the processor and I/O provide control of the primary data flow and support functions as commanded from the ground through the spacecraft interface. The sensor and gain control causes the signal level of the primary data to be appropriate for the input received. Special sensor control is provided for up to 12 sensors whose outputs are needed to support the spacecraft mission and are fed into the primary data streams.

The power supply system converts the spacecraft provided power to the voltage levels and regulation needed throughout the OLS.

The scanner monitor and control analog processing function, together with the encoder and wow/flutter digital processing function provides the ability to collect scene data and assign it the proper geographic location.

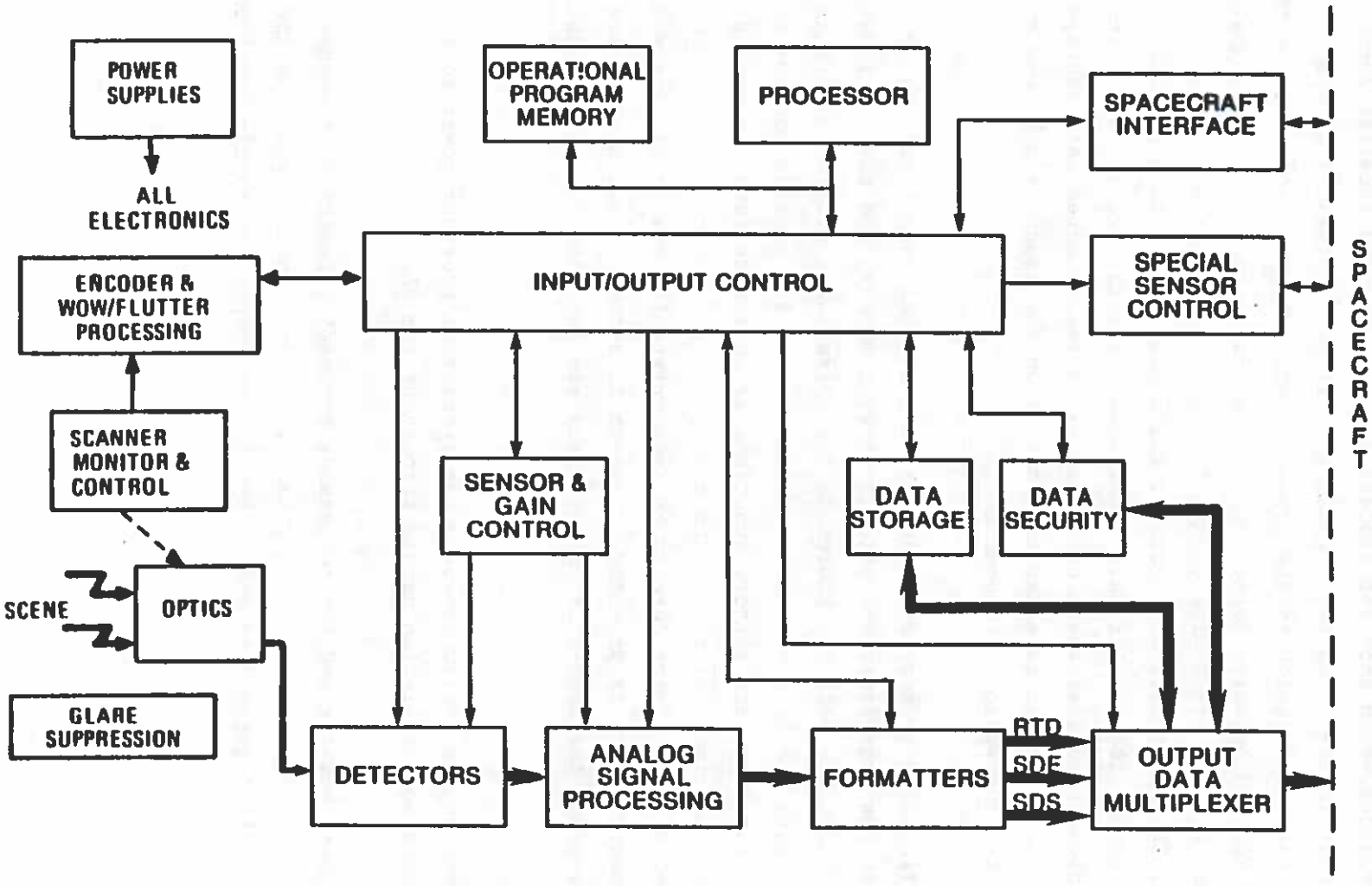


Figure 2.1.0-1. 5D3 OLS Functional Block Diagram

The OLS provides functional module redundancy in all power and data handling systems as shown in figure 2.1.0-2, the 5D-3 OLS System Block Diagram. The operational system configuration which determines which functional blocks are "on-line" is controllable from ground commands or from a stored program in the on-board memory.

Redundant functional blocks include:

Power Supply - cross switching between two independent supplies is provided.

L-Channel - redundant VDGA, lin-log amplifier, transient blanker, and filters.

T-Channel - redundant shaper network, segment gates, and filter.

Scan Monitor - redundant encoder fiducial pulse generation within the optical encoder and redundant auxiliary pulse generation enables redundant encoder control track generation.

Motor Drive Circuitry - redundant ENPA decoder and drive motor electronics which are independent of the processor.

Processor - dual processors where each processor can handle the entire data processing function.

Memory - redundant memories where either memory may be accessed by either processor.

I/O Interface - redundant I/O control, S/C interface, sensor control, gain control, encoder and wow/flutter processing, output data multiplex and formatter controls where any functional block of either I/O may be placed on line.

Formatters - dual formatter memories, RTD formatters, SDF formatters, SDS formatters, and SSP processors where each block can be connected independently.

Output Switching Unit - dual oscillator and clock circuitry.

In addition to full redundant modes, there are fallback modes which result in slightly degraded performance. The modes are:

IMC Shut-Off - The elimination of IMC in the event of failure in the IMC drive.

Encoder Simulator - The digital generation of the encoder delphi clock from encoder control track signal. The control track is redundant but the encoder delphi clock generation is not. The digital generation of the delphi clock is redundant.

T-Channel - Use of a single detector segment, preamp and postamp (left or right) across scan in the event of a failure.

HRD Backup - Use of a back-up HRD postamplifier to be used only with the "C" detector segment across scan. This fallback mode covers the eventuality of an A or B detector segment or primary postamplifier failure.

2.1.1 Electro-Optical

The electro-optical function performs the transformation of scene radiant energy received by the OLS to low level electrical signals proportional to the desired scene and suitable for further signal processing. Scene radiant energy is collected by the scanning telescope over a wide spectral band, selectively processed to travel two spectral paths, focused on three detectors, and converted from photons to electrical signals proportional to the desired scene energy. The functional consideration of this portion of the OLS is described in three subsections.

Optics - the portion accomplishing photon collection and processing.

Glare Suppression - the portion rejecting unwanted photons within the desired spectral band.

Detectors - the portion converting electromagnetic energy to electronic signals.

2.1.1.1 Optics

The optics of the OLS receive wideband radiant energy from terrestrial scenes and deliver portions of that energy to three detectors located at three different focal planes of the optical system. There are two portions of the OLS optics:

Telescope - a five reflective surface Cassegrain assembly that scans the scene in the crosstrack direction.

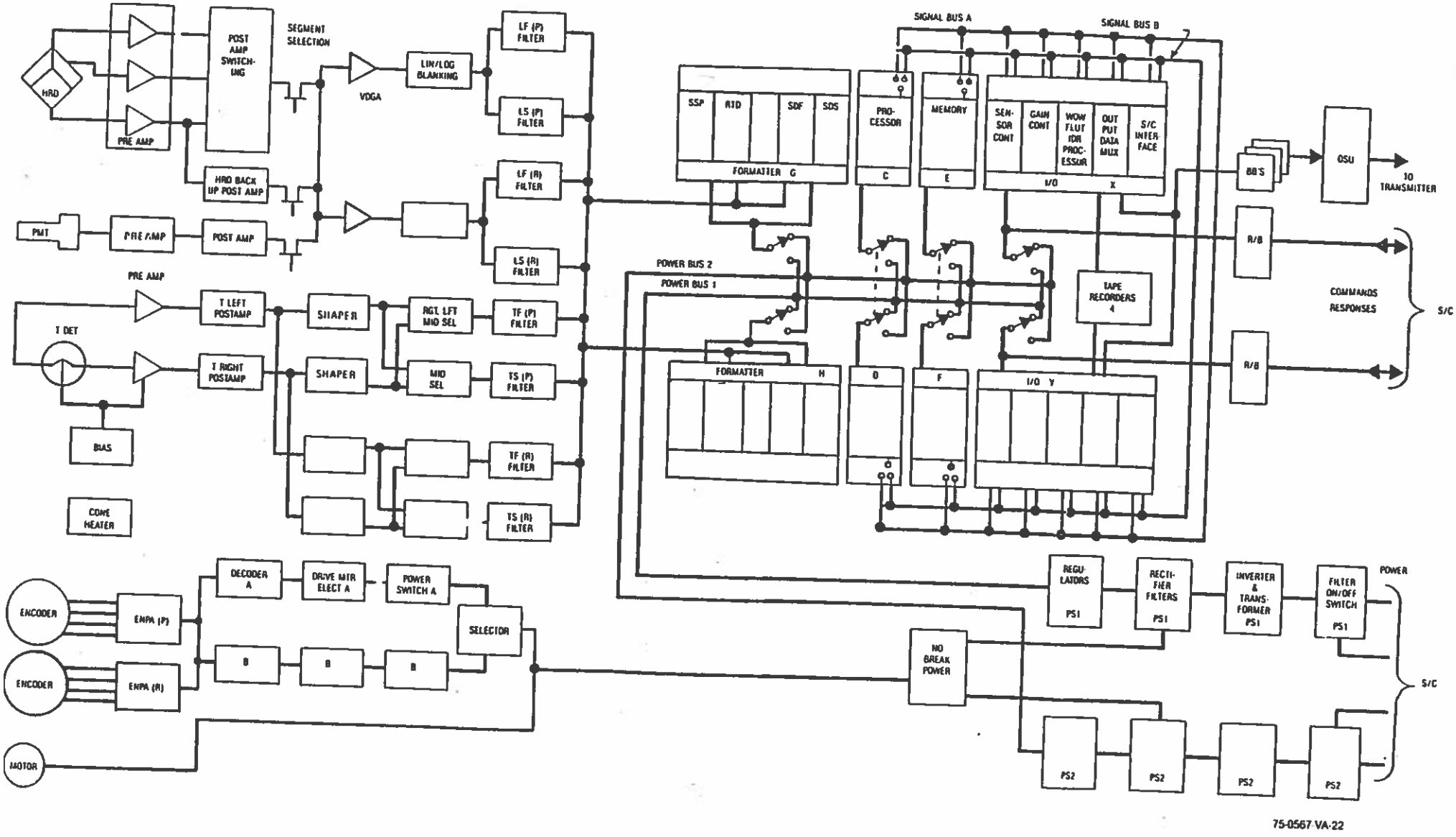


Figure 2.1.0-2. OLS System Block Diagram

Relay Optics - the stationary optical subsystem consisting of both lenses and mirrors, that distributes the telescope output to three detector focal planes.

2.1.1.1.1 Telescope

The telescope, the scanning front end of the OLS optics, receives the scene radiant energy with a nominal effective aperture of 187.4 cm^2. Figure 2.1.1-1 shows the basic Cassegrain optical configuration of the telescope and illustrates the size of the light bundle along the optical path.

The first mirror in the optical path is the primary mirror (M1) which has an 8-inch, f/1.0 parabolic. The secondary mirror (M2) is hyperbolic with a focal length of -2.499 inches. The resulting telescope focal length is 48.0 inches. This combination forms a real image 13.11 inches from the vertex of M2.

Energy reflected from M2 is intercepted by a flat mirror (M3) on the rotational center line. M3 redirects the energy at an angle of about 30° away from the rotational center line in the plane determined by the telescope axis and rotational axis. M3 also provides the image motion compensation (IMC) that converts the scan motion to rectilinear.

An elliptical mirror (M4) approximately 0.20 inch in front of the telescope image plane has a dual function: it redirects the line of sight radially inboard toward the rotational axis, where the line of sight is intercepted by a flat mirror (M5); and it serves as a field stop. M5 reflects the line of sight away from the telescope assembly both coparallel and concentric to the rotational axis.

As the telescope scans, the mirror M4 sweeps an arc in space. Near the end of scan in either direction, the line of sight is interrupted by calibration mirrors M4' and M4", which are near M4.

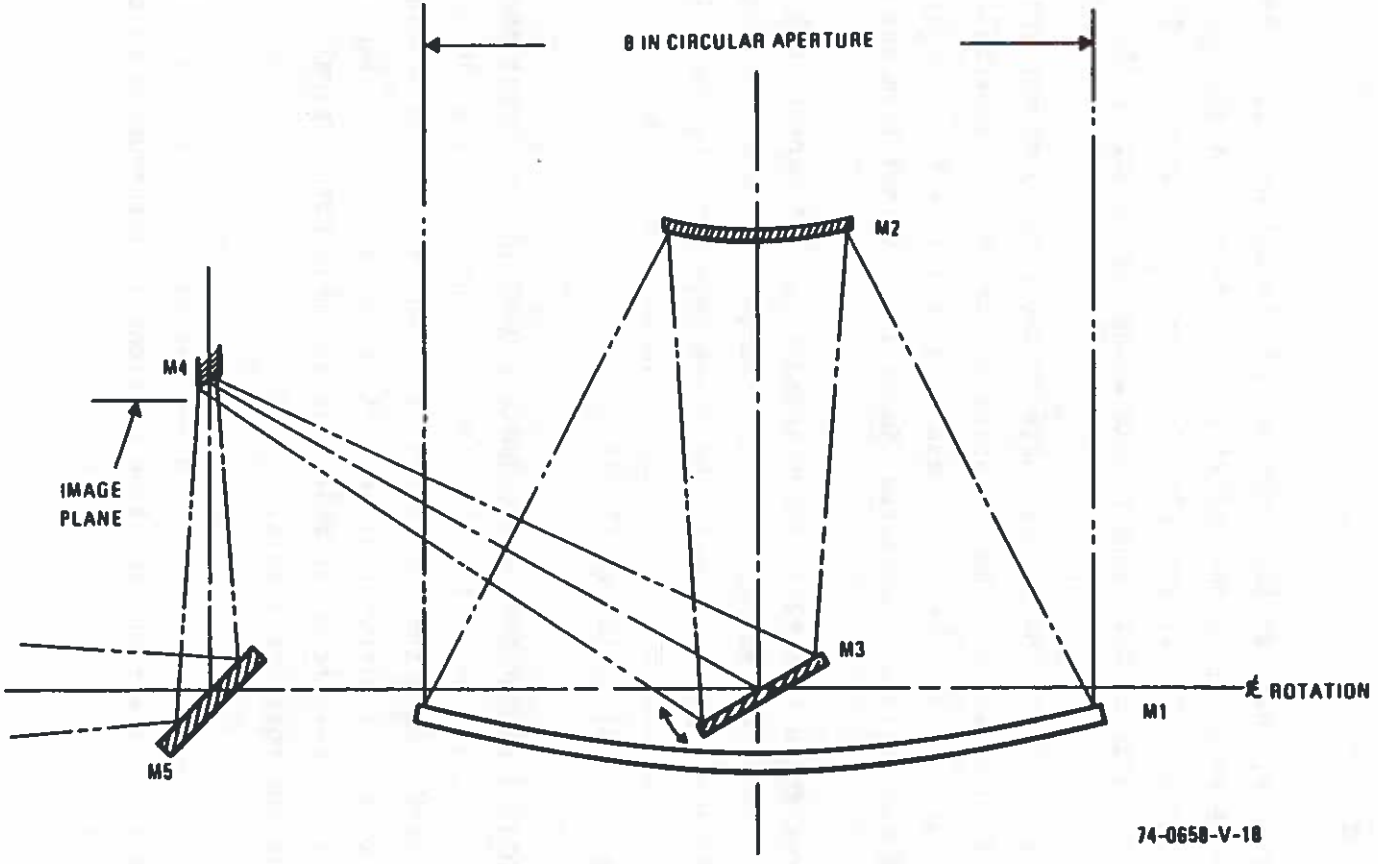


Figure 2.1.1-1. OLS Cassegrain Telescope

These calibration mirrors direct the view from the detectors into cone shaped near blackbody sources of known temperature for thermal channel calibration. The light-day channel also uses the -Z calibration source as a dark reference.

To minimize weight, momentum and inertia, beryllium is used almost exclusively in the construction of the telescope. Beryllium has good thermal and structural properties and provides good dimensional stability when suitably processed. The Be mirror substrates are nickel plated to obtain a smooth surface by optical polishing. Reflective overcoats of protected silver (M1 and M2) and aluminum (M3, M4, M5) are vacuum deposited onto the completed substrates. Care is taken throughout the fabrication and testing cycle to protect these mirrors from contamination. A deployable cover protects the telescope surface from contamination during launch and the first 10 days in orbit.

2.1.1.1.2 Relay Optics

The relay optics, the stationary portion of the OLS optics, delivers focused scene energy to all three detectors. The optical configuration of the relay optics is shown in figure 2.1.1-2. The wideband energy received from the telescope is first split spectrally by a dichroic beamsplitter which reflects the 10.2 to 12.8 micrometer thermal infrared energy for the T-channel while transmitting the 0.4 to 1.1 micrometer visual and near infrared energy for the L-channel.

The T-channel energy reflected from the beamsplitter is transformed into a slightly coverging beam by a germanium lens before being directed by two flat mirrors along the optical axis of the T detector optics (not shown). The final T-channel optical transformation is performed by an f/1.0 meniscus lens of germanium. The meniscus lens uses spherical first and second surfaces to focus the T-channel energy on the T detector through a germanium flat for correction of spherical aberration.

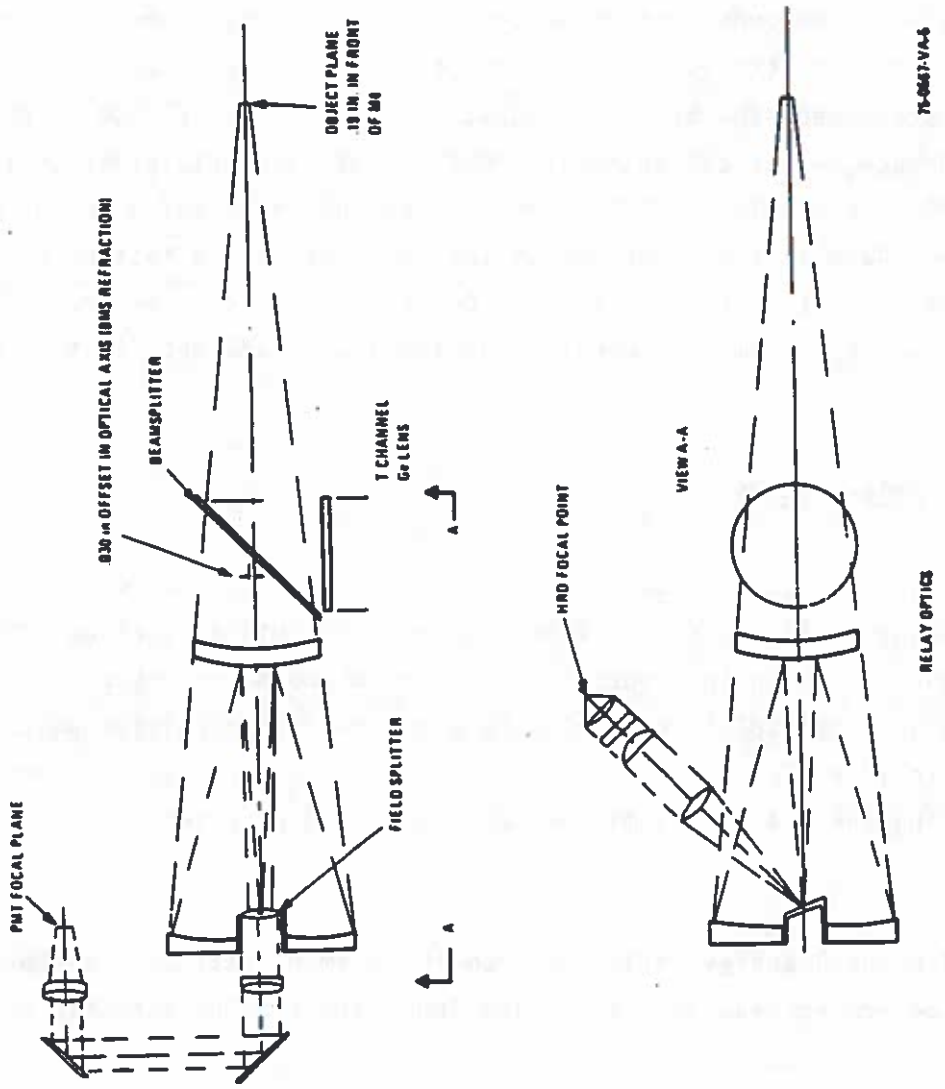


Figure 2.1.1-2. Relay Optics

The L-channel energy passed through by the beamsplitter is transmitted by a folded optical system utilizing two mirror surfaces to the field splitter focal point. The central core of the field of view is reflected by the field splitter into a series of lenses that focus the energy on the L-daylight detector focal plane. The rest of the field of view is transmitted by the field splitter into a series of lenses and redirecting flat mirrors that focus the energy on the L-nighttime detector focal plane.

2.1.1.2 Glare Suppression

Loss of data due to on-axis scattering of incident sunlight is to be minimized. This is to be accomplished by incorporating antiglare features into the optical/mechanical design of the telescope and by providing sunshades.

Glare is suppressed in the telescope in four ways:

(1) The geometric configuration of the telescope

The geometric shape of the telescope limits the maximum input acceptance angle to 14 degrees. The telescope is configured to keep this angle small and thus reduce glare not only from direct input but also from secondary diffuse reflection from M1.

(2) The low scatter finishes on M1 and M2

The low scatter surface on the nickel-overcoated beryllium mirrors M1 and M2 reduces the amount of energy scattered into the field of view from sources off the optical axis.

(3) A field stop at M4

The maximum field half angle is limited to 2.5 milliradians, which is adequate for optics alignment and the required field coverage. The diameter of mirror M4 serves as the field stop. Light traps around its support structure capture radiation out of the desired field of view. Unwanted glare is suppressed by limiting the field angle.

(4) An aperture stop between M5 and the relay optics

Glint from the edges of the hat-shaped part of the telescope, the outer edge of M1, and the support spiders for M2 are sources of glare. M4 is an elliptical mirror that provides a soft focus of these glare sources at a position between M5 and the relay optics. An aperture stop "mask" congruent with the soft image of these sources blocks out this glare.

For noon orbit glare suppression, first surface specular mirror sunshades (GSSA) are mounted immediately adjacent to the aperture area of the telescope. These mirrors prevent sunlight from impinging directly on any part of the telescope or surrounding diffuse scattering surfaces. Because they are highly specular, the mirrors minimize primary scatter into the protected areas. This sunshade provides protection for all orbit positions of orbits having sun angles between 75° and 95°.

For terminator orbit glare suppression, the spacecraft provides an additional sunshade comprised of a large stationary opaque glare obstructor (GLOB) at the +Z (Sunward) end of the spacecraft. It projects in the +X (Earthward) direction and prevents sunlight from impinging directly on any part of the telescope or surrounding difuse surfaces for orbits having sun angles between 0° and ±45°.

2.1.1.3 Detectors

The three photon radiation detectors in the OLS transduce the scene radiant energy into low level electrical signals:

T detector for thermal infrared energy

The T detector is a two-segment Mercury-Cadmium-Telluride (HgCdTe) photoconductive detector cooled to a temperature of about 110°K and maintained within ±0.1°K of the chosen set point by an active temperature control loop using a small heater on the inner stage of the cone cooler. Spectral bandpass is set by an optical filter on the detector germanium window for passing the 10.2 to 12.8 um range and for rejection of water vapor, CO_2 and ozone effects.

The detector consists of two orthogonal elements, designated T left and T right. Figure 2.1.1-3 shows the T detector configuration. The track and scan directions are shown at the nadir scan angle. Figure 2.1.1-4 shows the along-scan T detector switching. For T fine (TF) data, T left video is used for scan angles more negative than -41°; T right video is used for scan angles more positive than +41°, and T left and T right are summed for the center scan angle (-41° to +41°) region. For T smooth (TS) data, T left and T right video are summed across the entire scan. In the event of a failure of one element, the other may be used for the entire scan in a fallback mode.

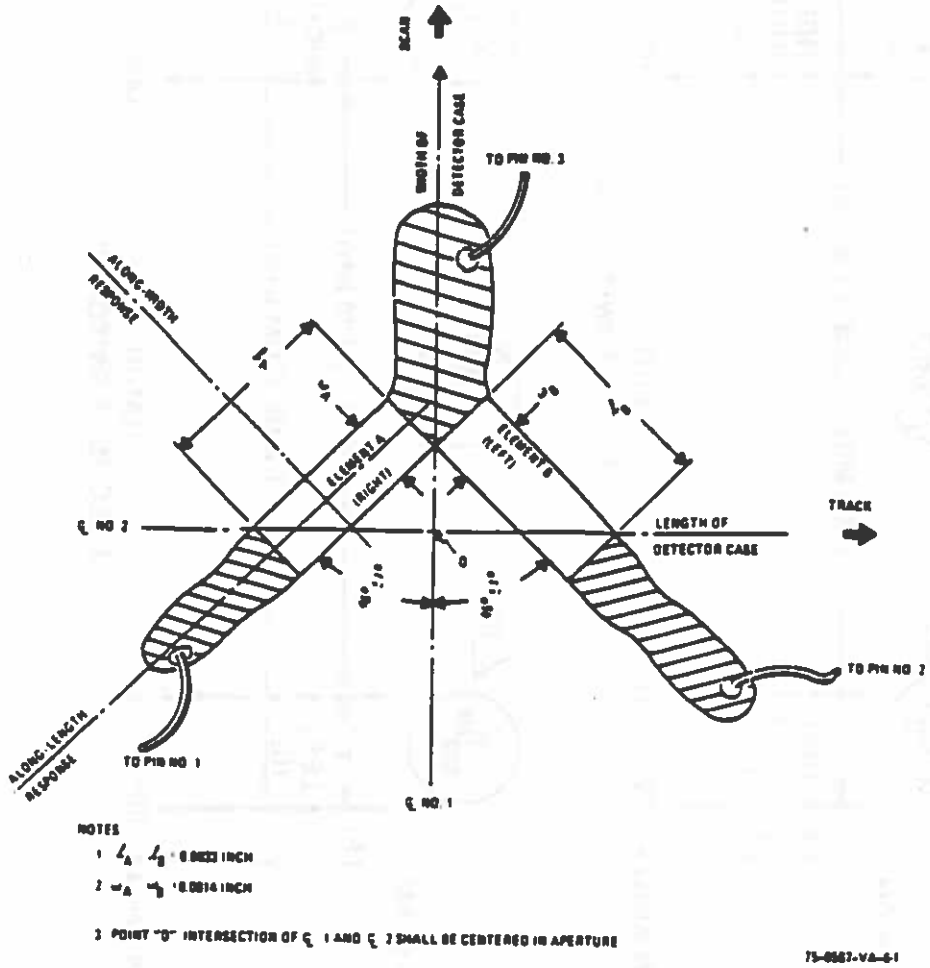


Figure 2.1.1-3. T. Detector, 2 Segment

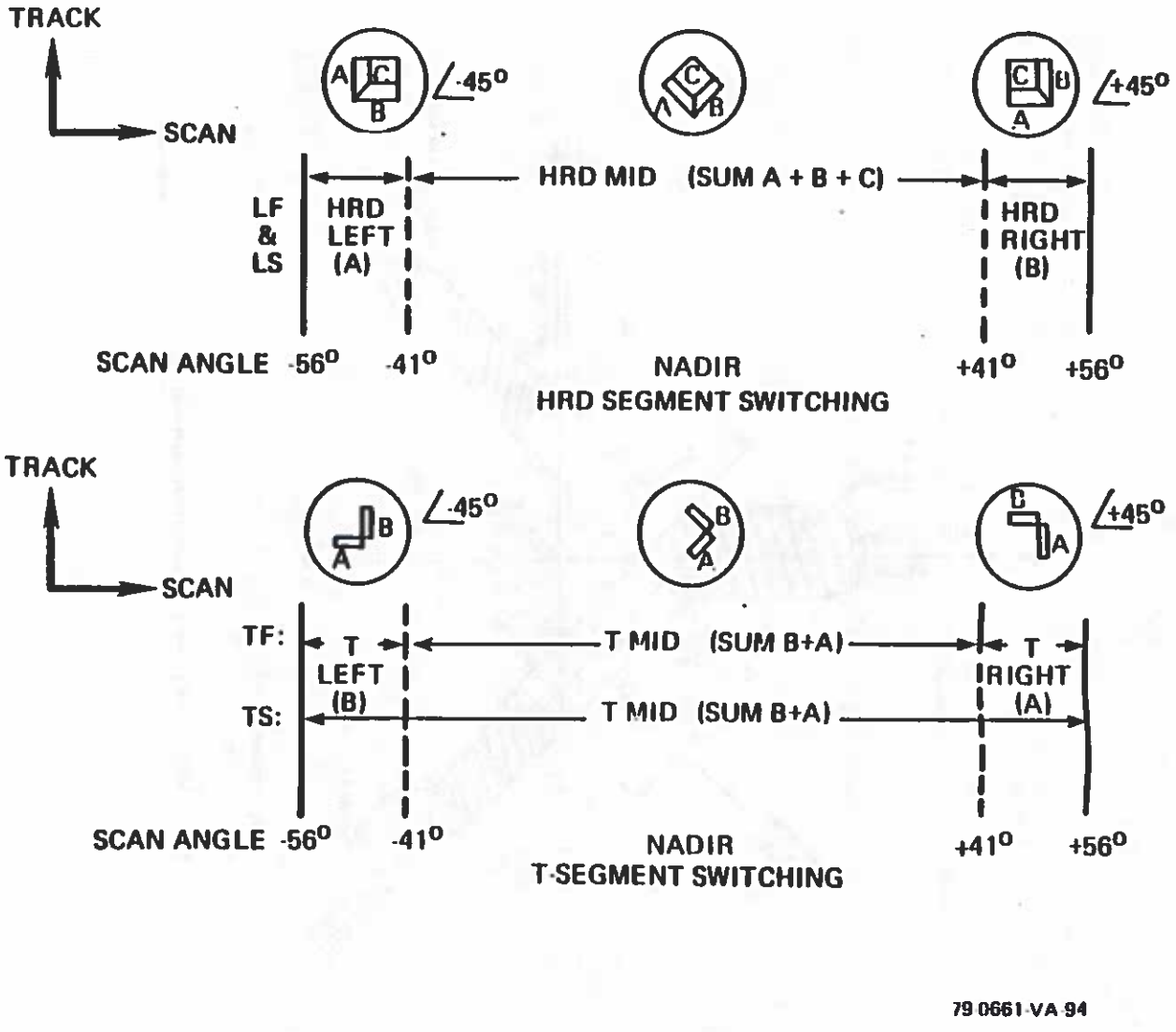


Figure 2.1.1-4. Along Scan HRD and T-Channel Detector Switching

HRD detector for daylight scenes

The HRD detector is a three segment, silicon, planar, reverse biased photoconductive PIN diode with the N side (cathodes) common for all three elements. A double glassing and double metallization technique is used to define the three active areas. This photodiode has a fused silica window with an antireflection coating and a metallized aperture for f/2.0 incoming rays. The dc dark leakage currents are so low below +10°C, that no cooling is required for the HRD. Figure 2.1.1-5 shows the HRD detector configuration. The track and scan directions are shown at nadir scan angle. Figure 2.1.1-4 shows the along-scan HRD detector switching. Segment A is used for scan angles more negative than -41°, segment B is used by command for scan angles more positive than +41°, and all three segments for the center -41° to +41° region. In the event of a failure of an element, any one or the sum may be used by command for the entire scan in a fallback mode.

PMT detector for night scenes

The PMT detector is a cesiated GaAs (gallium arsenide) opaque photocathode, image dissector type, multiple dynode photomultiplier tube (PMT) that serves as the low resolution detector for the nighttime visible wavelength energy. Figure 2.1.1-6, a cross-sectional view, shows features of the PMT design. The photocathode is a square with a nominal edge of 0.100 inch. The PMT consists of cascaded gallium phosphide secondary emission dynodes that provide the necessary noise-free gain for tube operation. The first dynode is coupled to the image dissector front end by the defining square aperture at the base of the plate cylinder. Emission current from the last dynode is collected by the anode. The defining square electron aperture is imaged on the photocathode side of the face plate to form an effective photocathode area equal in size and shape to that dictated by system field-of-view requirements. With the proper focusing fields in the front end (determined by the photocathode, focus, cone, and plate voltages), only photoelectrons emitted from the effective photocathode area will pass through the defining aperture hole, undergo secondary emission multiplication in the dynode chain and subsequently be collected by the anode.

To vary the field of view, (FOV) the image dissector magnetically deflects the defining electron aperture image referred to the photocathode. This effect, in conjunction with the physically limited (masked) photocathode area, allows FOV control by varying the size of the overlap region between the limited photocathode area and the defining electron aperture image. The magnetic deflection is accomplished by controlling the currents in two orthogonal coils on the PMT yoke. Figure 2.1.1-7 shows the PMT detector aperture configuration. The full aperture resulting from no magnetic deflection is used in the central portion of the scan from about -41° to +41° (±413 nm). The right edge aperture consists of the rectangular section that is the full FOV in one dimension and .33 to .40 of the full FOV in the other This FOV, which is obtained by magnetic deflection in one direction only, is used from +41° to the +Z end of active data at +56.24° (800 nm). The left edge aperture is identical to the right edge aperture but the long and short dimensions are interchanged. This FOV is obtained by magnetic deflection only in the direction orthogonal to that used to obtain the right edge aperture and

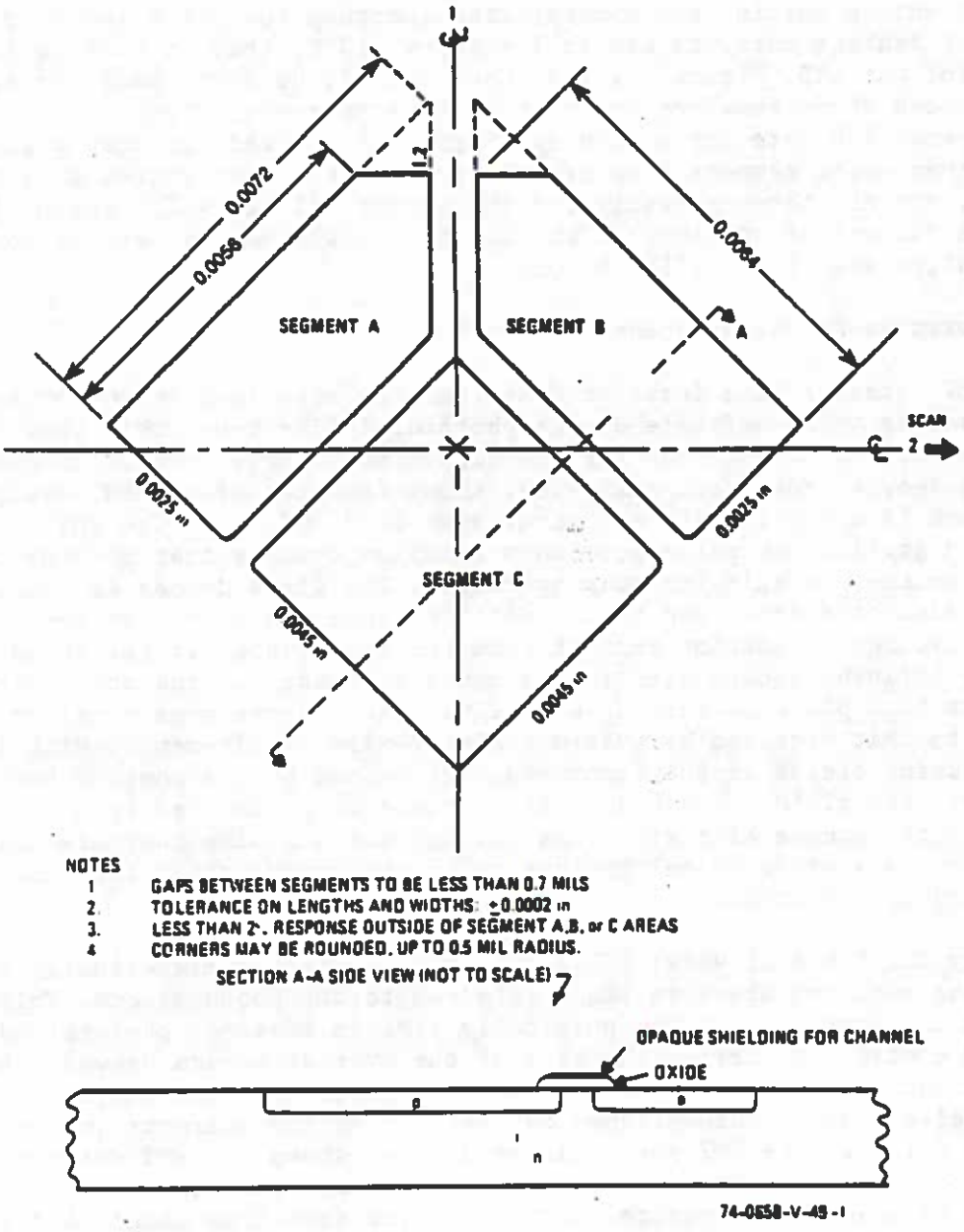


Figure 2.1.1-5 HRD Detector, 3 Segment

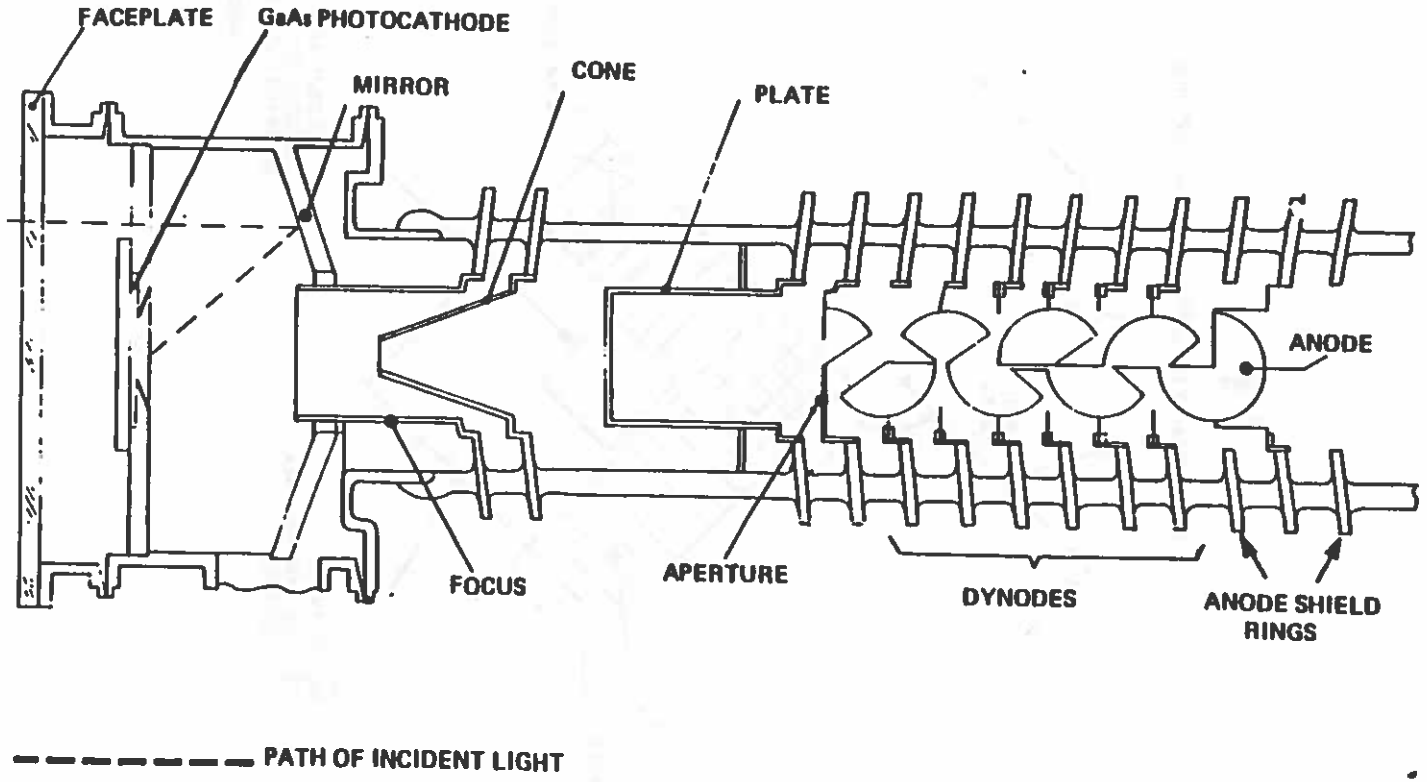


Figure 2.1.1-6. PMT Detector

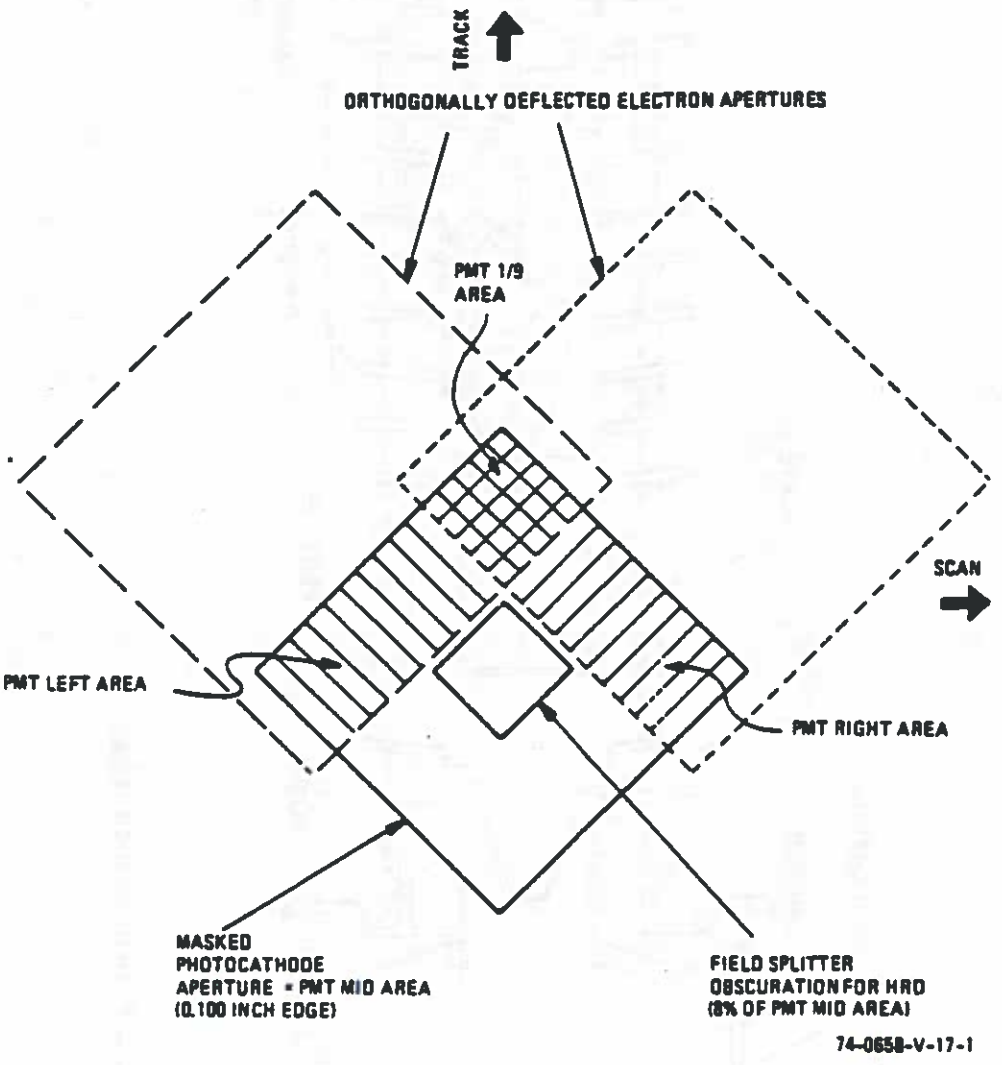


Figure 2.1.1-7. PMT Detector Aperture

is used from -41° to the -Z end of active data at -56.24°. When both magnetic deflections are applied simultaneously, the corner common to the right edge and left edge configurations becomes the FOV. This mode is called PMT 1/9 since it reduces the PMT detector area to about 1/9 of PMT MID.

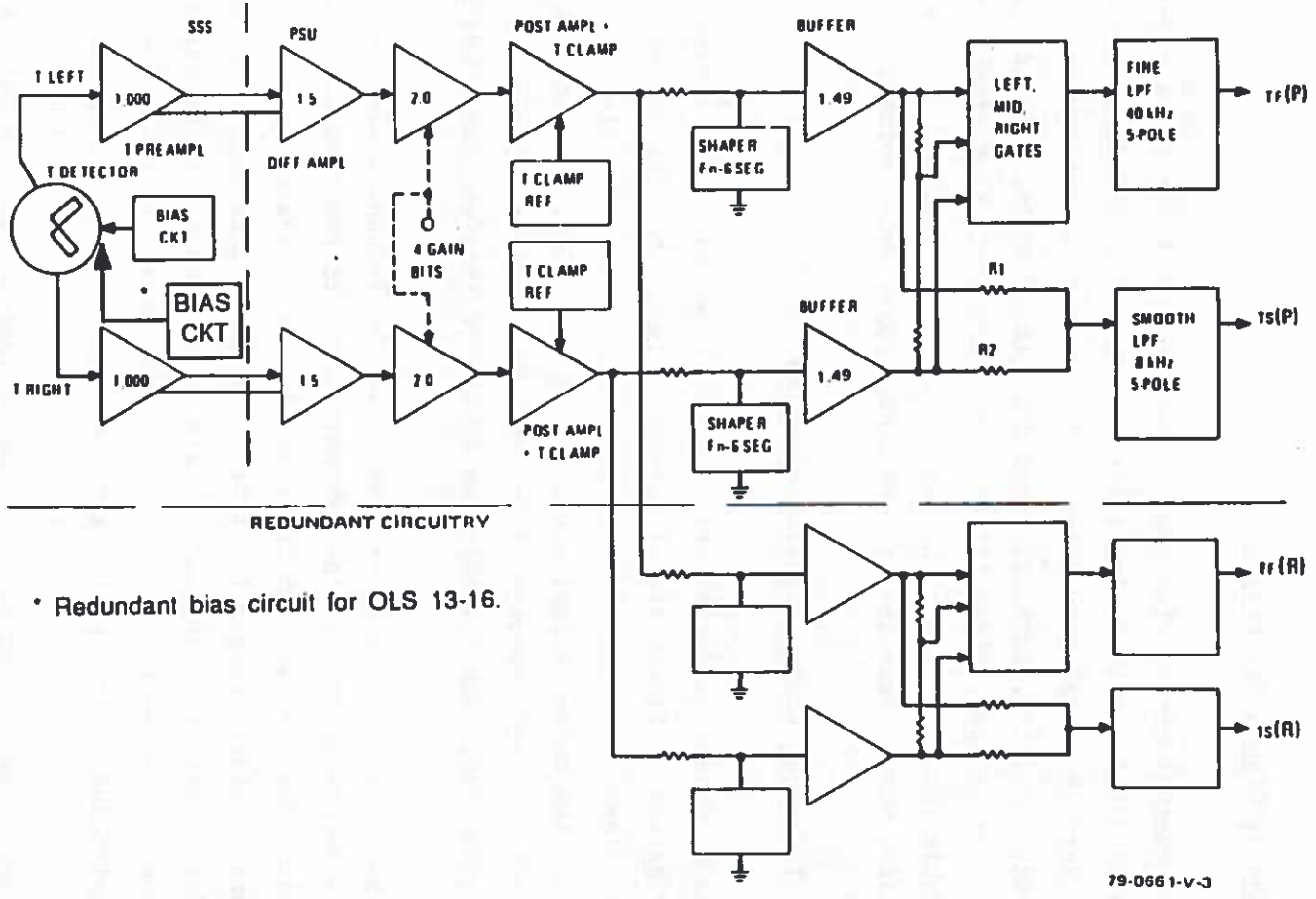
2.1.2 Analog Signal Processing

The channel analog electronics converts the three primary detector output signals into full scale analog signals of the four OLS data types: TF, TS, LF and LS. Various signal processing functions such as amplifying, dark level dc restoring, switching, summing, commanded gain changes, commanded level changes, and low-pass video filtering are provided. Significant amounts of commandable redundant analog hardware blocks and fallback modes are provided in the 5D-2 OLS as described in the subsections which follow.

2.1.2.1 T-Channel Analog Signal Processing

The T-channel analog electronics amplifies each of the very low signal level T detector element signal outputs, clamps the bias offset level to a dc voltage reference, selects the proper detector segment, (left, right or both), linearizes the output signal amplitude to equivalent blackbody temperature instead of radiance, provides T hot and cold monitor signals, and limits the signal video bandwidth for both the 40-kHz TF data and the 8-kHz TS data.

Figure 2.1.2-1 is a block diagram of the T-channel electronic mechanization from the detectors through the channel output to the T-sample/hold and A/D converters. The T video from the first buffer is shaped by a six line segment (five break points) shaper function which linearizes signal to temperature. The T left/mid/right switching for TF data is located after the buffer amplifier following the shaper function so that continuous T video is available for TS data. Switching is at a high signal level so transient suppression is excellent. The T-left and T-right shaped video signals from the shaper output buffer amplifier are summed by R1 and R2 into the TS five pole, 8 kHz active low-pass filter. The output buffer amplifier also feeds the T-right, T-mid, and T-left switching gates for TF video which is supplied by the TF five pole 40 kHz active low-pass filter.



• Redundant bias circuit for OLS 13-16.

Figure 2.1.2-1. T-Channel Analog Signal Processing

Two kinds of redundancy are provided:

Normal Operation

In the analog hardware all circuits after the post amplifier/gated clamp are duplicated. The redundant buffer amplifiers, shaper networks, segment switching gates and TF and TS low pass filters are all identical to the primary hardware. They are continuously active and the choice of which hardware source of data outputs to use (TF and TS primary or TF and TS redundant) is made by ground command selection.

Fallback Mode

If a failure occurs in one detector element, preamplifier, commandable gain amplifier or post amplifier/gated clamp, the opposite detector segment signal can be used across the entire scan to provide TF data. TS data will also switch to the same single segment source. The redundant switching will be accomplished by a change in the T gate waveform timing commands. This T fallback mode is selectable by ground command.

2.1.2.1.1 T Detector Temperature Control

A low bandwidth, high gain temperature control loop is incorporated into the T channel to hold the T detector temperature constant. An individual set point temperature is selected for each cone cooler. The gain of the loop is set so the T detector temperature will vary less than $\pm$0.1°K over the full cone cooler inner stage heater power range of zero to 50 milliwatts maximum. Very tight temperature control is necessary since measured data on typical HgCdTe detectors show responsivity variations of -5%/°K. The T detector cold patch (oven) heating voltage is sampled and provided as a telemetry output for equipment status monitoring as are the detector cooler inner stage and outer stage temperatures.

Circuits are also provided for simultaneously switching the 1 watt inner stage de-icing heater and the 10 watt, 28 volt dc outer stage de-icing heater on or off by ground command. An analog EST is provided on the 1 watt heater voltage.

2.1.2.1.2 T Channel Preamplifier

The T channel preamplifier assembly which is located on the Sensor Subsystem (SSS) contains three separate circuits: a bias supply, and identical T left and T right preamplifiers. The supply section provides a very low noise, very low ripple -10 volt dc voltage source for both of the preamplifiers and for both of the selected resistors that set each detector segment bias current to their optimum value. Because of their very high gain of 1000, the preamplifiers raise the noise and the signal voltages developed by the detectors to a level well above the noise level of the T postamplifier circuits. The preamplifier -3 dB pass band is approximately 0.02 Hz to about 200 kHz.

The T channel video signal leaves the SSS after the preamplifier and is fed to a differential receiver and amplifier located in the Power Supply Unit (PSU). This amplifier has a gain of 1.5. As shown in Figure 2.1.2-2 a +5 volt dc offset is injected to nearly cancel the T preamplifier output -5 volt dc level that the video rides on.

2.1.2.1.3 T Channel Commandable Gain

The T channel commandable gain circuitry provides ground command gain change capability in the T channel. This may be necessary if channel sensitivity becomes degraded through optical contamination, detector temperature increase or other channel changes. It is a 4-bit gain changer located between the T preamplifier and the T postamplifier (gated clamp stage), after the differential receiver amplifier stage. Sixteen discrete gains can be commanded. Figure 2.1.2-2 is a block diagram of the signal flow through the two commandable gain circuits. The output goes from 0 dB to a maximum of +3.4695 dB (1.4910 ratio) in 15 steps of nominally 0.2313 dB (1.0270 ratio) each. The initial T gain used during factory adjustment and calibration of the T channel is usually $(0100)_2 = 4$.

The T left gain and the T right gain can be independently commanded to any of the sixteen gain values in a 50-3-0LS.

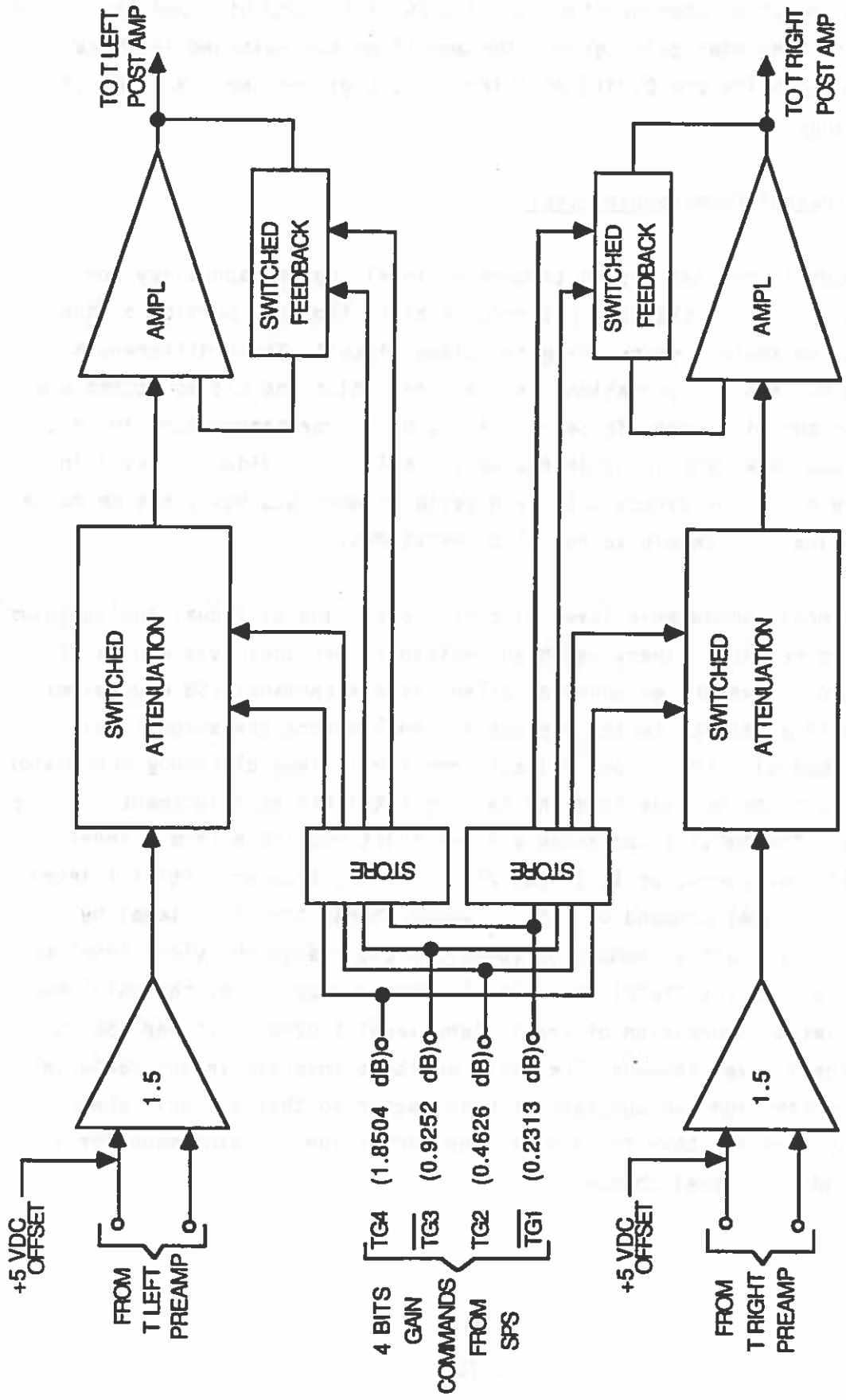


Figure 2.1.2-2 T Channel Commandable Gain Amplifier Block Diagram

The switched attenuator provides the 0.4626 dB (second bit) and the 1.8504 dB (fourth bit, the MSB) delta gains. The amplifier has switched feedback resistors that provide the 0.2313 dB (first bit, LSB) and the 0.9252 dB (third bit) gain changes.

2.1.2.1.4 T Channel Commandable Level

The T channel provides ground command dc level change capability for offset differences in background radiance received from the portion of the telescope not corrected for by the gated clamp circuit. These differences eminate from temperature variations in the fore-optics and are monitored via a thermistor on the M1 mirror. To correct for a M1 mirror temperature increase, the T commanded level should be decreased (to pull the T video dc level in the less positive or colder direction). Each serial number OLS has a custom table of command value of T levels versus M1 temperatures.

The T channel commandable level circuit, consisting of 2 dual analog gates and a set of precision, binary weighted resistors, provides, via 4 bits of ground command, 16 values of added dc offset levels (nominal LSB equivalent to 1.02°K shift at 210°K) to the T clamp dc level before the shaper. This signal is summed with the shaped voltage from the T clamp blackbody thermistor circuit and with the voltage from the factory-set T offset adjustment potentiometer. The total T commandable level shift available from T level command is fifteen steps, or 15.3° (at 210°K). Thus, from an initial T level of $(1000)_2$, a T level command of $(1111)_2$ would change the video level by +7 steps or +7.16°K and a command of $(0000)_2$ would change the video level by -8 steps or -8.18°K (at 210°K). For signals warmer than 210°K, the main shaper function causes a compression of the T video level 1.02°K shift per LSB at 210°K from the T level command. The level shift is inserted in the radiance domain before the high end compression main shaper so that a T gain change theoretically does not have to be made when correction is being made for a background radiance level change.

2.1.2.1.5 T Channel Postamplifier

Each T commandable gain amplifier output directly drives a T postamplifier stage with a gated clamp around it for dc restoring. The postamplifier gain is adjustable in thermal vacuum at system level test via a potentiometer and is typically set to provide 5 volts full scale channel output with the T commandable gain at (0101)2 Independent of the input signal to the detectors, the outputs of both the left and right postamplifier stages are clamped during the T clamp gate pulse (2.5 millisecond pulse at an interpulse period of 168 milliseconds) to the reference voltage supplied to the noninverting input of this operational amplifier stage. The gated clamp around the amplifier stage has both the dynamic range of a gated clamp at the input and the drift stability of a gated clamp at the output. The T clamp pulse occurs at the peak -Z scan angle.

The T channel is clamped while the T detector is viewing the variable temperature (240 +12/-13°K) T clamp blackbody during -Z overscan. The temperature of this source is sensed by a thermistor network with the output shaped to provide the desired characteristic of nonlinear output voltage versus temperature. The output of this network is used as part of the T channel video dc level restoration. For a variance of the 240°K T clamp blackbody source from 227°K to 252°K, inclusive, the desired characteristic is achieved within ±0.21°K peak and 0.16°K rms (for 210°K targets). One clamp source is used for referencing both the T left and the T right postamplifiers. However, independent dc amplifiers are provided on both T left and T right to provide the level shift, amplification, and system level adjustment of T channel offset and postamplifier gain. By dc restoring to a temperature near midscale (240°K typical) instead of to free space temperature, any detector responsivity changes cause a pivoting action of the slope of the channel transfer function about this near-center point. This action reduces peak error compared to pivoting about a clamp which is beyond the end-point of the range.

2.1.2.1.6 T Channel Shaper

The T video signal from the first buffer amplifier is shaped by the main T shaper function circuit. This biased diodes and resistors nonlinear shaping network compensates for the nonlinear input radiance versus scene temperature relationship (Planck's Law for the OLS T spectrum). This network makes the T channel output signal voltage amplitude proportional to the equivalent blackbody temperature of the scene. It has a passive signal voltage high end compression function with five inflection points and six linear segments of decreasing slope. The peak shaper network error referenced to the ideal linear scale factor at the network output is -0.35°K for 195°K targets, but only -0.28°K in the 210 to 310°K range. The rms error over the 210 to 310°K range is 0.15°K rms.

A standard noninverting high input impedance operational amplifier stage is used as a buffer between the high output resistance of the nonlinear shaping network and the reasonably low input resistance of the analog filter stage. The gain of this stage is set at 1.488 to raise the 0 to 3.361 volt dc shaper network output range to the desired 0 to 5 volt dc output range required at the TF and TS filters.

2.1.2.1.7 T Channel Data Switching

The T left buffer amplifier output is coupled through a series JFET analog gate switch to the TF low pass filter stage input. The logic signal to the gate will have the left gate ON during the time the T detector is scanning between -56 and -41 degrees. Similarly, the T right analog gate switch will enable the output of the T right buffer amplifier during the +41 to +56 degrees scan angle. The left and right segments are summed and averaged for the midsegment of scan between -41 and +41 degrees for TF. The T left and T right signals are summed and averaged for the entire scan angle for TS video. Figure 2.1.1-4 shows the T channel switching and signal summing described above.

2.1.2.1.8 T Channel Output Filters

Separate active T output filters provide the TF and TS analog data outputs. Each filter is a five-pole Butterworth low pass response with -3 dB corner frequencies of 40 kHz for TF and 8 kHz for TS. The T video output scale factor is 41.67 mV/°K (0.00 to +5.00 Vdc for 190 to 310°K). Both the primary and redundant T channels have their own pair of filters: primary TF/TS and redundant TF/TS; respectively.

2.1.2.1.9 T Cal and T Clamp

A standard sample and hold circuit is connected to the filter output for acquisition of EST and formatted reference data. This circuit (over its two scans cycle period) sequentially samples during both ends of scan time and holds, for approximately a scan line each, in sequence:

The left channel clamp output signal (cold)
The right channel calibration signal (warm)
The right channel clamp signal (cold)
The left channel calibration signal (warm)

The above is accomplished with only one circuit, utilizing logic signals controlling the T left gate, T right gate, and the T cal and T clamp read gates. The resulting 5.94 Hz square wave signal output is provided on the T Cal/T Clamp equipment status telemetry (EST) signal. The T Cal and T clamp output data is also converted by a 10 bit A/D and the most significant 8 bits plus a left/right identification bit are inserted in the Stored Data Subsync Frame.

2.1.2.2 L Channel Analog Signal Processing

The very low level HRD and PMT detector signal outputs are amplified to digital processing levels and filtered in the analog electronics section. Figure 2.1.2-3 is a block diagram of the L channel electronic mechanization from the detector input through the channel output to the L channel A/D

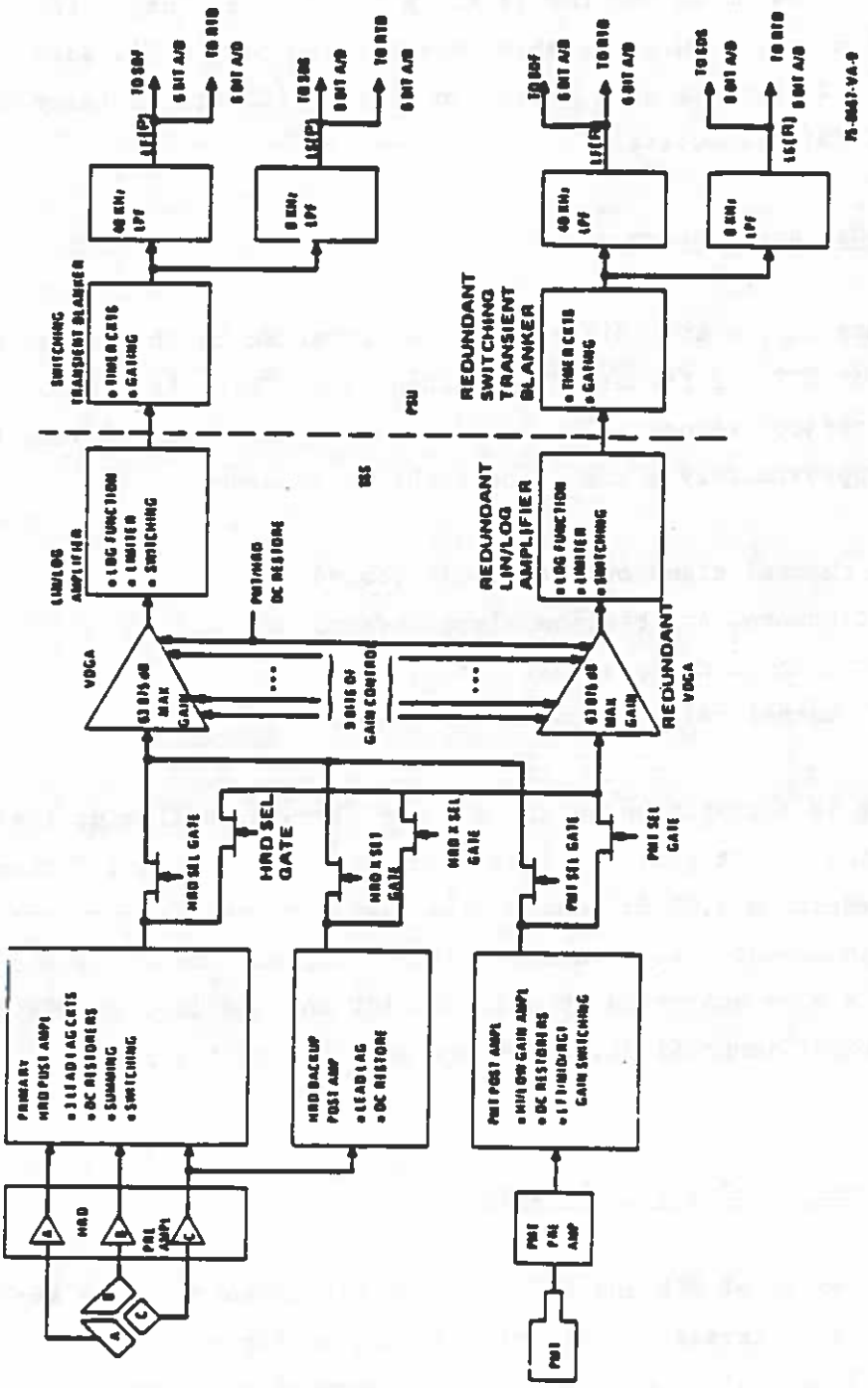


Figure 2.1.2-3. L Channel Analog Signal Processing Block Diagram

converters. Zero input (dark reference) restoration to zero dc signal level is accomplished at the -Z end of scan. Detector and detector segment selection is accomplished in response to processor command signals. The proper postamplifier selection and variable digital gain amplifier (VDGA) gain value selection are also provided under processor control. Amplification may be linear or 2 decade logarithmic compressed by ground command selection. End-of-scan calibration signals are provided for the output data format. Switching transients are suppressed in the switching transient blanker. Finally, before signal delivery for digital processing, presample low-pass filtering limits the Light Fine (LF) data signal to 40 kHz and the Light Smooth (LS) data signal to 8 kHz video bandwidth.

The L channel has two kinds of redundancy provided:

Normal Operation

In the analog hardware all circuits after the postamplifier outputs are duplicated. This includes the redundant source selection gates, VDGA, lin/log amplifier, switching transient blanker, and LF and LS low pass filters which are all identical to the primary hardware. They are continuously active and the choice of which hardware source of data outputs (LF and LS primary or LF and LS redundant) to use is made by ground command selection.

Fallback Modes

A HRD Segment C fallback postamplifier is provided which can be selected by ground command for use across the entire scan in the event that the common summing amplifier stage or DR amplifier (Figure 2.1.2-4) of the HRD post-amplifier were to malfunction. In addition, the gating logic can be changed by ground command to select either HRD left or HRD right for use across the entire scan line to bypass a failure in one L-day detector segment, or preamplifier, or postamplifier.

2.1.2.2.1 HRD Signal Processing

Each of the three HRD segments has its own separate transimpedance type of preamplifier stage consisting of a low noise dual JFET source follower and a low noise operational amplifier. The load resistor that determines the preamplifier gain is a 44 megohm low capacitance component.

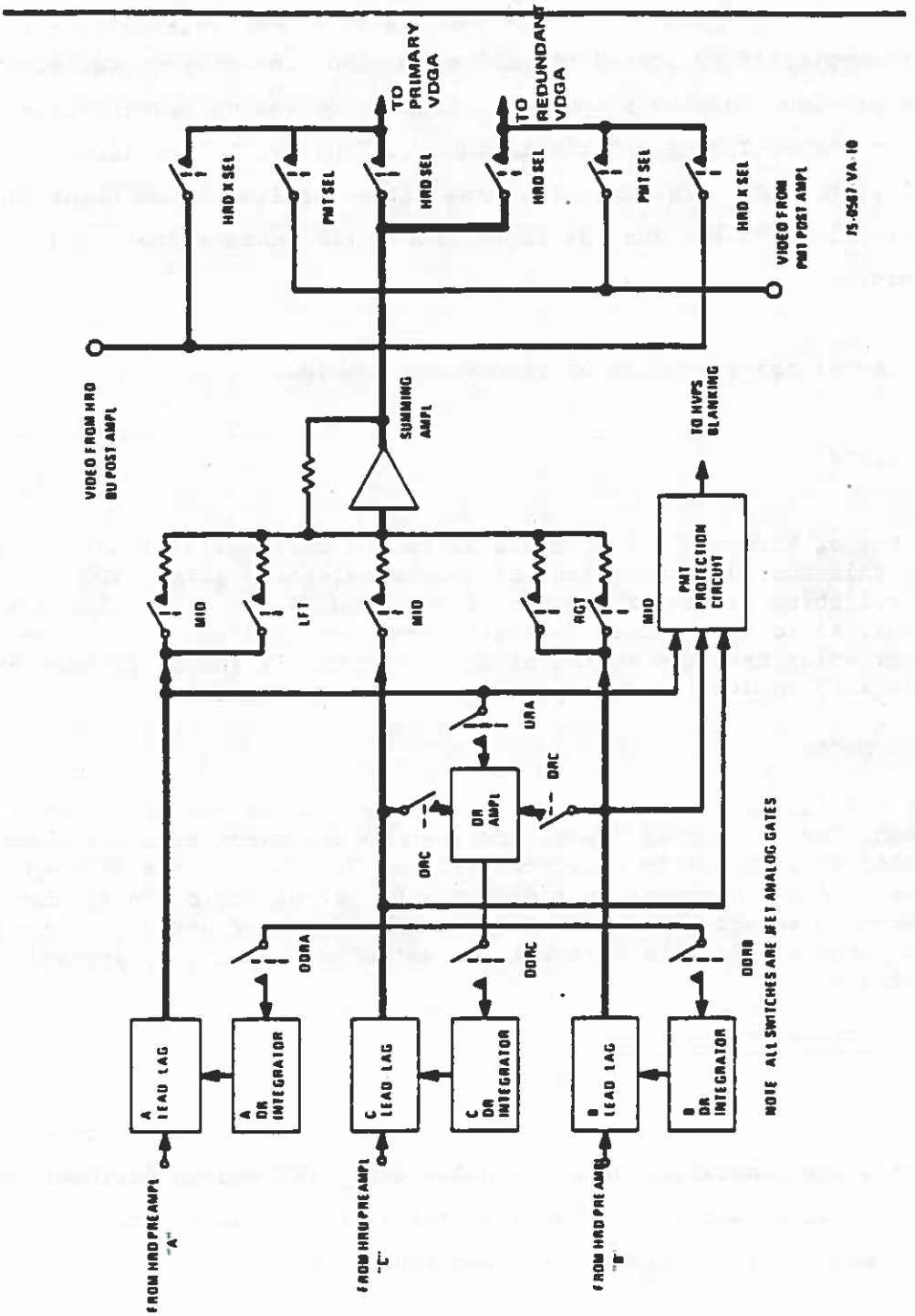


Figure 2.1.2-4. Primary HRD Postamplifier Block Diagram

The HRD postamplifier dc restores the three segment signals from the three HRD preamplifiers and switches the gain and summing so as to yield a single scan line L-day video output. Figure 2.1.1-4 shows the HRD channel switching and signal summing. On the -Z end of the scan, segment A is used., on the +Z end of the scan segment B is used, and on the central (nadir) region of the scan, between appproximately -41° and +41° of scan angle, detector segments A, B, and C are summed to provide the L-day video. Figure 2.1.2-4 is a block diagram of the HRD postamplifier. The lead/lag first amplifier increases the approximately 5 kHz, -3 dB signal bandwidth from the HRD preamplifier to be exactly 40 kHz. The lead/lag 5 kHz corner frequency and the gain are adjustable in all three lead/lag circuits. During the -Z (left) side of the scan, the LFT switch feeds the A detector segment signal to the summing amplifier. During the +Z (right) side of the scan, the RGT switch is enabled to feed the B segment to the summing amplifier. During the middle part of the scan the three MID switches are closed to sum all three detector segments, lower the gain, and feed the HRD signals into the summing amplifier. The processor segment gating logic can be changed by ground command to select the left, the right, or the mid (the sum of all segments) for use at all scan angles in case of a failure in one of the three segment channels. A ground command can also select the fallback postamplifier which is described in a paragraph below.

The HRD dark reference dc restoring technique results in low offset voltage and very low difference in offset between the A, B, and C sources as shown in the block diagram, the restoring is accomplished by switching DRA and DDRA together on the first -Z scan overtravel so the DR amplifier drives the DRA integrator and, therefore, the A channel offset towards zero. On the second -Z scan overtravel DR time, the DRB and DDRB gates are enabled and the DR amplifier is used to drive the B channel offset toward zero. On the third -Z scan overtravel DR time, the DRC and DDRC gates are enabled and the DR amplifier is used to drive the C channel offset toward zero. The sequence then repeats, beginning again with the A channel The offset of each of the three channels is detemined by the offset of the (common) DR amplifier and since, the same DR amplifier restores all three HRD channels, the offsets of the three channels will be equal. This means that theoretically there will be no

offset variation with HRD segment changes. The DR times are 2.5 milliseconds and the DDR times are 2 milliseconds. The two HRD SEL gates are enabled to feed L video into both VDGA's when the HRD is selected.

The PMT protection circuit limits the PMT maximum anode current to prevent damage and saturation recovery problems in bright light ambients The control signal (derived from the HRD channel) provides a blanking signal to the PMT high voltage power supply when the HRD light level exceeds a value that would produce a PMT anode current of greater than 2 microamperes. This protection circuit varies its gain to account for the PMT FOV (full, edge, or 1/9) selected. PMT blanking is also provided by SPS command. This processor input is OR-gated with the protection blanking provided from the HRD channel

The HRD fallback (or backup) postamplifier is similar to the C segment portion of the primary HRD postamplifier. Figure 2.1.2-5 is a block diagram of the HRD fallback postamplifier. The fallback postamplifier receives its signal directly from the C segment HRD preamplifier output, thus bypassing the primary HRD postamplifier entirely By using the C segment of the HRD detector, the large square, it is possible to obtain a very usable L-day signal over the full scan angle. DC restoration is performed by a DR amplifier and integrator. These are pulsed every third scan by the same DRC and DDRC logic signals used by the HRD segment C restorer in the primary HRD postamplifier.

The fallback postamplifier lead/lag network is the same type circuit used in the primary HRD postamplifier, adjustable for the segment C bandwidth and sensitivity. Output bandwidth after the lead/lag is 40 kHz. Nominal gain of the fallback postamplifier has been increased over that of the primary HRD postamplifier midmode (-41° to +41° scan) to compensate for the narrower instantaneous field of view, caused by the use of only detector segment C rather than by summing A, B, and C. When the two HRDX SEL gates are enabled, the output of the HRD fallback postamplifier is connected to both the primary VDGA and the redundant VDGA inputs.

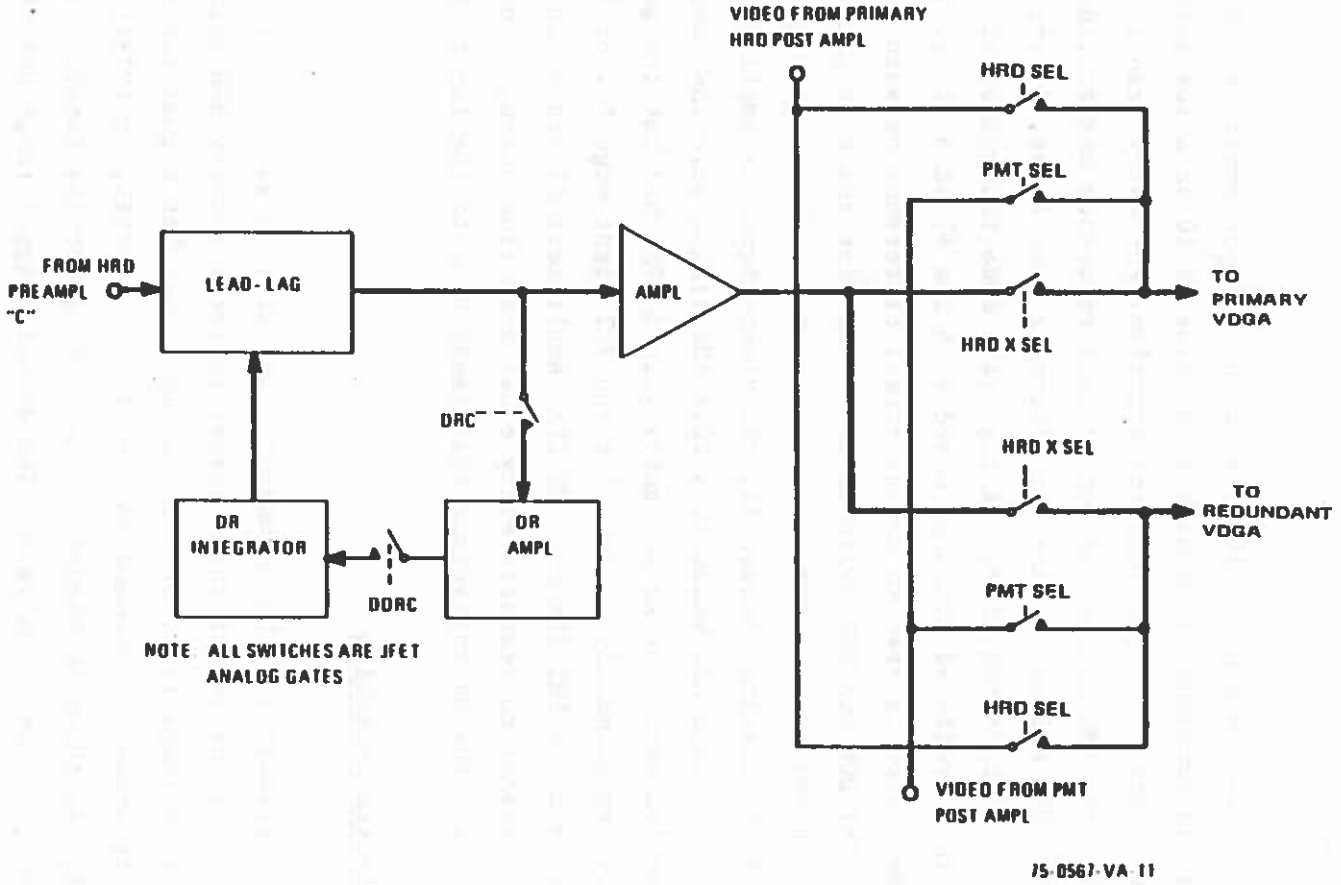


Figure 2.1.2-5. HRD Backup Postamplifier Block Diagram

2.1.2.2.2 PMT Signal Processing

The PMT has a single stage low noise transimpediance type preamplifier with a 3.92 Megohm low capacitance feedback resistor. Dual low noise JFET source followers provide high impedance input stage. The preamplifier's input is the photo-multiplier to be anode current. The preamplifier -3 dB bandwidth is about 45 kHz.

Figure 2.1.2-6 is a block diagram of the PMT postamplifier. Switched gain amplifier A1 is commanded to a high gain value of 10 or a low gain of 0.329 by the PMT Gain State (PGS) gain control function. For every scan line during the -Z overtravel the PMT is blanked for dc dark reference restoration of amplifier A1 by the PMT DR1 switch closure. On alternate scan lines, during the -Z scan overtravel dc restoration time, the high gain mode integrator or low gain mode integrator is dc restored synchro- nized with the A1 gain state. The same dark reference amplifier is used to the dc offset difference between gains is negligible. PMT DDH and PGS switches are closed for the high gain mode dark reference, and PMT DDL and PGS switches are closed for the low gain mode dark reference. After passing through A1, the video signal is amplified 1.5 times and filtered by stage A2, which is a 20.8 kHz single pole low-pass filter. The FOV compensation amplifier A3 has unity gain in PMT Mid but the gain is increased by approximately 3 times for the PMT Right edge FOV or Left edge FOV by means of switches PMT RPA and PMT LPA. Amplifiers A2 and A3 in series are also dark reference dc restored every other scan line during -Z overscan by gage PMT DDH and the DR integrator that feeds back to the input of A2.

2.1.2.2.3 L-Data Switching

Both the primary and the redundant video digital gain amplifiers (VDGA's) may be driven by any one of three signal sources: primary HRD postamplifier, fallback HRD postamplifier, or PMT postamplifier. The signal source is selectable by processor command on the HRDSEL, HRDXSEL, or PMTSEL logic lines, respectively, as shown in Figure 2.1.2-7. The switching function is performed by JFET analog transmission gates. The dynamic signal range has been extended to -7 volts on these six analog gates by powering them from unregulated -13.5

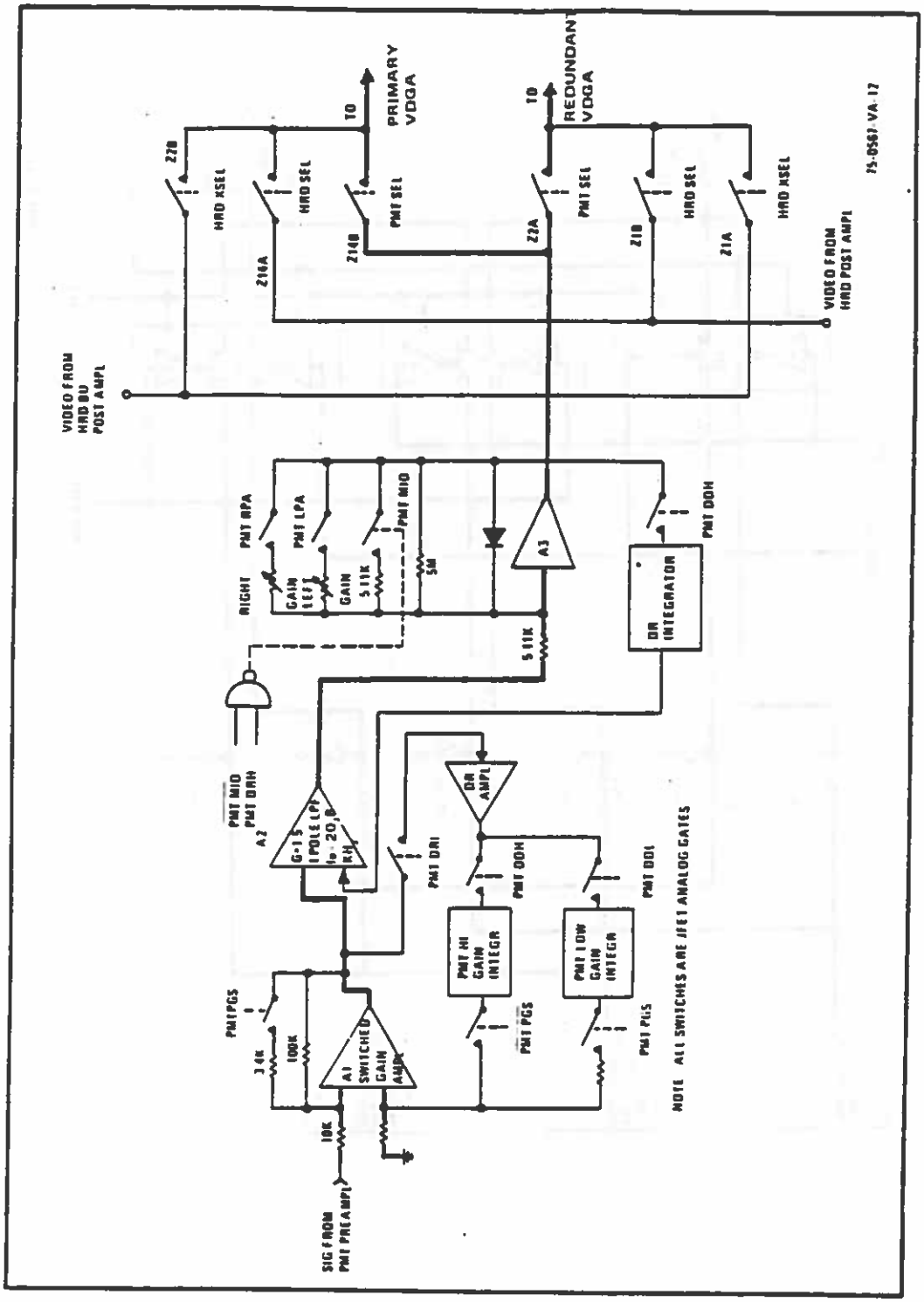


Figure 2.1.2-6. PMT Postamplifier Block Diagram

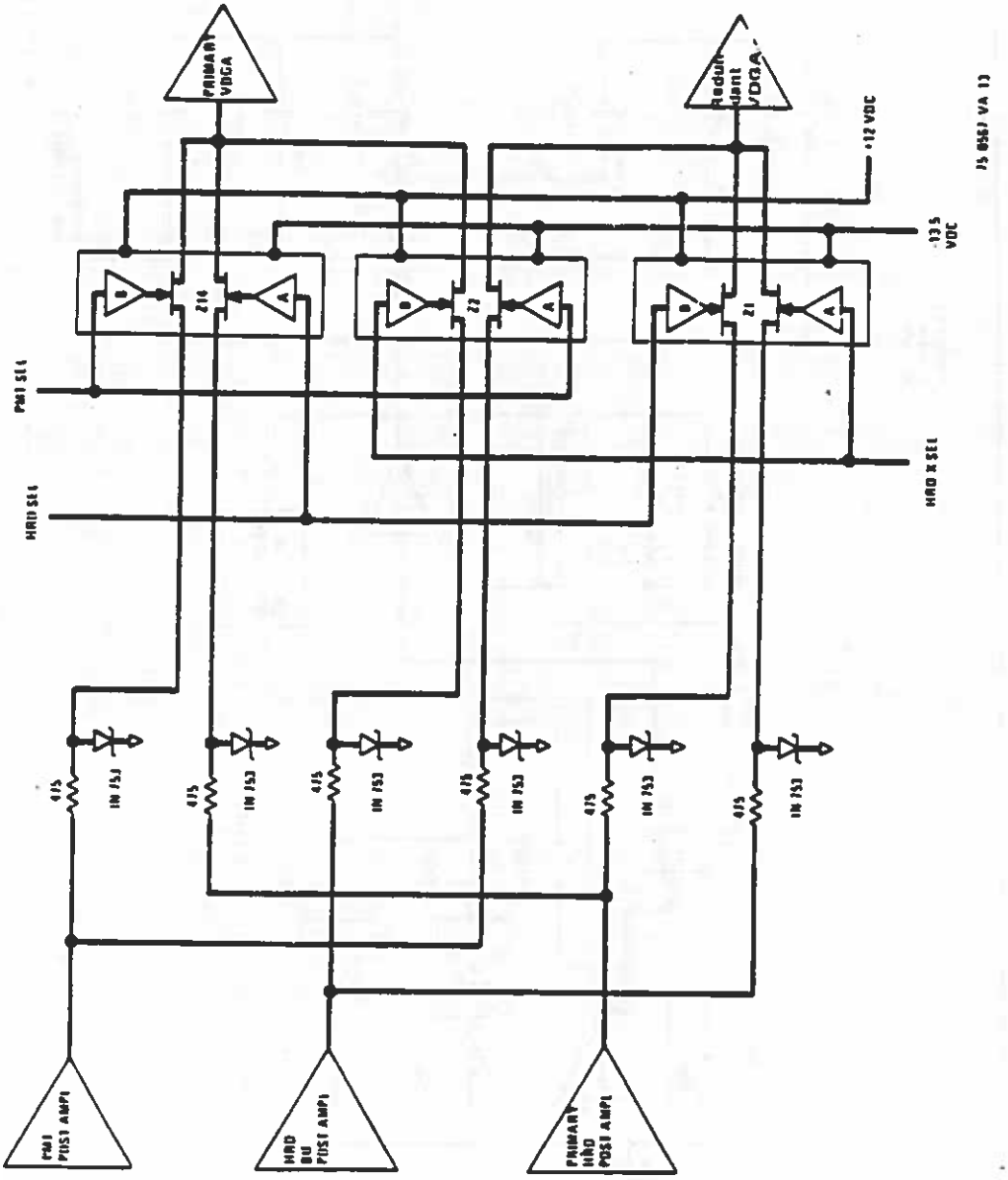


Figure 2.1.2-7. L Data Switching Schematic

volts dc instead of -12 volts dc. The input signal range is limited by resistor and zener diode networks at each switch to a nominal -6.2 volt maximum swing. Video is negative-going for increasing light level at this point.

2.1.2.2.4 Video Digital Gain Amplifier (VDGA)

The primary and redundant VDGA's are identical. Each VDGA has nine bits of logarithmic (decibel) increments of gain control. These 9 bits produce 512 discrete gain states from 0 to 63.875 dB in 0.125 dB steps. The smallest gain step (LSB) is 0.125 dB and the largest step (MSB) is 32 dB. The VDGA consists of five inverting amplifiers; the output range is 0 to +5.0 volts and the full power bandwidth exceeds 200 kHz. Figure 2.1.2-8 is a block diagram of the VDGA.

The VDGA gain is controlled by nine primary lines of command bits from the gain control function in the SPS that commands 0.125, 0.25, 0.5, 1, 2, 4, 8, 16, and 32 dB amplifier-attenuator combinations. The actual gain switching is accomplished by analog gate-switched T pad network attenuators in the input and feedback paths of the operational amplifiers. The first two amplifiers together provide the 32 dB gain delta and the third amplifier provides the 16 dB gain delta. The fourth amplifier provides the 8 dB, 0.125 dB, and 0.25 dB gain deltas. The fifth amplifier provides the 0.5 dB, 1 dB, 2 dB, and 4 dB gain changes.

DC dark reference restoration of the VDGA is provided by the HRD postamplifier source and the PMT postamplifier source on two interleaved alternate scans. During the -Z scan overtravel blanking time, gates are alternately enabled to a pair of rebalance integrators. During dc restoration time, the VDGA is commanded to the maximum gain condition. HRD SEL and PMT DDH gates operate together for the HRD DR integrator PMT SEL and PMT DDL gates operate together for the PMT DR integrator on the -Z scan overtravel during which the PMT postamplifier third stage is not being dark referenced.

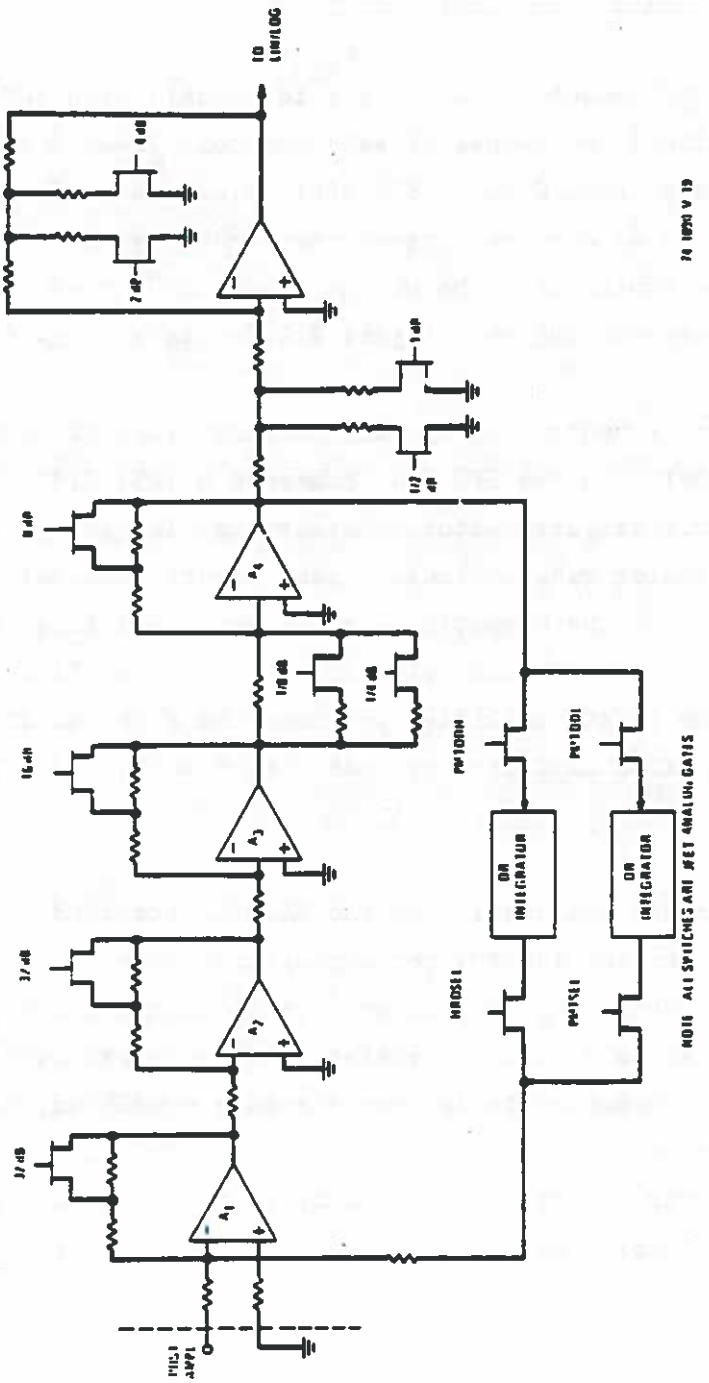


Figure 2.1.2-8. VDGA Block Diagram

2.1.2.2.5 LIN-LOG Amplifier

The primary and redundant LIN-LOG amplifiers are identical and the following description applies to both.

The LIN-LOG amplifier either passes the VDGA signal unaltered from its input to the output (linear mode) or provides an output proportional to the logarithm of the input signal level (log mode). The selection of linear or logarithmic mode is made by ground command. Higher level signal voltages (brighter scenes) are compressed by the log function. The linear mode is a direct path through the LIN analog switch, as shown in Figure 2.1.2-9, the LIN/LOG amplifier block diagram.

A two decade logarithmic function output voltage versus a linear input voltage characteristic is achieved by using a well-known nonlinear characteristic of diffused base Silicon bipolar transistors. A limiter consisting of stages A1 and A2 at the input of the log mode path clips off negative-going peaks for inputs less than +50 millivolts to prevent the log amp small signal (ac) gain from rising towards infinity as the input signal falls towards zero.

A midscale dc calibration point (0.5V in, 2.5V out) on the log amp characteristic is established during each dark reference level restoration. This reference level is established by inserting a known input current and dc clamping the log amp output to a desired voltage. The A3 input calibration current is made equal to the midrange value of input signal current while the output of amplifier A4 is dc clamped to the mid range value of output voltage. Thus, the condition is established where a nominal input voltage of 0.5 volt gives a log amplifier output of 2.5 volts. The gain gives a 2.5 volt change at the log amplifier output for a decade (20 dB) change from nominal input voltage. The log amplifier equation is:

$$V_o = 2.5 \log (V_{in}/0.05)$$

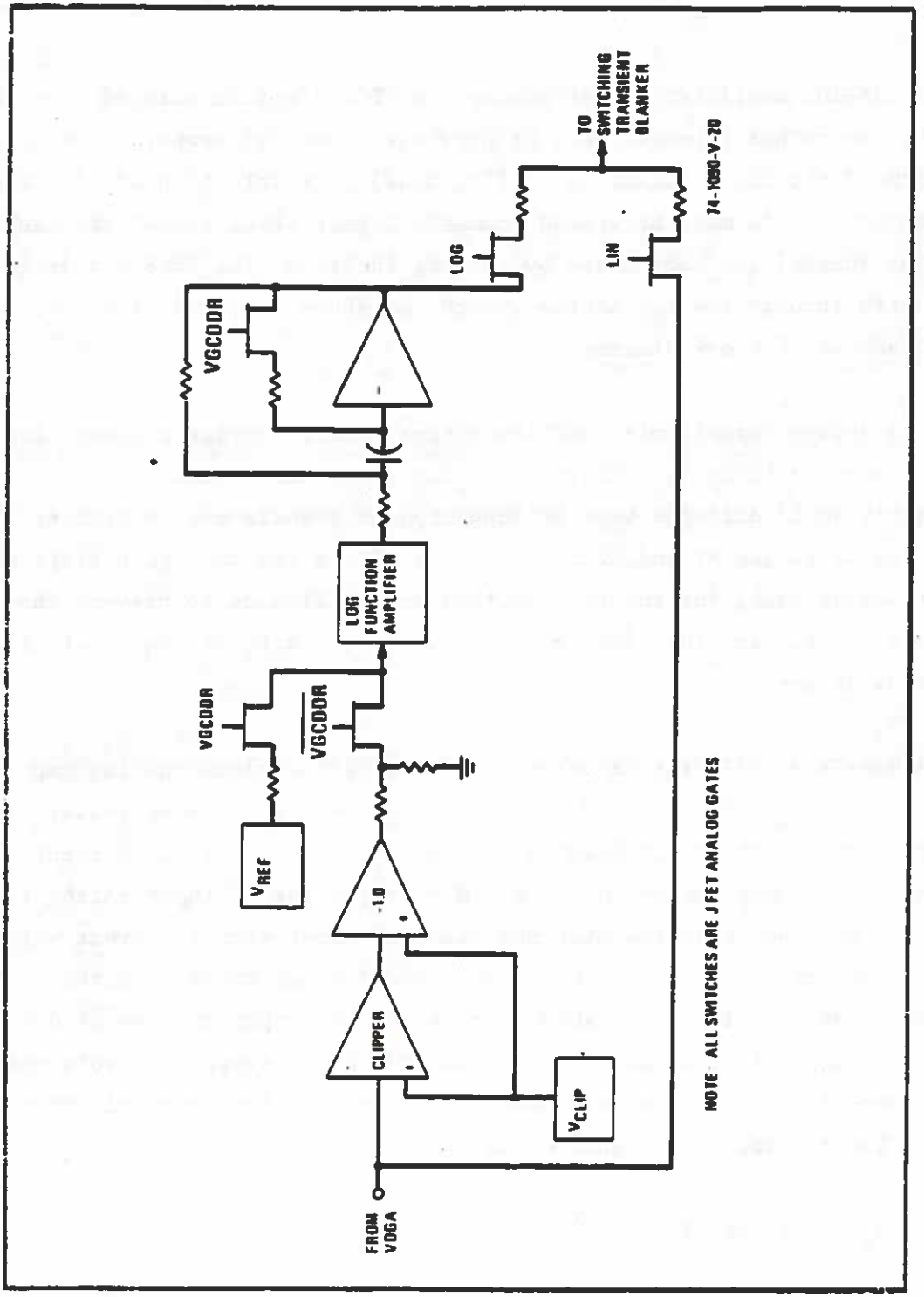


Figure 2.1.2-9. LIN/LOG Amplifier Block Diagram

where V_{in} and V_o are in volts. The log mode input to output relationship is shown in Figure 2.1.2-10.

2.1.2.2.6 Switching Transient Blanker

The primary and redundant transient blankers are identical and the following description applies to both.

The switching transient blanker opens the L video path for the duration of gain segment selection and PMT/HRD source switching transients, outputs the held level of the previous video signal value during a short blank time, and returns to normal L video after the transient. It is a track and hold function. This technique suppresses transients satisfactorily because it removes the energy of narrow, fast transients at a point in the L channel signal flow where the channel has wide bandwidth just ahead of the LF and LS low-pass filters. This reduces the transient expansion in time by the ringing of the LF and LS Butterworth analog low-pass filter's impulse response.

Figure 2.1.2-11 is a block diagram of the switching transient blanker. The blanker analog JFET gate opens and holds the signal value before the switching transient has moved significantly toward its peak voltage at the switching transient blanker low-pass RC filter output. This causes the energy content of the switching transients into the LF and LS filters to be reduced. The low-pass $(R1+R2)C_1$ time constant is 0.82 usec and the equivalent single pole lowpass filter bandwidth is 194 kHz. Capacitor C_1 also serves as the "boxcar" holding capacitor for the unity gain noninverting follower buffer amplifier. The gate driver circuit is fed by the OR gate output whose multiple input is a series of balanced R-C timing circuits which generate blanking pulses. Two R-C circuits are used in series for each pulse generated to compensate for threshold level variation of the CMOS Logic and for temperature compensation.

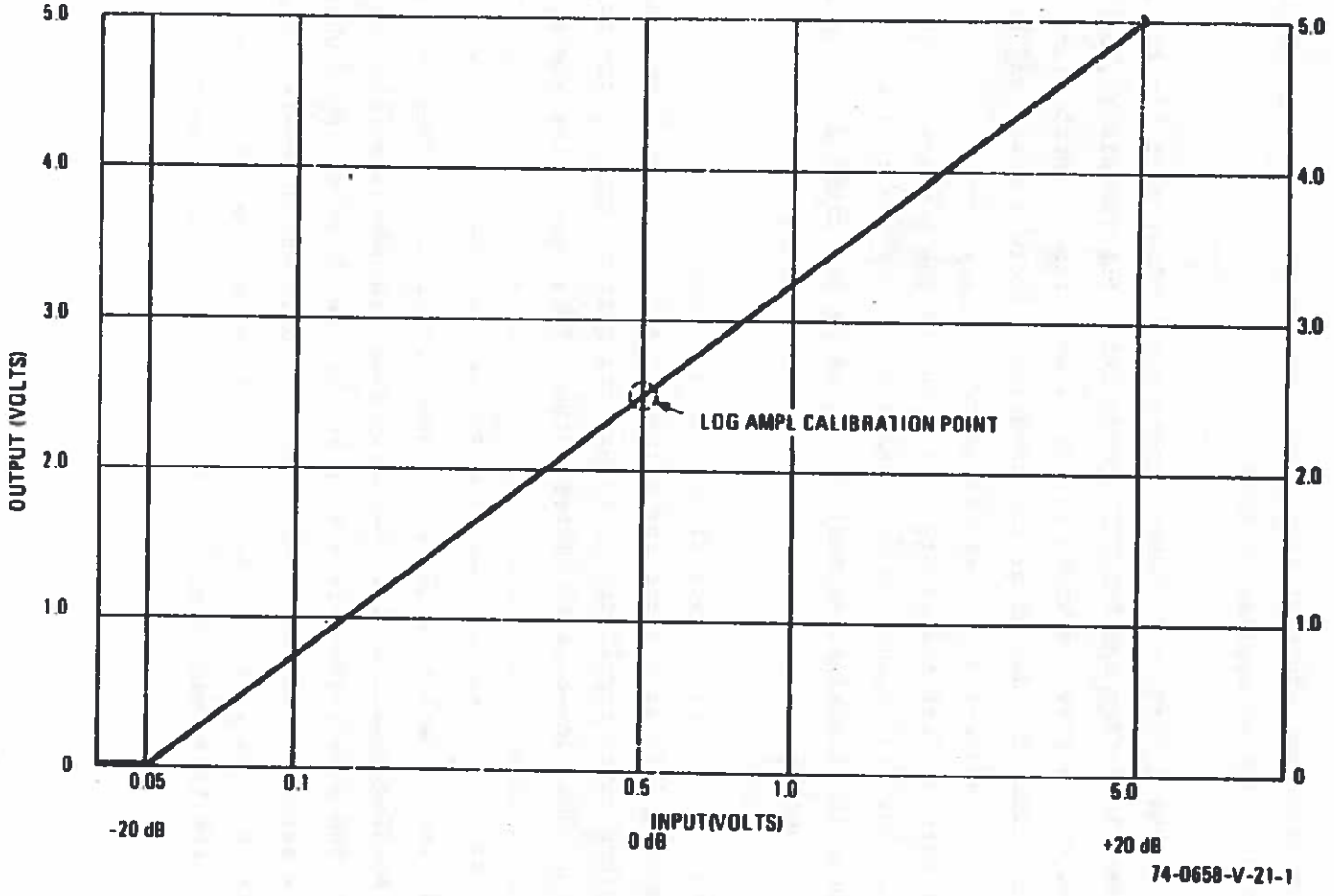


Figure 2.1.2-10. L Channel Log Mode Amplitude Transfer Function

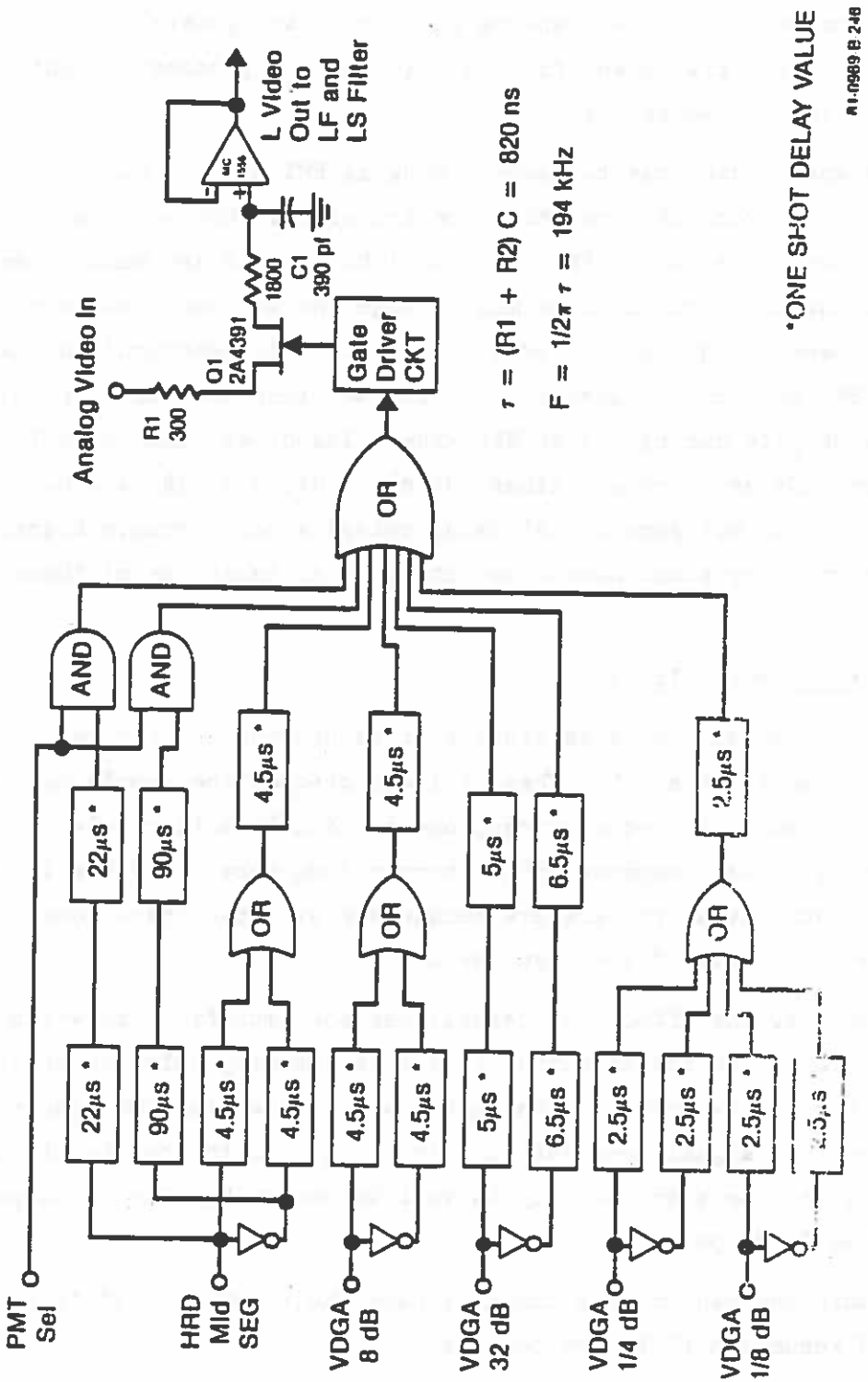


Figure 2.1.2-11. Switching Transient Blanker

Five input signal lines from the processor are used to generate blanking pulses corresponding to the location of the most objectionable transients visible to the L channel data. The blanking pulse circuits generate pulses synchronous with both the rising and falling edges of the procesor output gain and segment selection waveforms.

The HRD MID signal, which has the same timing as PMT MID, is used to generate pulses for blanking HRD and PMT video transients that occur at the edge/mid and mid/edge transitions. PMT LS channel transients are much wider than HRD, so blanking times of 180 usec mid to edge and 44 usec edge to mid are used versus 9 usec (either mid to edge or edge to mid direction) for HRD LF blanking. The PMT SEL line is used to inhibit the wider PMT blanking pulses from reaching the OR gate during use of HRD video. The other blanking pulses are generated from VDGA gain command lines: 32 dB, 8 dB, 0.25 dB, and 0.125 dB. The other dB bits do not generate blanking pulses since adequate transient suppression is provided by simultaneous switching of at least one of these four commands.

2.1.2.2.7 L Channel Output Filters

The two L channel output low-pass video filters provide the two resolution data type analog outputs: LF and LS. These filters precede the sample/hold and A/D converters. The temporal frequency response is ideally a five-pole Butterworth low-pass filter response with a corner frequency of 40 kHz for LF and 8 kHz for LS. Both output filters are mechanized by a two operational amplifier noninverting active filter synthesis.

For the HRD source, the effective preamplifier/postamplifier bandwidth is a 40 kHz single pole lag so the LF output filter is actually only the other four low-pass poles (the two complex conjugate pairs). When the PMT source uses the LF filter, the signal bandwidth is limited due to the optical field of view of the PMT and the scan velocity to well below 40 kHz. The LS output filter has all five 8-kHz poles.

Both the primary and redundant L channels have their own pair of filters: primary LF/LS and redundant LF/LS, respectively.

2.1.3 Digital Processing

The digital processing circuitry, as shown in Figure 2.1.3-1 consists of two identical sets of circuits, subdivided and switched so that a working system may be configured out of combinations of working sections from each side.

The Processor is a low-power general-purpose computer. Its operational program is contained in the Memory which has both Read Only Memory and Random Access Memory sections. The Processor and Memory sections communicate by "Signal BUS A" or "Signal BUS B" (e.g., this allows Processor C to be used with Memory F over BUS B), so that there are eight possible combinations.

The Input/Output Units contain several cross-switchable functions under direct processor control. An I/O unit responds to processor commands coming over either signal BUS A or signal BUS B. With both I/O X and I/O Y powered up and operating independently, choices may be made as to which I/O controls each of the functions such as:

Spacecraft Interface
Data Control
Sensor Control
Output Data Multiplexing and Tape Recorder Control
Encoder and Wow/Flutter Processing

It should be noted that the basic "I/O Control" section within each I/O must be working properly to use any of the functions in that I/O.

The formatter units contain the circuitry which performs analog-to-digital conversion on the video signals, processes the digital video as required, adds additional information and organizes the result, using synchronization codes, into various formats for transmission to the ground. If both Formatter G and Formatter H are powered up, each of the following functions may be performed by either Formatter unit.

Real Time Data Formatting
Stored Data Fine Formatting

Stored Data Smooth Formatting
Special Sensor Processing

The formatters communicate with the processor through the I/O unit selected by IFSEL from the spacecraft. It does not matter to the Formatters whether one or both I/O units are powered up, or what functions are being performed by either I/O. The Formatter Memory, which is used mainly by Stored Data Smooth and to a certain extent by Stored Data Fine, is connected only to the SDS and SDF blocks within its own Formatter.

The OLS requires a sequence of events to make it operational. The power relays must be configured to select the desired Processor, Memory, I/O, Data Processors, Analog Electronics, and Motor Controller. The Spacecraft Interface selection (IFSEL) then steers the Set Load Processor line to the selected processor.

The OLS power supply may now be enabled and the data busses selected. Resetting the Load Processor line allows the operational program to be loaded and initiated. The OLS will now accept commands for redundant function selection, gain control, Data Formatter Selection; process elapsed time count, telemetry, Encoder, and Wow Flutter information; and will accept other commands. Figure 2.1.3-2 OLS Control Paths shows the 4 major redundant functions and the sixteen bit wide control data paths that connect them. Figure 2.1.3-3 I/O Function Control shows the major I/O Functions and the control paths that enable them. Figure 2.1.3-4 Formatter inputs and control shows the major inputs to the four Data Formatters and the control lines that enable them. Figure 2.1.3-5 OLS Data Path Control shows how the redundant Data Formatters are interconnected and the control lines that select the data paths.

2.1.3.1 Processor and Memory

A block diagram showing the relationship between processor, memory and I/O is in Figure 2.1.3.1-1.

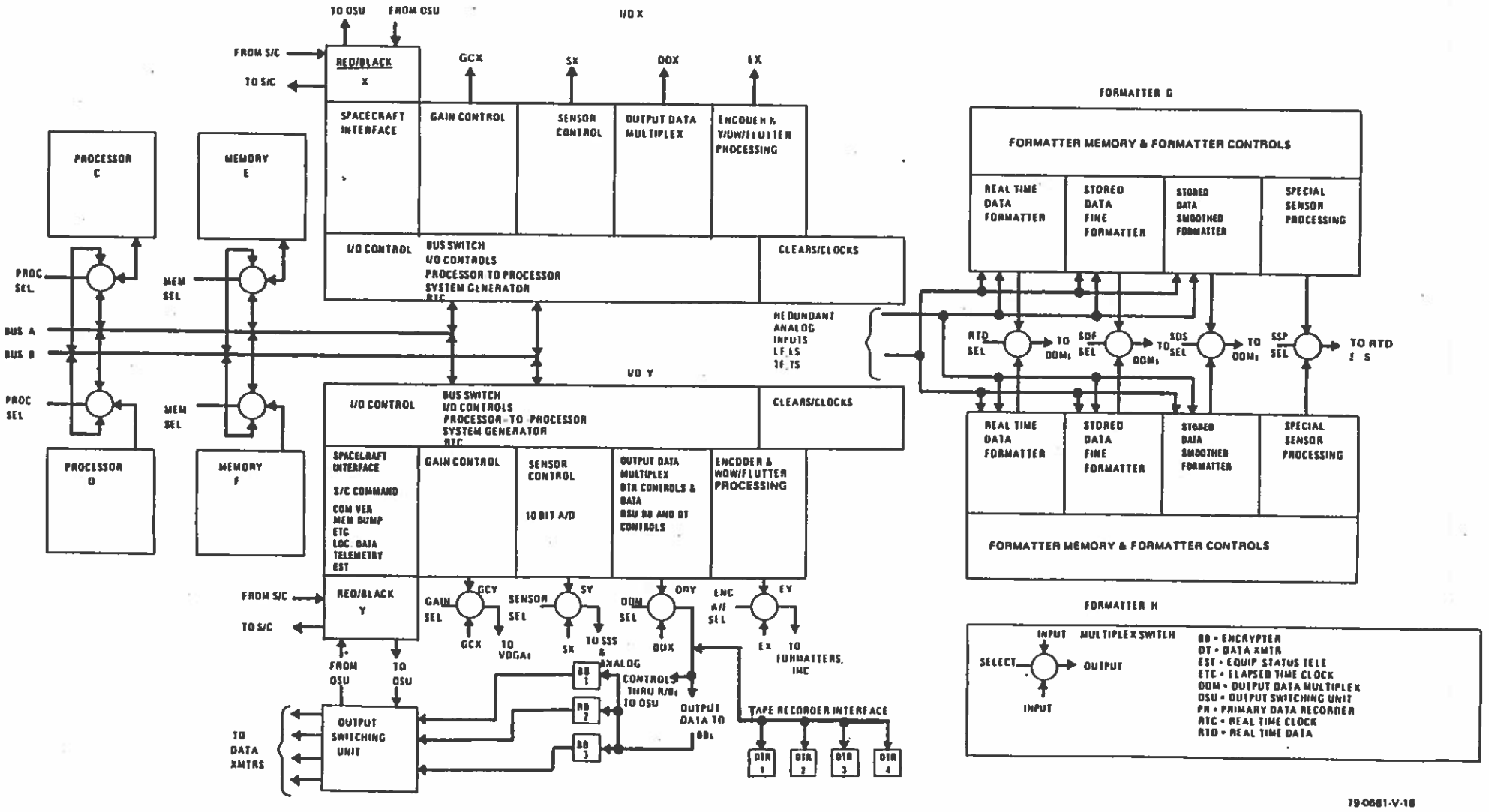


Figure 2.1.3-1. 5D-2/5D-3 Digital Processing Diagram

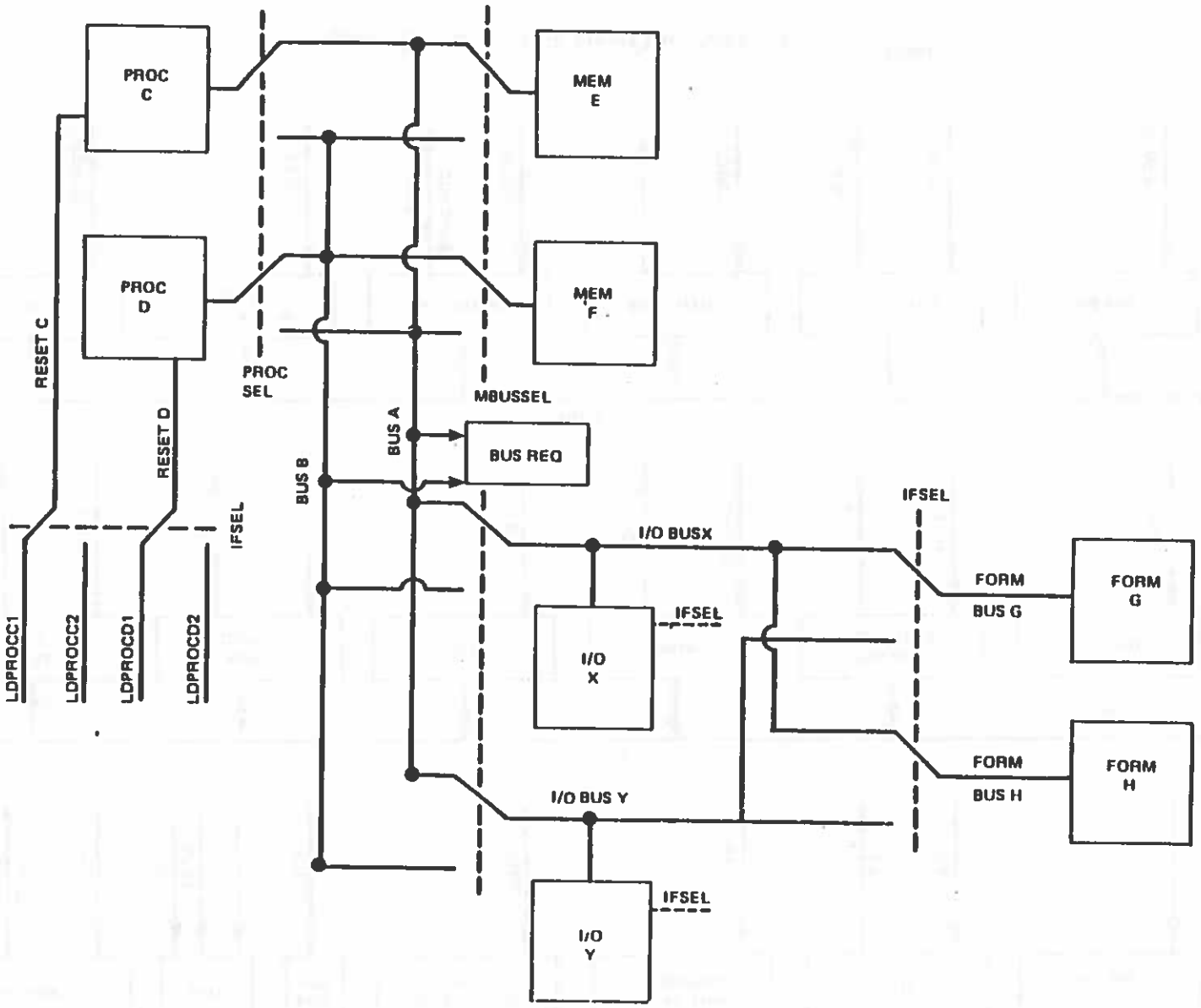


Figure 2.1.3-2. OLS Control Paths

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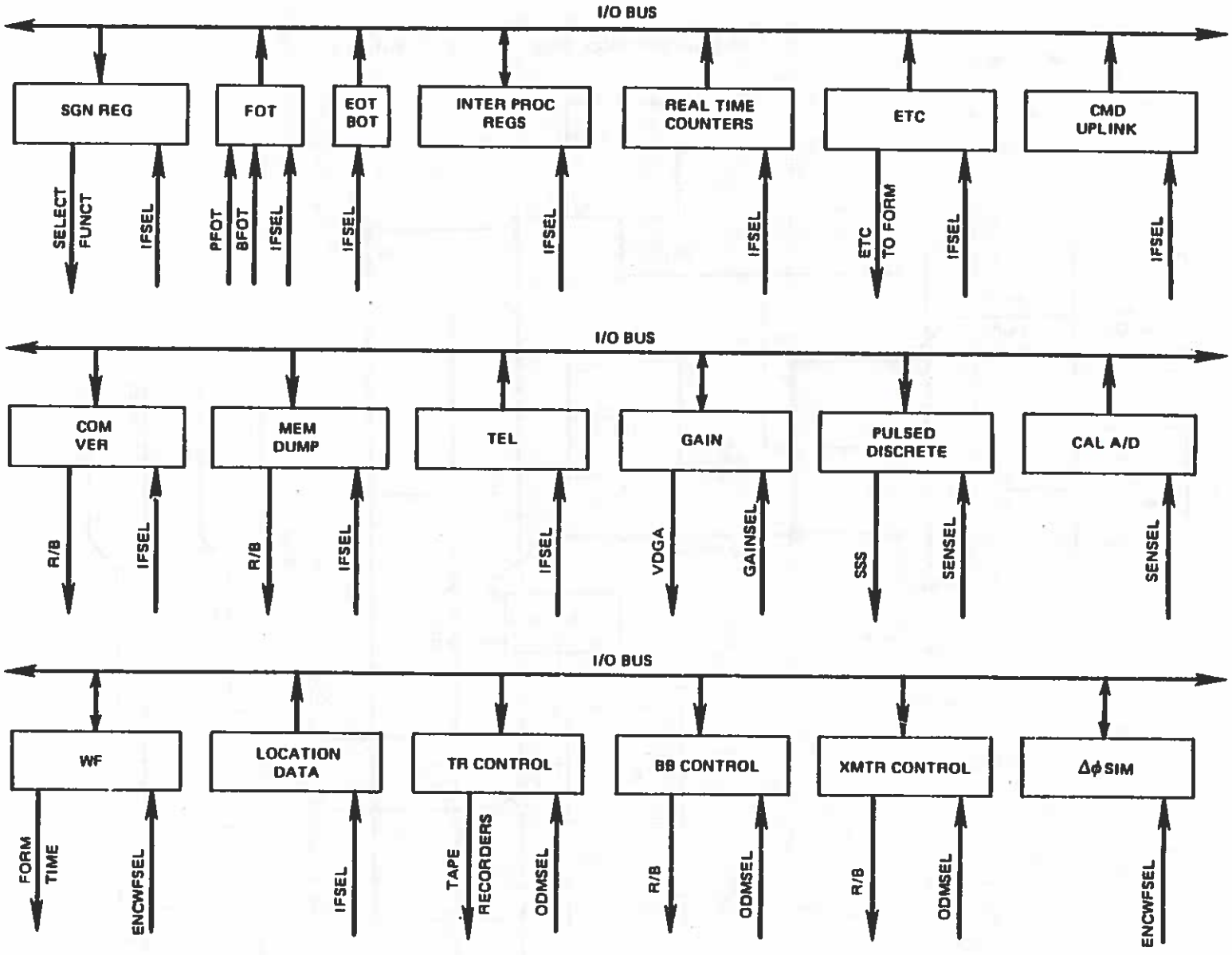

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Figure 2.1.3-3. I/O Function Control

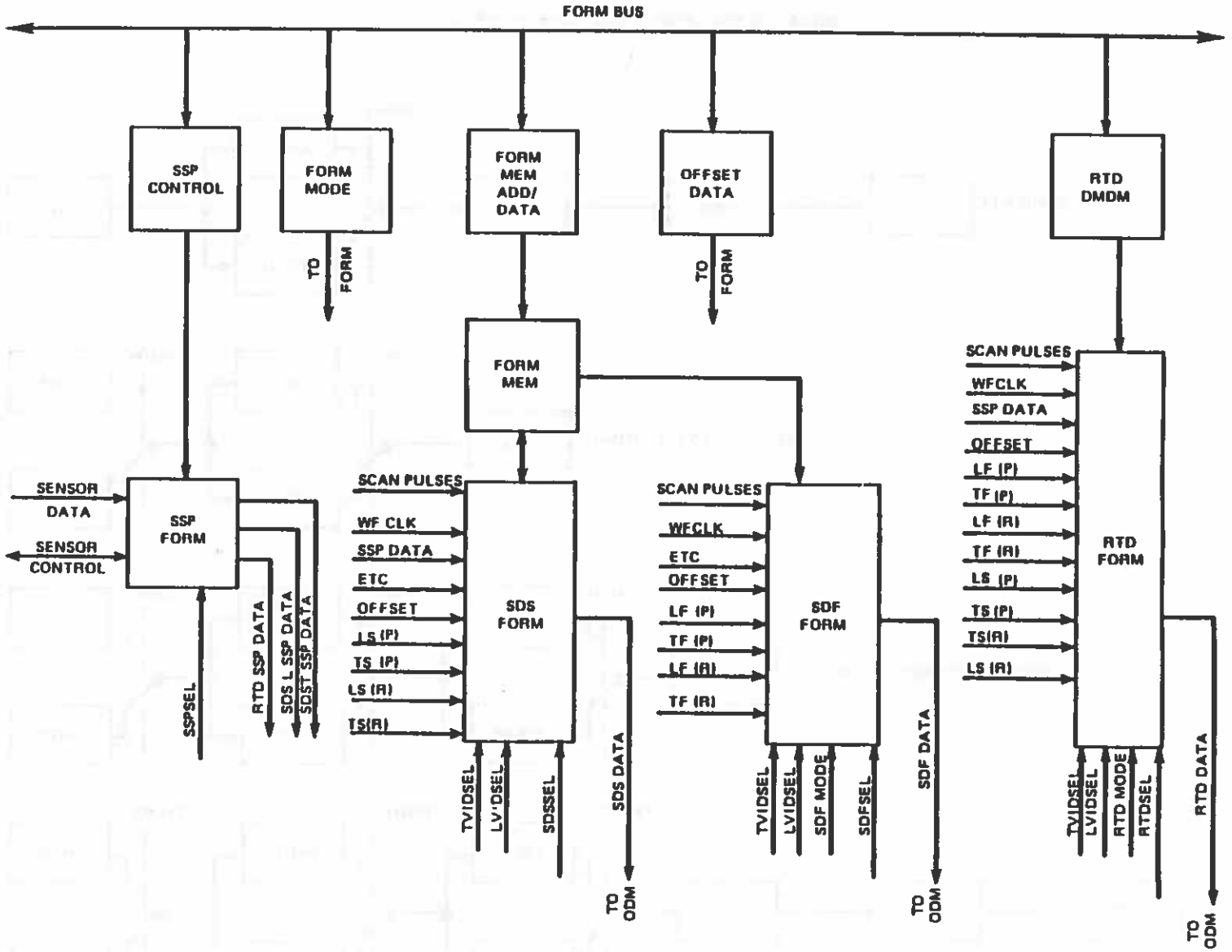

Figure 2.1.3-4. Formatter Inputs and Control

79-0681-V-19

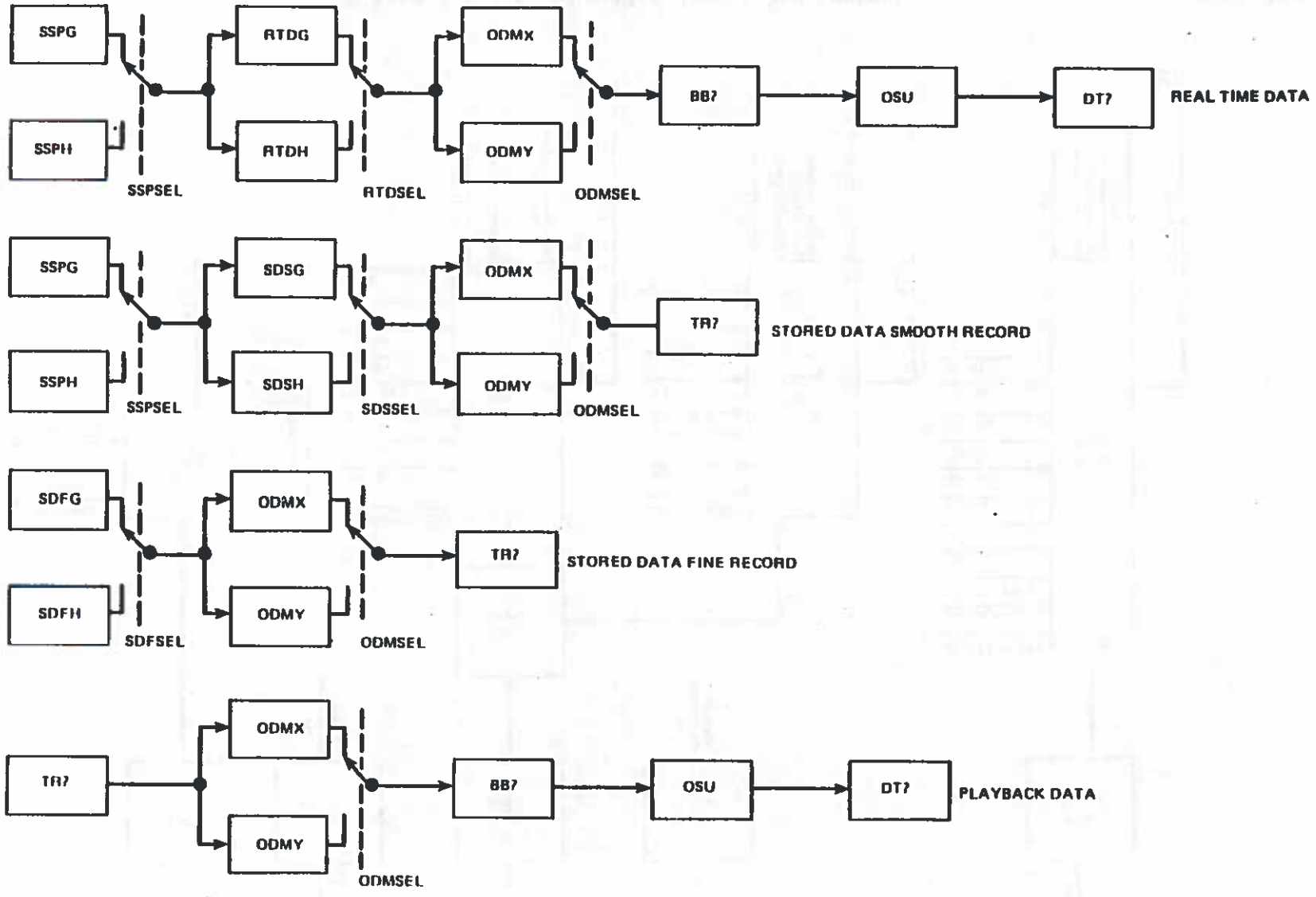

Figure 2.1.3-5. OLS Data Paths

79-0661-V-37

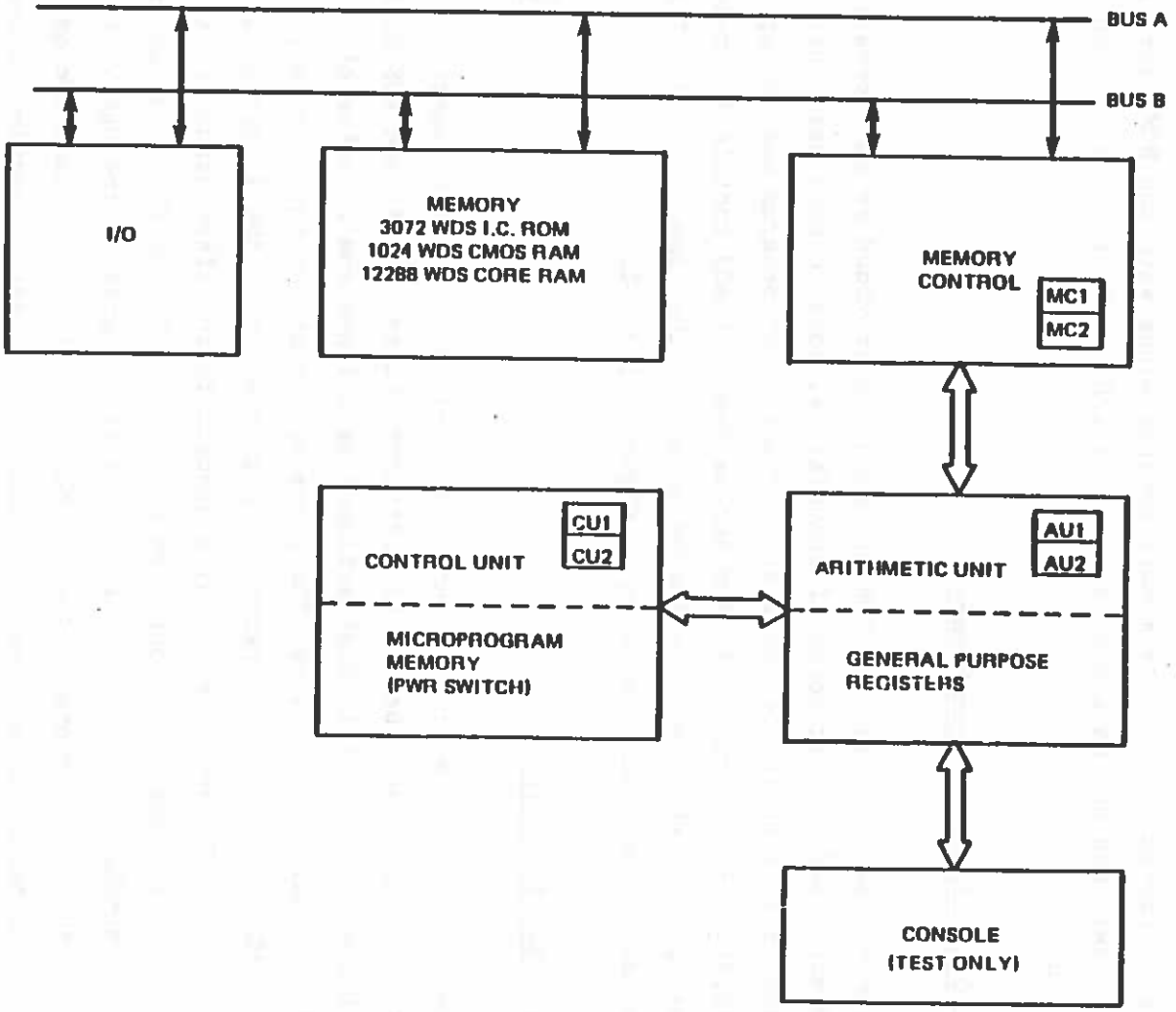

Figure 2.1.3.1-1. Processor Block Diagram

2.1.3.1.1 Processor

The OLS processor is a 16-bit, functional, two's complement, stored program processing unit built with low power MSI technology. This processor consists of eight registers, including four accumulators, a microprogrammed control matrix and decoding and execution control logic. Detailed descriptions of processor operation and instruction set are found in paragraph 3.1.

In the Microprogram ROM, the memory devices along with the ROM address drivers are switched on, as a function of the I/O clock, for only 24% of the clock period.

2.1.3.1.2 Operational Program Memory

Program and data storage for the processor is provided by the Operational Program Memory. 3072 16-bit words of nonvolatile, nonalterable Read Only Memory (ROM) are allocated for an initial "bootstrap" program and lookup tables. 13,312 16-bit words of Random Access Memory (RAM) contain the main operational program which will be loaded by way of the command uplink. The configuration of the memory is shown in Figure 2.1.3.1-2.

2.1.3.1.2.1 Bus Switching

The Memory Control Section (Figure 2.1.3.1-3) provides the interface between the processor and the two bidirectional buses, BUS A, and BUS B. Each of these buses consists of 16 bidirectional data lines and a number of single-directional control lines. The processor input and output buses, level shifted to CMOS levels, are connected to either BUS A or BUS B, depending on the state of PROCSEL, which is set by a Spacecraft interface signal to the OLS. Similarly, the memory is connected to either BUS A or BUS B, depending on the state of MEMSEL (another spacecraft interface signal to the OLS). It should be noted that only one of the two Memory Control sections, the one for Processor C and Memory E is shown. The other Memory Control section connects Processor D and Memory F to the buses. Therefore, Processor C can operate with Memory F on BUS B, etc., depending on the states of PROCSEL and MEMSEL.

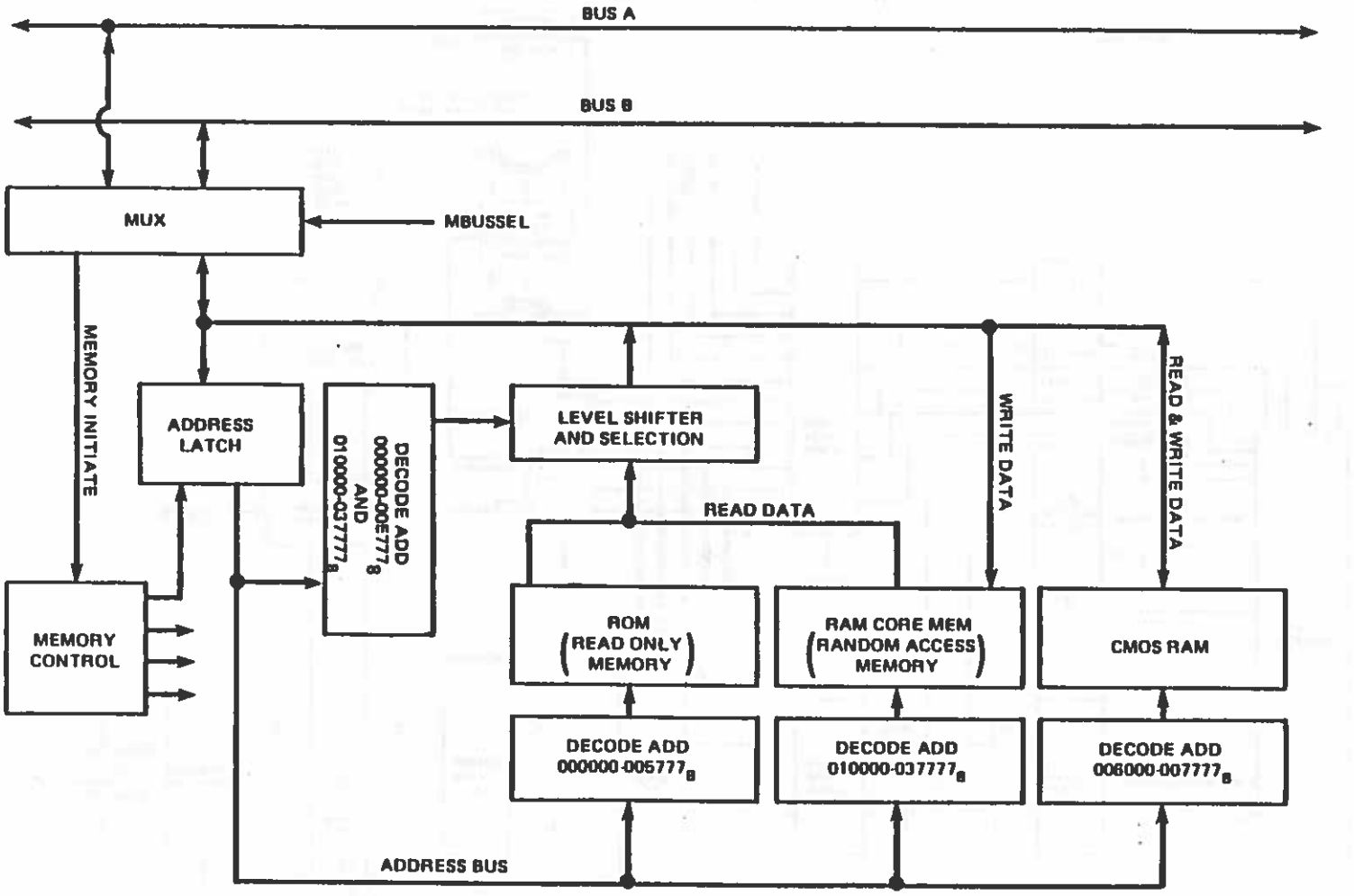

Figure 2.1.3.1-2. Memory Block Diagram

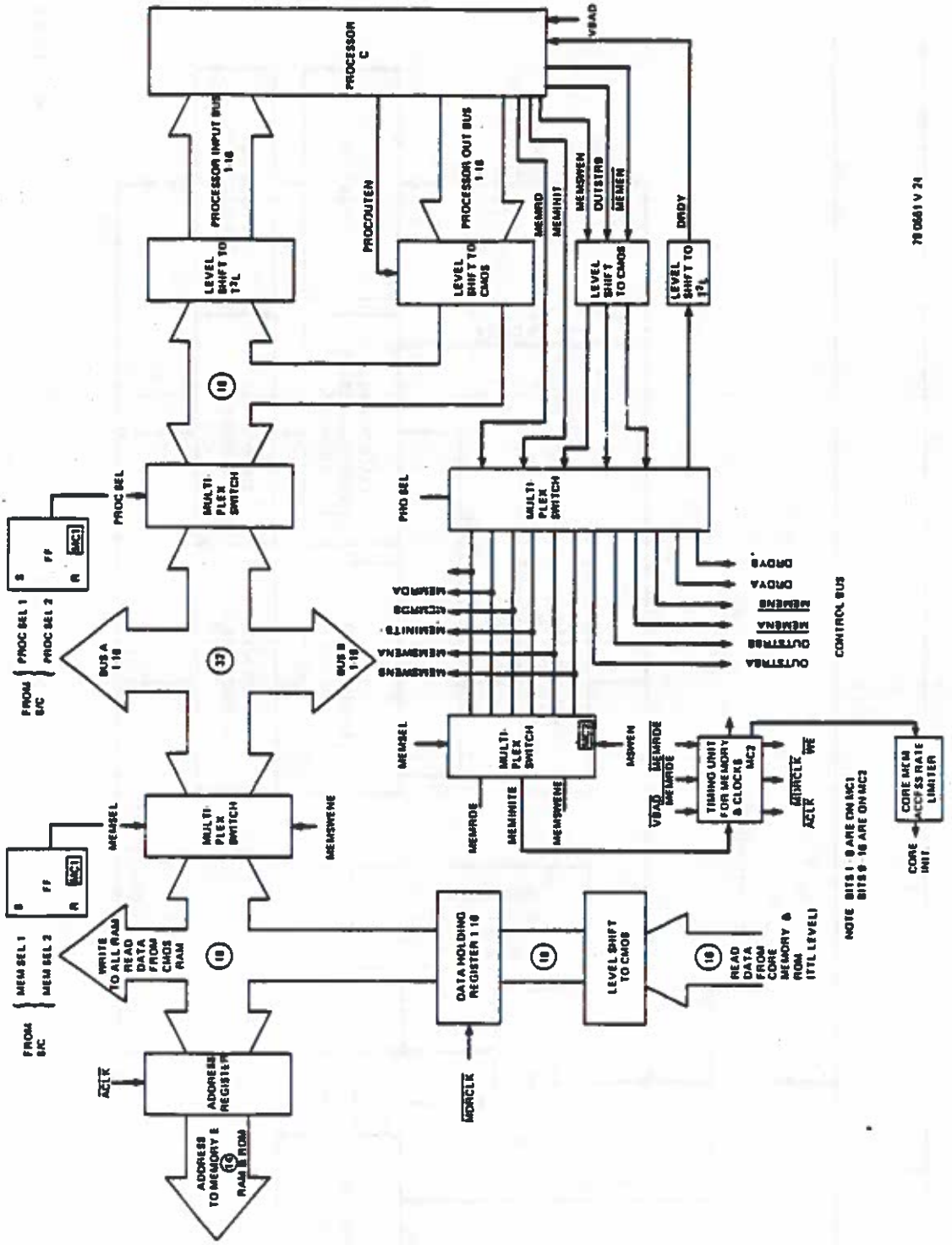

Figure 2.1.3.1-3. Memory Control Section

2.1.3.1.2.2 Memory Timing

The timing unit and holding registers can be considered as a part of the memory. They are connected to a bus (A or B), rather than to a particular processor. MEMINIT starts the memory cycle, with MEMRD indicating whether it is a read or write cycle. ACLK- strobes the address from the bus into the Address Register. In the case of a write cycle, the data then appears on the bus and is written into the proper RAM location by WE-. In the case of a read cycle, MDRCLK-strobes the data from the memory (either RAM or ROM) into the Data Holding Register, where it is seen on the bus. MEMSWEN removes the Memory from the bus when an I/O instruction is being executed. CLEAR and VBAD are initial clearing pulses generated by power turn-on.

NOTE: Signal ACLK- is the complement of signal ACLK.

2.1.3.1.2.3 ROM Memory

The configuration of the 3072 word by 16-bit ROM board is shown in Figure 2.1.3.1-4. The ROM chip is 4 bits by 512 words and the chips are grouped by fours into blocks of 16 bits by 512 words. Only the block which is being addressed is powered.

2.1.3.1.2.4 CMOS RAM Memory

There are 1024 16-bit words of CMOS RAM memory located on one board. Each board contains 16 4096-by-1 bit chips (CMM5104) organized as a 16-bit by 1024 word block of memory. This portion of memory is used for parts of the operational program with extremely high access rates. A large power saving is realized by this method, since the 12K of core memory then has a much lower access rate.

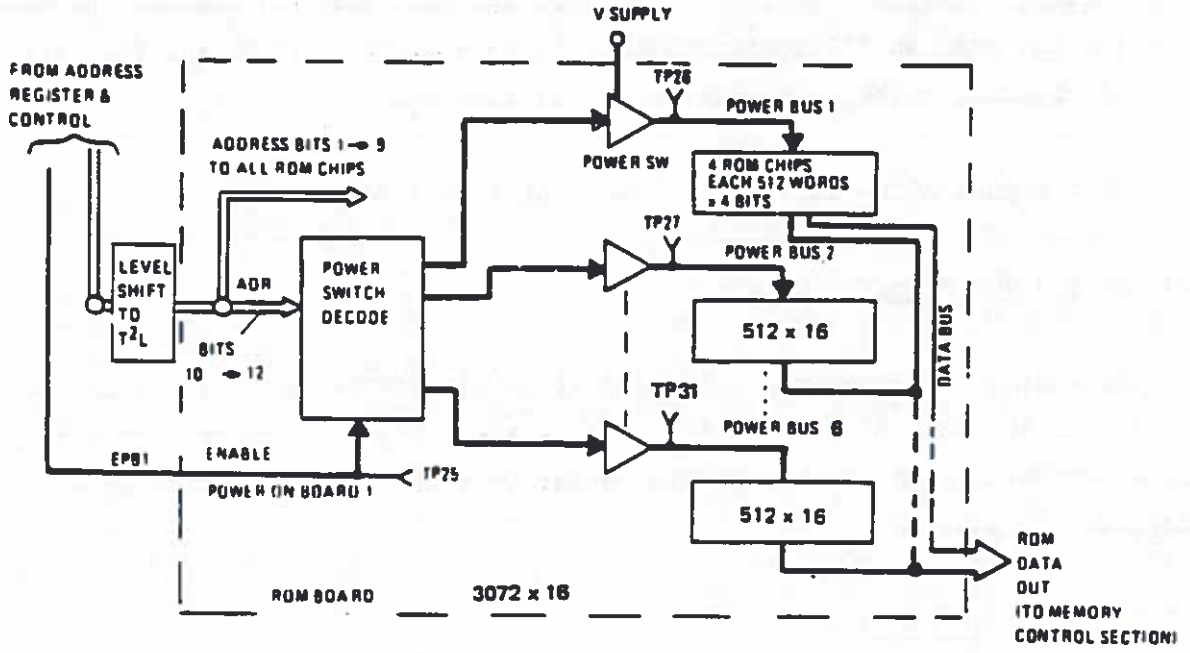

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Figure 2.1.3.1-4. 3072 Word X 16-Bit ROM

2.1.3.1.2.5 Core Memory

The Core Memory unit contains two electrically separate memories. One is a 16-bit, 12K word memory used for the Operational program RAM. The other is an 18-bit, 4K word memory used for the formatter memory (see para. 2.1.3.3.1). The Operational Program memory is shown in figure 2.1.3.1-5. Extensive power switching is done in the memory unit, with the result that the power consumption of the core memory depends directly on the access rate. To prevent overheating, an external protection circuit limits the number of accesses (reads or writes) to the core memory. If more than 25,000 accesses are done in a 250 millisecond period, all accesses are cut off for the next second. As a result, the processor will stop executing the operational program and revert to the idle mode. The operational software is written so as to prevent such a high access rate, but this circuitry acts as a backup.

2.1.3.2 Input/Output

The I/O performs a number of communication and control functions which are shown in figure 2.1.3-3. There are redundant functional blocks in the X and Y I/Os for each function.

2.1.3.2.1 Input/Output Control

2.1.3.2.1.1 I/O Bus Structure

Each I/O is connected to both BUS A and BUS B as shown in figure 2.1.3.2-1. It can accept processor Input/Output instructions from either bus, with BUS A arbitrarily having priority when instructions arrive simultaneously over the control lines of the two buses. As soon as I/O X, for example, receives processor output instruction over BUS A, it throws SELAX to the state where I/OBUSX is connected to BUS A. The data from BUS A is then loaded into the appropriate output holding register. The next processor instruction to arrive might be an input instruction over BUS B. I/O X would then throw SELAX to the state where I/OBUSX is connected to BUS B. The data from the appropriate input holding register is then gated onto I/OBUSX and thus onto BUS B for input to

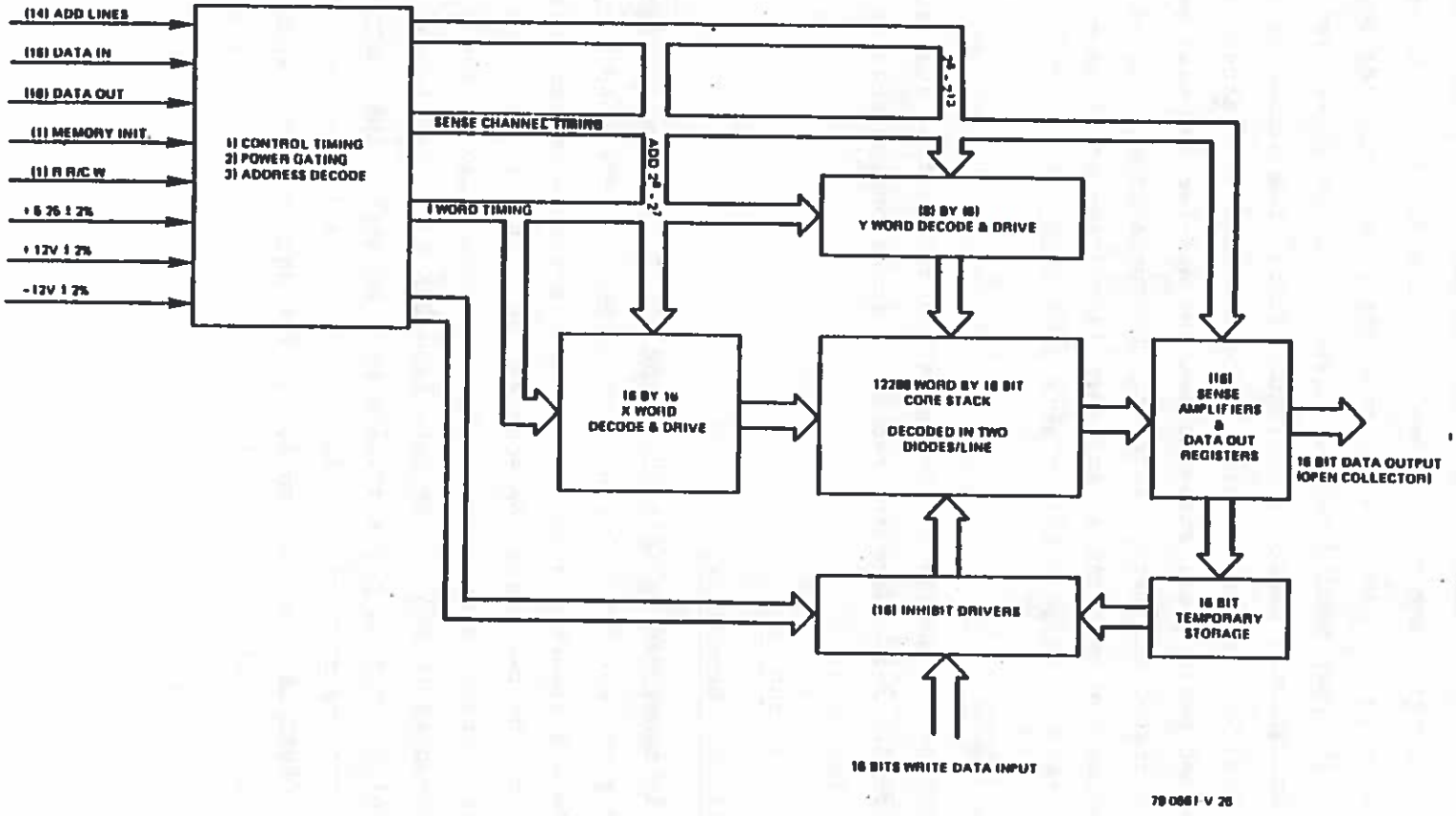

Figure 2.1.3.1-5. Operational Program Core Memory

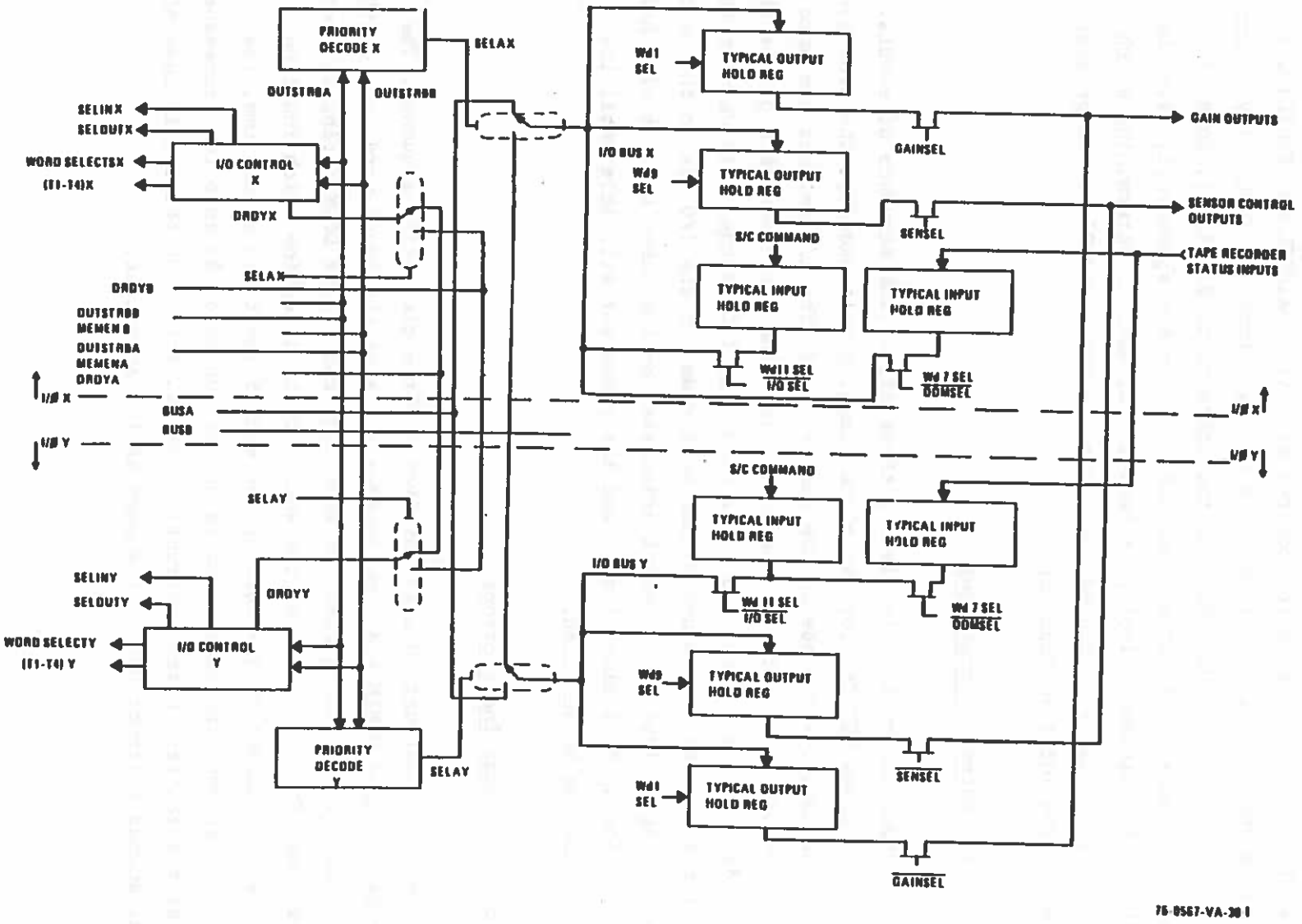

Figure 2.1.3.2-1. I/O Bus Structure

the processor. When both I/O's are powered up, they will execute instructions exactly in parallel. A given output register in I/O X and its duplicate in I/O Y will be loaded simultaneously with the same data from the same bus (A or B). The state of the configuration control bits (ex. GAINSEL or SENSEL) will determine whether the bits from I/O X or those from I/O Y actually control the output lines to other OLS Units or the spacecraft. Similarly, both I/O's will receive the same inputs from other OLS units or the spacecraft, with the state of the configuration control bits (ex. IFSEL, ODMSEL) determining which register is actually connected back onto the bus (A or B) to the processor which did the input instruction.

2.1.3.2.1.2 Output Instructions

An output instruction involves a three clock-time sequence of events. The processor raises OUTSTRB for two clock times. Simultaneously, the processor places the output word code on the bus (A or B). The I/O catches the word code and raises DRDY during the second clock time. The processor then places the output data on the bus for one clock time. The I/O catches this data in the proper register as determined by the word code. If the I/O was in the process of executing an instruction which originated on the other bus, it will hold DRDY low for up to 5 clock times, and the processor will idle until its instruction can be serviced.

2.1.3.2.1.3 Input Instructions

The input instruction also involves a three clock-time sequence. The processor raises MEMEN and simultaneously places the input word code on the bus (A or B). The I/O catches the word code and raises DRDY during the second clock time. The I/O then uses the word code to determine which input holding register to connect to the bus. At the end of the third clock time, the processor strobes the data which is on the bus (A or B) into the processor register specified in the instruction format. Action of the I/O in case of simultaneous instructions is the same as for an output.

2.1.3.2.1.4 Clear/Clock Drivers

The Clear/Clock drivers, as shown in figure 2.1.3.2-2 consist of redundant clock oscillators in the OSU, redundant line receivers in the Red/Black units, level shifters to CMOS levels, selection switches to select either OSU "X" or OSU "Y" as the clock source, and drivers to distribute the clocks throughout the system. The basic clock frequencies and their derivations are given in table 2.1.3.2-1.

The master oscillators and dividers are located in the OSU to prevent corruption of the clock signals which are used by the BBTs. Differential line drivers and receivers are used to carry the clocks to the SPS, where they are level shifted to CMOS (12-volt) levels where necessary. The configuration control bit CLKSEL is used to determine whether the clocks used throughout the system originate from OSU "X" or OSU "Y". Clear (reset) signals to various areas of the system are generated by the power turning on to that particular area. This sets components to known initialization states.

2.1.3.2.2 Spacecraft Interface

There are six digital serial information interfaces between the OLS and the spacecraft. These interfaces are shown in figure 2.1.3.2-3. Four interfaces carry information from the spacecraft to the OLS: Command Data, Elapsed Time Count, Location Data, and Telemetry Data. Two interfaces carry information from the OLS to the spacecraft: Real Time Command Verification and Memory Dump.

2.1.3.2.2.1 Red/Black Interface Unit

Signals to and from the rest of the spacecraft are routed through the Red/Black Interface Unit which is located within the SPS. This unit provides power supply and ground isolation in order to keep any traces of "red" data within the SPS from appearing on the lines to and from other spacecraft units. Level shifting from the 5-volt signal levels used on spacecraft interface lines to the 12-volt levels used within the SPS is also

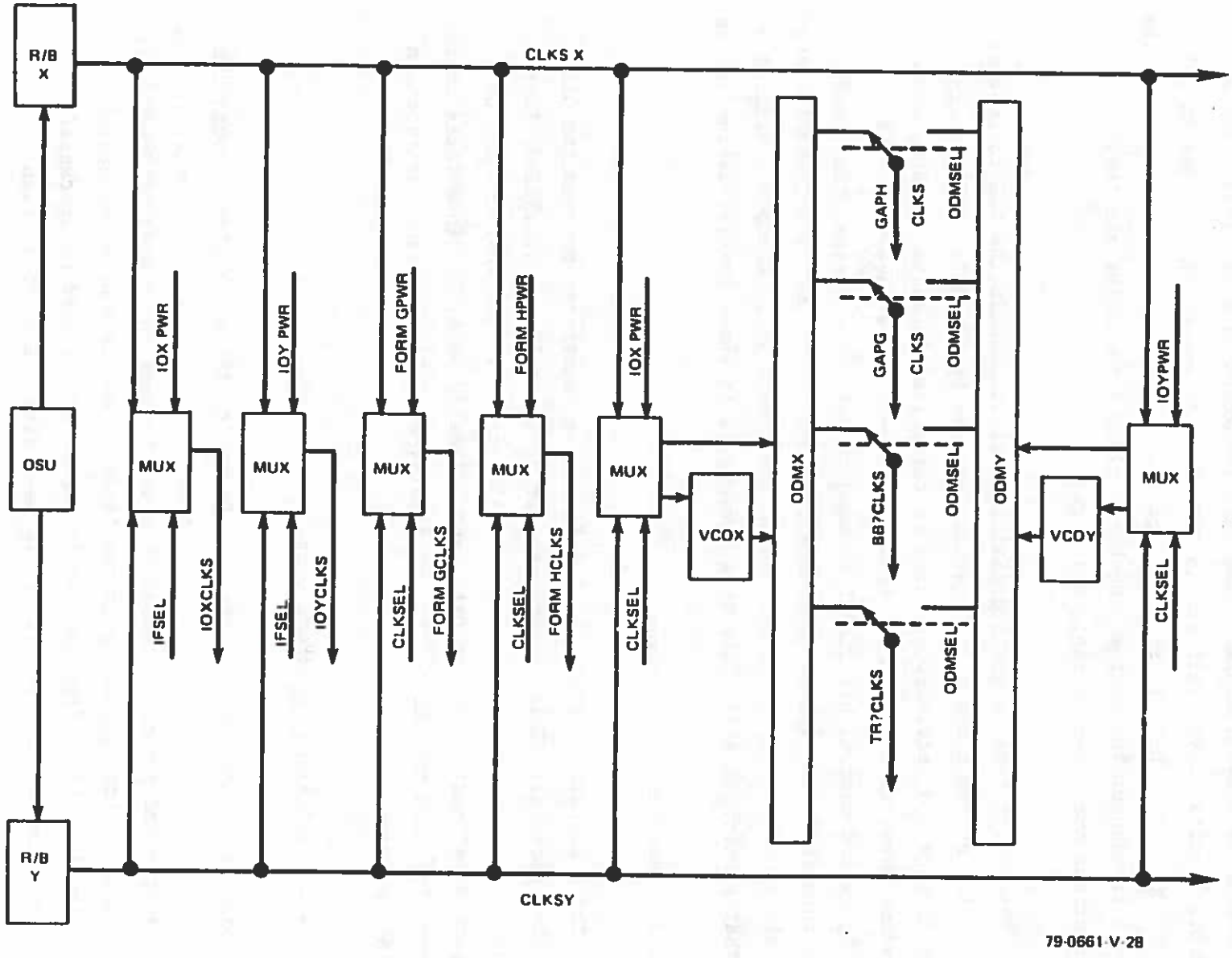

Figure 2.1.3.2-2. Clock Selection

Table 2.1.3.2-1. OLS/AVE Basic Clock Frequencies

Clock Freq. (Hz)	Source	Divided By	Use	
512,000 (Nom.)	WF (SPS)	1	W/F VCO in SPS	RTD, SDFR, SDSR
102,400 (Nom.)	WF (SPS)	5	SDF Sampling	SDFR
20.480 (Nom.)	WF (SPS)	25	SDS Sampling	SDSR
6023.529411 (Nom.)	WF (SPS)	85	RTD Frame Count	RTD
5,324,800	ST (OSU)	1	Basic OSC (ST) in OSU	
2,662,400	ST (OSU)	2	Tapes, BB	2.66 P
1,331,200	ST (OSU)	4	Tapes, BB	1.33 P. SDFLTR
665,600	ST (OSU)	8	Tapes, Formatter	SDFL or T R
66,560	ST (OSU)	80	Tapes, Formatter	SDF R
1,064,960	ST (OSU)	5	A/D Converter	SDF
4,096,000	RT (OSU)	1	Basic OSC (RT) in OSU	
1,024,000	RT (OSU)	4	RTD Formatter BB, A/D Converter	RTD
819,200	RT (OSU)	5	Processor - I/O	-ALL-

All 3 main oscillators are redundant

R = Record

P = Playback

ST = Stored Data Oscillator
RT = Real time Data Oscillator
WF = Wow/Flutter VCO

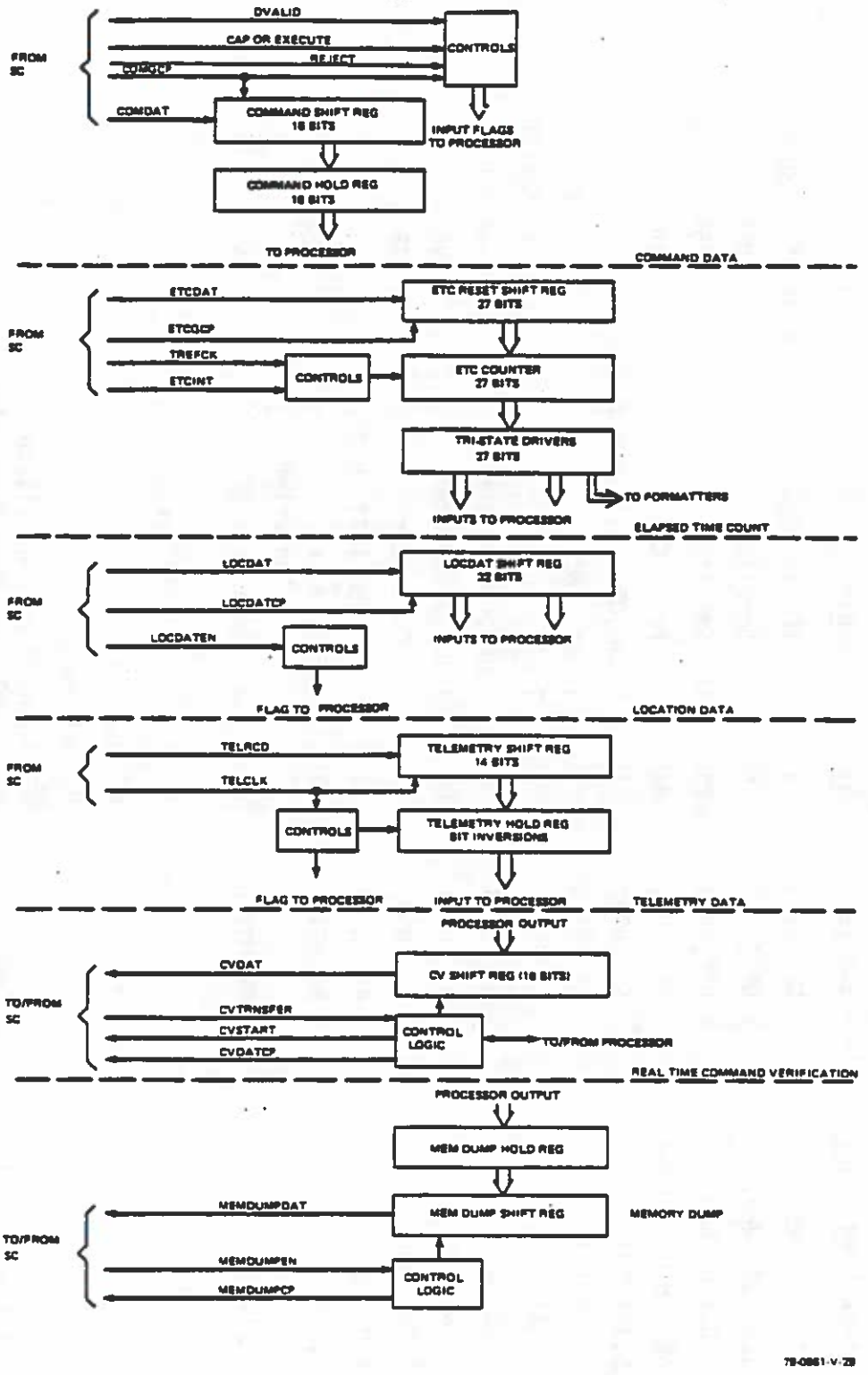

Figure 2.1.3.2-3. Spacecraft Interfaces

accomplished within the Red/Black. There are separate, independent Red/Black units for each I/O, so far as redundancy switching is concerned, they fall within the Spacecraft Interface section. (Selected by IFSEL from the Spacecraft.)

2.1.3.2.2.2 Uplink Command Data

The OLS 16-bit commands from the ground are received by the OLS/AVE as signal data (COMDAT) along with a 2000 bps gated clock (COMGCP). When the DVALID signal is true, the data is serially shifted into a 16-bit shift register and a 4-bit counter detects the count of 16. The count of 16 provides an enable signal which allows the data to be transferred into a holding register and sets a ready flag for the program (UPREDY). Upon execution of a Select Input Word II to transfer the data to the processor and memory, the flag bit is reset.

This 16-bit transfer continues until either the gated clock is inhibited, or the data valid line (DVALID) changes state indicating sync has been lost.

On spacecraft where command encryption is implemented, two pulsed lines (EXECUTE and REJECT) are provided to the OLS. The execute or reject pulse will occur between 25 and 35 milliseconds after the OLS receives the last COMDAT bit. The processor will accept those commands followed by an EXECUTE pulse, and ignore those followed by a REJECT pulse.

On spacecraft without command encryption a Command Access Period (CAP) line is provided to the OLS. If this line is at the "OFF" level, the processor will ignore real time commands. If the line is at the "ON" level, the processor will accept real time commands. Different operational programs are used in the OLS depending upon whether command encryption is implemented.

2.1.3.2.2.3 Elapsed Time Count Data

The Elapsed Time Count (ETC) counter is a 27-bit counter which is parallel loaded with a preset value and then counts the reference clock (TREFCK) at a rate of 1024 Hz. The output of the ETC counter is loaded into a 27-bit hold register by the NADIR pulse. This gives the formatters an elapsed time with respect to a given reference on the scanner. The processor reads the ETC count directly to a resolution of 2^{-10} seconds.

The ETC counter update is accomplished by receiving the ETC preset data (ETCDAT) along with a 1024 Hz gated clock (ETCGCP). After transfer of 27-bits of data the new ETC value is parallel-loaded into the counter upon receipt of the ETCINT signal and counting continues.

2.1.3.2.2.4 Location Data

The cosine solar azimuth, S/C altitude and solar elevation components of the Location Data from the S/C are used in the determination of scene solar elevation for L-channel gain control. The longitude, latitude, ephemeris time, and crossing angle data is inserted in the primary data streams to aid ground processing. Upon receipt of the Location Data Enable gate (LOCDATEN), the Location Data (LOCDAT) is clocked into a 32-bit shift register by the Location Data Clock (LOCDATCP). Upon receipt of the trailing edge of the Location Data Enable gate, a flag is set and the processor will input the data. There are five 32-bit data transfers in each 500 msec period spaced 100 msec apart where the last three (3) bits of each transfer defines the data type:

1st - Ephemeris Time and Longitude
2nd - Latitude and Cosine Crossing Angle
3rd - Cosine Solar Azimuth and Solar Elevation
4th - Spacecraft Altitude/Earth Radius Ratio and Ephemeris Time
5th - Cosine Lunar Azimuth, Lunar Elevation and Lunar Phase

The Location Data interface is also used to receive Load Shedding commands from the spacecraft. When used for this purpose the 32-bit transfer will occur at least 100 msec from the previous location data transfer and not be followed by another transfer for at least 100 msec. The upper 16 bits of the transfer will be the OLS command to be executed and the 3 data type bits will have the value 7.

2.1.3.2.2.5 Telemetry Data

The OLS/AVE receives the Equipment Status Telemetry (EST) Data for incorporation in the SDS Format to provide stored EST information throughout the orbit.

The EST Data (TELRCD) is received from the spacecraft as digital serial data along with a 2000 Hz Telemetry Data Clock (TELCLK). The data is serially shifted into a 14-bit register. The TELCLK pulses are counted (a 4-bit counter is preset to a count of 2 and detects the 14th clock pulse count at overflow). The 14th pulse loads the hold register and sets a program ready flag (TELRDY). After the program has input the Telemetry data, the flag is reset. The program formats the data and stores it in formatter memory for the Stored Data Smooth Formatter. This data output by SDS includes a number indicating the number of telemetry words in the SDS line.

2.1.3.2.2.6 Real Time Command Verification

The 5D-3 OLS uses a command verification sequence to provide protection against errors in real time commanding. Upon request of a real time command the parity is checked and if it is correct, the least significant 15 bits are left alone. If the parity is incorrect, the least significant 15 bits are complemented. The MSB is set to indicate which processor received and echoed the command, with "0" indicating Processor C and "1" indicating Processor D. The command (modified as discussed above) is output by the processor to a holding register for downlink transmission through the CIU. The OLS requests CIU access through the CV START line, the Spacecraft CIU responds over the CV TRNSFER line, enabling the OLS to serially output a single 16-bit word (CVDAT) and a burst of 16 clocks (CVDATCP) at a 102.4 MHz bit rate once every PIP frame. The MSB is transmitted first.

2.1.3.2.2.7 Memory Dump

The Spacecraft PIP indicates to the OLS that it can accept blocks of 1, 2, 10, or 11 16-bit words, dependent upon PIP mode. Effective OLS downlink rates in words/sec are as follows:

Mode	Words/Sec	Words/Frame
2 Kb non-OLS Dump	4	1
2 Kb OLS Dump	40	10
10 Kb Non-OLS Dump	40	2
10 Kb OLS-Dump	220	11

The PIP provides a gate signal (MEMDUMPEN) and the OLS responds by outputting up to 11 16-bit serial words (MEMDUMPDAT) at a 9.99 kb/s bit rate. A 9.99 kHz gated clock (MEMDUMPCP) is provided by the OLS to transfer the data. Memory dump data is double buffered in the OLS.

2.1.3.2.3 Gain Control

The Gain Control function (Figure 2.1.3.2-4), controls the L channel gain configuration so as to select the proper value from the 150 dB range that is available. There are 3 modes of L channel gain control.

Along Scan Gain Control (ASGC)
Along Track Gain Control (ATGC)
Preset Gain Control (PGC)

The gain control function may be in only one of these modes at any given time. The mode is commanded from the ground and is set up by the processor during the positive end of scan (EOS).

The ASGC mode provides a variable gain and sensor select during active scan. The ASGC mode is required for near terminator areas when scene illumination varies greatly along the scan line but is operationally applicable at any time regardless of spacecraft position. It is therefore considered the primary gain control mode throughout the orbit. During the entire length of active scan, the processor in ASGC mode controls the sensor select and modifies the rate of change of the VDGA so that the gain closely follows the desired gain. The desired gain is obtained from the gain versus scene source (sun or moon) elevation curve (GVVSSE), stored in constants memory, as modified by BRDF and lunar phase correction factors. The BRDF correction factor compensates for the anisotropic (nonuniform) reflectance characteristics of the scene which cause saturation of both visible day and visible night OLS imagery. The lunar phase correction factor automatically adjusts the nighttime gain for the variable illumination as a function of the moon's phase. The correction factors are calculated using the following inputs: source (sun and moon) elevation angle, source azimuth, OLS scan angle and spacecraft altitude. The location data (S/C ephemeris) is obtained from the spacecraft.

The ATGC mode provides a constant gain and sensor select for the entire active scan. This mode is operationally applicable as a backup to the ASGC mode in areas where scene illumination is constant along scan (e.g., noon orbit) but may be commanded at any time. Some failure modes would allow ATGC mode operation but not ASGC mode operation. In the ATGC mode the processor (during positive EOS) chooses, as a function of scene source elevation at

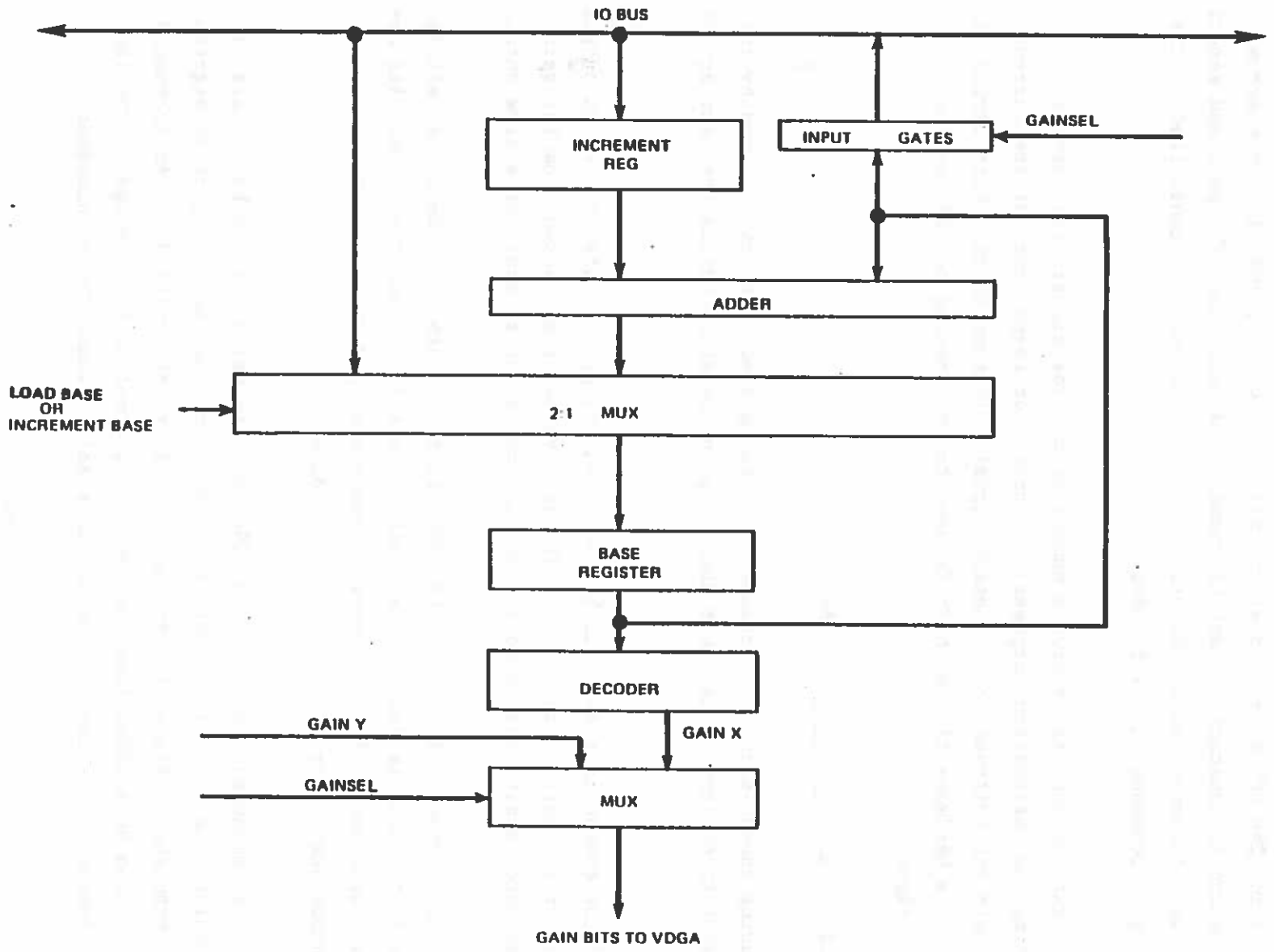

Figure 2.1.3.2-4. Gain Control

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nadir, the sensor and gain for the next active scan based on the GVVSSE curve values.

The PGC mode provides a constant gain and sensor select for the entire active scan. The PGC mode is operationally applicable primarily where scene illumination is constant but may be commanded at any time. The gain and sensor select is not controlled by the processor but is completely controlled by the uplink gain commands in the PGC mode.

The various sensors require a number of control signals for segment switching and calibration purposes. The processor keeps track of the current scan angle and switches these control signals. In some cases, where timing is critical, a hardware timing chain is used to synchronize certain sensor control signals.

2.1.3.2.3.1 End-of-Scan Functions

During end-of-scan the L channel gain command word is interrogated by the processor to determine what mode should be in operation during the next active scan.

If the commanded mode is to be PGC, then the proper bits are set in output word 2 for the correct sensor use. The gain value is extracted from the gain command word, scaled and saved for output just prior to start of active data.

If the commanded mode is to be ATGC, Location Data from the spacecraft is utilized to calculate gain and determine sensor selection. The proper bits are set in output word 2 for the correct sensor use, and the gain value is saved for output just prior to start of active data.

If the commanded mode is to be ASGC the gain value for the base register is calculated using Location Data from the spacecraft and using 56.24 degrees as the scan angle, since it corresponds to start of active data. An increment value is also determined from the two's complement of the average of the last two increment values used in the previous active scan. These increment

register and base register values are output to their respective registers (Output Words 0 and 1) when the scanner is near 56.24 degrees and its direction is towards the next active scan. Output word 2, which determines sensor selection, is output at the same time.

2.1.3.2.3.2 Active Scan

The processor has no gain functions to perform during active scan for Preset Gain Control (PGC) and Along Track Gain Control (ATGC) modes. The base register for these modes is a fixed value determined during end-of-scan. Since an increment value is never output in these modes, updates to the base register are inhibited during the entire scan.

It is the function of the Along Scan Gain Control (ASGC) program to see that the base register has the proper gain value as the scanner passes through a wide range of illumination. The base register value is controlled by outputting values to an increment register. This increment register is added to the base register (by I/O hardware not controlled by the processor) at a rate of 40960 Hz.

The ASGC mode involves calculations using sines, cosines, arcsines, and the Gain Value Versus Scene Source Elevation (GVVSSE) curve. The GVVSSE curve is entered in the processor as a table with a value for each degree of solar elevation angle from -15 to +80 degrees and for each degree of lunar elevation from -5 to +80 degrees.

The base register range of values is 0 dB to 64 dB. Because of the wide range of gain values of the GVVSSE curve any one of the four sensors (HRD, PMT 1/9, PMT LOW, PMT HIGH) may be selected by the processor. The sensor selection is determined by a sensor switching routine which is called at least each 1.6 milliseconds. The sensor switching routine compares the current value of the base register (Input Word 1) against a predetermined sensor switch point. When the switch point has been passed, the next sensor is selected and the base register gain altered to reflect the new sensor selection.

2.1.3.2.3.3 Redundancy

The Gain Control section is fully redundant. Use of the "X" or "Y" sections is determined by the state of the GAINSEL bit in the configuration control word.

2.1.3.2.4 Sensor Control

The control signals for the sensors are characterized as either software implemented or hardware implemented. As shown in figure 2.1.3.2-5, both types of signals are under control of the program, but where critical timing is required for pulsing certain lines, these are timed by a hardware counter (pulse timer).

Some of the signals in output word 2 take effect immediately (T gain, T level, PMT unblank, log/lin amp, etc). The sensor select signals (PMTSEL, PMTY4, PMTPGS) are held when output and do not take effect until the VDGA is changed with an output word 1 to the base register. The signals output in word 9 are discrete enables switched at a given Delphi count. These are PMTLFT in bit 1, PMTMID, PMTRGT, etc.

The hardware implemented signals, or pulsed signals, are output in word 10. Upon receipt of the PULSEN signal output in word 9 or the $\pm$1018 encoder control track signal entering overscan, a counter is started, counting the I/O clock to generate the 2.5, 2.0, and 0.5 msec pulses required for generating the pulses required during overscan for Dark Referencing, etc. These are PMTDR1, PMTDDH, etc.

Also in the Sensor Control section is a 10-bit A/D converter which samples calibration signals from the PMT and the Thermal detector. This calibration is done during the overscan region so as not to interfere with normal video. The processor inputs the values and outputs them to the formatter memory for insertion into the SDF and SDS data streams.

The Sensor Control section is fully redundant, and its outputs are switched by the SENSEL bit. Signals which control two redundant sensor units (for example HRD electronics) are wired separately to each unit. Signals which

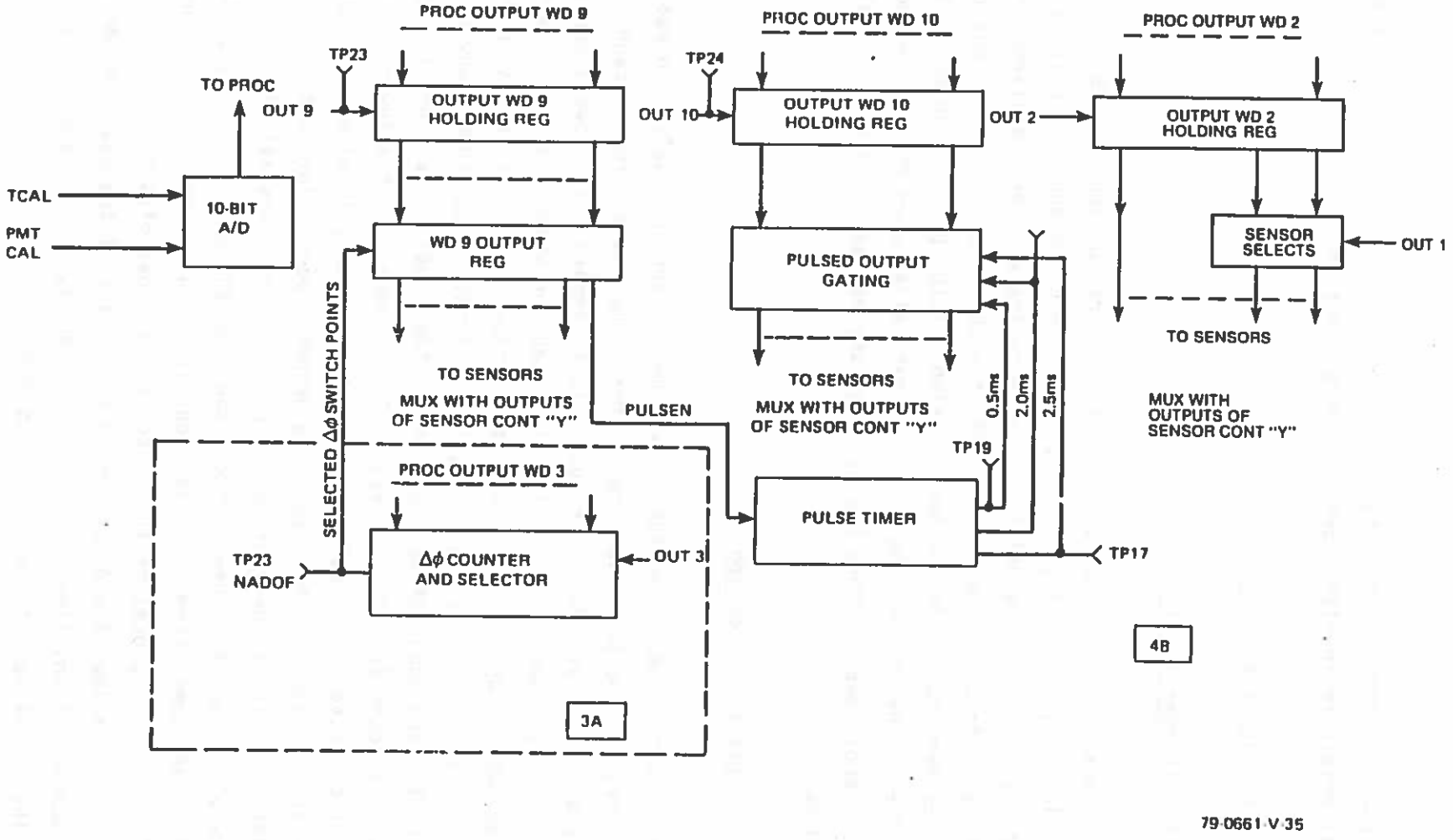

Figure 2.1.3.2-5. Sensor Control

control nonredundant sensor units (for example the PMT) use single wires, but may still originate in either Sensor Control section.

2.1.3.2.5 Encoder Processing

2.1.3.2.5.1 Encoder Inputs

The encoder processing circuitry acts on three pulsed signals from the encoder electronics (see figure 2.1.3.2-6). These are Nadir (a pulse at the mid point of the scan), Delphi (a pulse approximately every milliradian of the scan, numbered from 0 at Nadir to ±1024 at each end of scan) and Control Track (six pulses per scan cycle located at Delphi -1018, Delphi +146 and Delphi +1018). The encoder processing circuitry determines when the scanner motion is up to full amplitude and then begins using the encoder outputs to sample and format data.

2.1.3.2.5.2 Offset Correction

The encoder processor measures the time between 1018 pulses in each overscan region. The processor inputs these times to determine scanner offset which is averaged over 1024 scan cycles to determine the software (data sampling) offset. Several control pulses used for video sampling, wow/flutter and image motion control all require correction when there is a scanner offset. These pulses-Line Sync (LS), End of Active Data (EOAD), Wow/Flutter Enable (WFEN) and Nadir Offset Correction (NADIRCOR) - are generated by outputting a count from the processor (Output Word 7) and allowing that number of center-detected Delphi pulses to pass by. The Delphi pulse which causes the counter to overflow will be steered to become a particular control pulse, depending on which of the four enable bits in word 7 was set. The counter overflow also requests a new counter load from the processor. The pulse which generates EOAD comes from a similar counter on Output Word 3. The counters are manipulated by the processor to correct for scanner offset. A separate counter (Input Word 3) allows the processor to keep track of the exact Delphi position of the scanner at any time. Offset correction may be inhibited by setting a bit in the uplink operational constants memory.

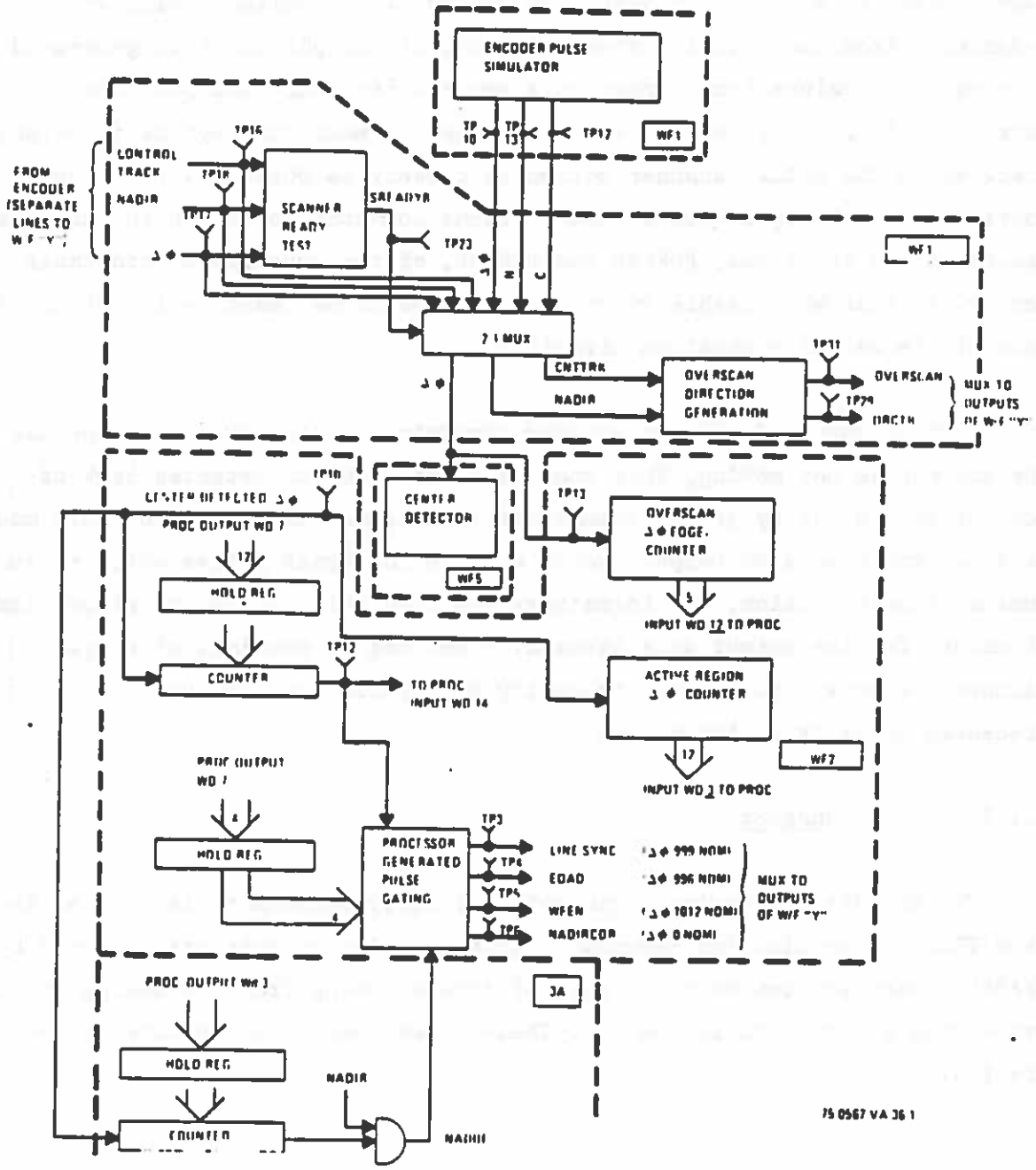

Figure 2.1.3.2-6. Encoder Processing

2.1.3.2.5.3 Encoder Simulator

Since the Delphi detection electronics on the actual scanner is not redundant, a precision encoder simulator has been incorporated in the digital hardware (see figure 2.1.3.2-7). This simulator can operate in a "locked" mode, where it receives the Nadir and Control Track pulses (which are redundant) from the actual scanner. A synthetic Delphi track is generated by reading delay values from a read only memory. Frequency and position correction is done by the processor in order to make this synthetic Delphi track match the actual scanner motion as closely as possible. Position correction may be optimized by using ground commands to uplink appropriate values in two locations, PDELBS and PDELSP, of the operational constants memory. In this way, usable video can continue to be taken in the event of loss of the Delphi generation circuitry.

A "free run" mode of the encoder simulator is also available for use when the scanner is not moving. This mode is entered due to detected lack of scanner motion, or by ground command if the scanner is in motion. This mode provides the simulated Delphi, Nadir and Control Track pulses which represent nominal scanner motion. The formatters are then able to provide proper line structure for the output data streams. Video has no meaning, of course, without a scanner, but stored telemetry and special sensor data can be processed normally on the ground.

2.1.3.2.5.4 Redundancy

The Encoder Processing logic which is fully redundant, is part of the "Wow/Flutter" section for redundancy purposes. Its outputs are switched by W/FSEL. There are two separate sets of inputs coming from the analog encoder processing electronics in the PSU. These lines come from separate drivers in the PSU.

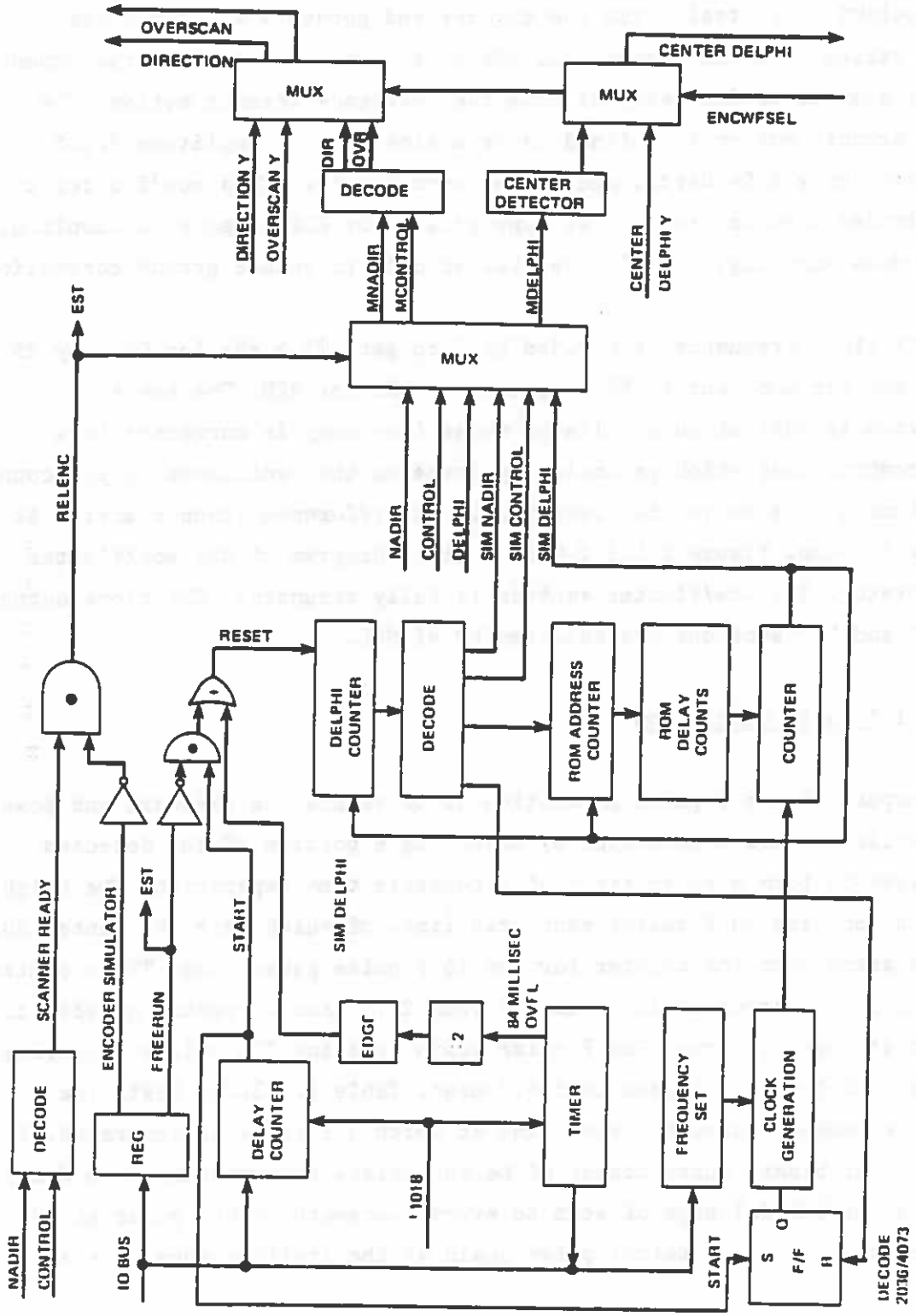

Figure 2.1.3.2-7. Encoder Simulator

2.1.3.2.6 Wow/Flutter Processing

The function of the wow/flutter clock generator is to process the center detected Delphi pulse train from the encoder and generate a clock whose frequency varies from the nominal 512 kHz as a direct function of the amount the actual scanner motion deviates from the reference scanner motion. The reference scanner motion is defined to be a sine wave of amplitude 57.85 degrees, frequency 5.94 Hertz, and offset zero degrees. This wow/flutter clock is then divided down to frequencies appropriate for SDF video data sampling, SDS video data sampling, and RTD wow/flutter data to enable ground correction.

The W/F clock frequency is divided by 5 to get 102.4 kHz for SDF, by 25 to get 20.48 kHz for SDS, and by 85 to get 6.024 kHz for RTD. The basic mechanization is that of an oscillator whose frequency is corrected in a feedback control loop which periodically compares the oscillator output count since beginning of scan to that required by the reference scanner motion at that point in scan. Figure 2.1.3.2-8 is a block diagram of the wow/flutter clock generator. The Wow/Flutter section is fully redundant. The clock outputs of the "X" and "Y" sections are selected by W/FSEL.

2.1.3.2.6.1 P Pulse Generation

The purpose of the P pulse generation is to reduce the hardware and power in the wow/flutter clock generator by selecting a portion of the detected Delphi pulses to form a pulse train of acceptable time separation. The Delphi pulse train contains 2049 pulses each scan line, of which only the center 2025 pulses are gated into the counter for use in P pulse generation. These center 2025 Delphi pulses occur at intervals of from 26.2 usec at center of scan to 164.7 usec at edges of scan. The P pulse train contains 256 pulses occurring at intervals of from 119.1 usec to 516.7 usec. Table 2.1.3.2-2 lists the Delphi pulse numbers through a scan line at which a P pulse is generated. P pulses occur at binary submultiples of Delphi pulses incrementing from every Delphi pulse at initial edge of scan to every sixteenth Delphi pulse at nadir, and decrementing to every Delphi pulse again at the trailing edge of scan.

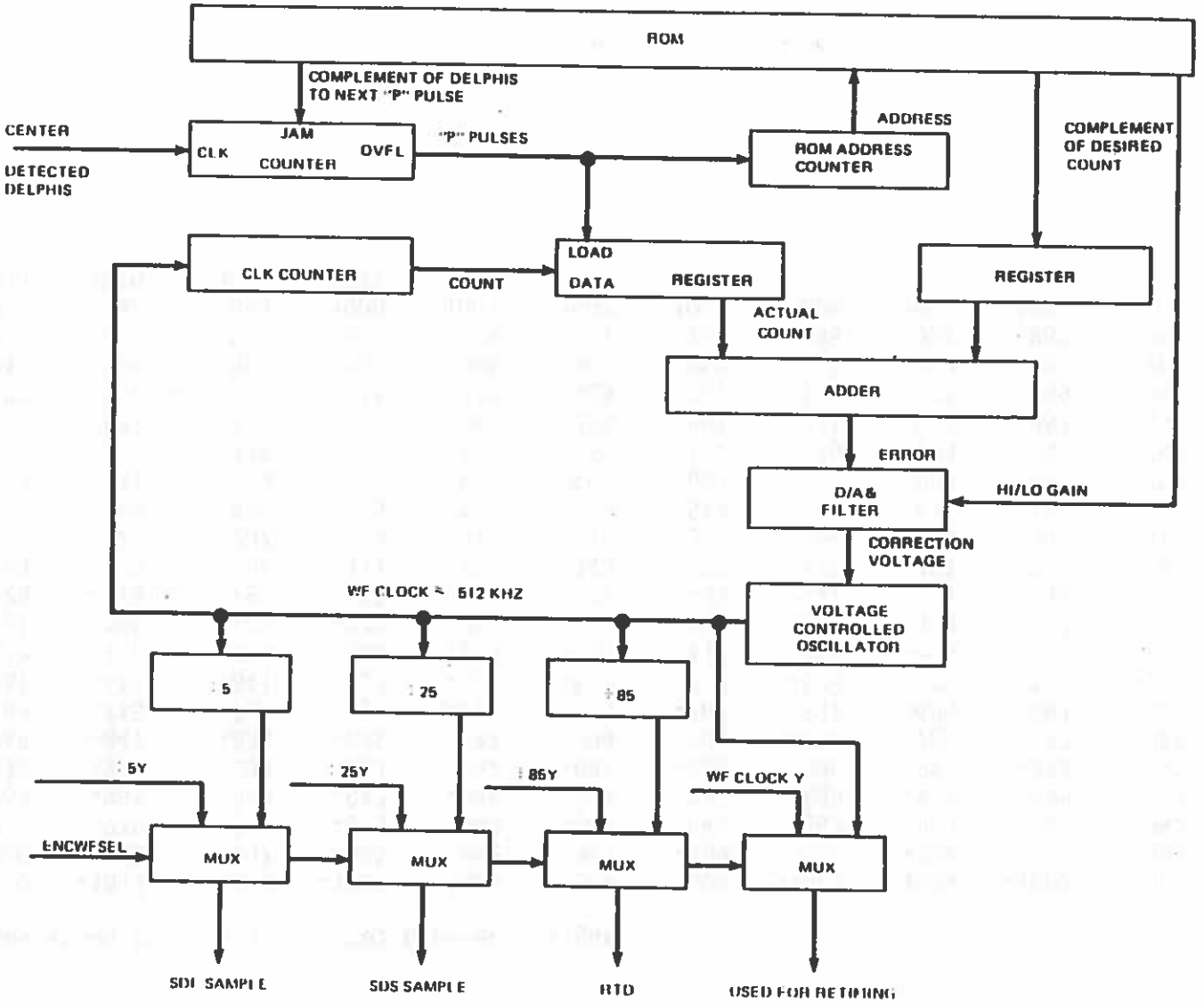

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Figure 2.1.3.2-8. Wow/Flutter Clock Generator

Table 2.1.3.2-2. Delphia Pulse Numbers at Which P Pulses Occur

Signs shown for DOS 1; for DOS Ø reverse signs

-1012	-1011	-1010	-1009	-1008	-1007	-1006	-1005	-1004	-1003	-1002	-1001
-1000	-999	-997	-995	-993	-991	-989	-987	-985	-993	-981	-979
-977	-975	-973	-971	-969	-967	-965	-963	-961	-959	-957	-955
-953	-951	-949	-947	-945	-941	-937	-933	-929	-925	-921	-917
-913	-909	-905	-901	-897	-893	-889	-885	-881	-873	-865	-857
-849	-841	-833	-825	-817	-809	-801	-793	-785	-777	-769	-761
-753	-745	-737	-729	-721	-713	-705	-697	-689	-681	-673	-665
-657	-649	-641	-633	-625	-617	-609	-593	-577	-561	-545	-529
-513	-497	-481	-465	-449	-433	-417	-401	-385	-369	-353	-337
-321	-305	-289	-273	-257	-241	-225	-209	-193	-177	-161	-145
-129	-113	-97	-81	-65	-49	-33	-17	-1	15	31	47
63	79	95	111	127	143	159	175	191	207	223	239
255	271	287	303	319	335	351	367	383	399	415	431
447	463	479	495	511	527	543	559	575	591	607	615
623	631	639	647	655	663	671	679	687	695	703	711
719	727	735	743	751	759	767	775	783	791	799	807
815	823	831	839	847	855	863	871	879	887	895	899
903	907	911	915	919	923	927	931	935	939	943	945
947	949	951	953	955	957	959	961	963	965	967	969
971	973	975	977	979	981	983	985	987	989	991	993
995	997	999	1000	1001	1002	1003	1004	1005	1006	1007	1008
1009	1010	1011	1012								

2.1.3.2.6.2 Oscillator and Control Loop

The oscillator and control loop mechanization, shown in figure 2.1.3.2-8, is described below. The wow/flutter voltage controlled oscillator (VCO) output (WF CLK) is counted in the WF CLK Counter. The count is sampled and placed in a register at the occurrence of each P pulse. The register count is compared with the desired count from a ROM and a 7-bit digital error generated. The digital error passes through a variable gain multiplexer to a D/A converter, first order hold and analog filter. The analog voltage output of the filter is used to control the frequency of the wow flutter VCO thereby completing the control loop. The control loop is opened in the scan region beyond Delphi pulse 1012 and the last frequency of the wow/flutter VCO is held. Beyond Delphi 1012 the loop cannot slew fast enough to follow the scanner motion.

The variable gain multiplexer increases loop gain by a factor of 4 before Delphi 737 at the beginning of scan and after Delphi 943 at the end of scan. The loop and filter characteristics were selected such that the transfer function of the D/A, hold, filter, and VCO is expressed by the equation:

$$\frac{\text{Frequency Change}}{\text{Quantum}} = \frac{K}{a_1} * \frac{a_1}{S+a_1} * \frac{S+a_2}{a_2}$$

$$= \frac{K}{a_2} + \frac{a_2-a_1}{a_2} * \frac{K}{S+a_1}$$

where a_1 = 2.372 rad/sec
a_2 = 350.85 rad/sec
K = 242,500 Hz/sec

A one quantum step error out of the D/A will result in a 691 Hz step and a 240,862 Hz/sec ramping exponential.

2.1.3.2.7 Output Data Multiplexer and Recorders

The Output Data circuitry performs the data management function in the OLS.

The SDF or SDS digital formatted data are selected by uplink or stored command, rate-changed to provide a gap for tape recorder synchronization codes, and gated to one of four tape recorders selected by command.

The SDF or SDS digital formatted data from the playback of one of four tape recorders are gated to one of four data channels, (three of which have operational use) encrypted or sent plain text, and gated to one of four independent data transmitters (three of which have operational use). The tape recorder selection, data channel selection, encrypter mode selection, and data transmitter selection are in response to uplink or stored command.

The RTD digital formatted data from the Data Processing function is gated to one of four data channels, encrypted or sent plain text, and gated to one of four independent data transmitters. The channel selected, encrypter mode selection, and data transmitter selection are in response to uplink or stored command.

The Output Data Multiplexer controls the data, clocks, gap sync and controls sent to the four Primary Tape Recorders. The Data outputs from the Tape Recorders and Real Time Data are then switched to four channels of the OSU.

2.1.3.2.7.1 Output Data Mux - Tape Recorder Write

The control words for direct control of the Tape Recorders (see figure 2.1.3.2-9) are held and also used to select the proper clock frequency to be sent to each recorder. The direct controls to each recorder consist of a power enable (TRxPRE), a read/write control (TRxWR), and two speed controls (TRxDR1 and TRxDR2). A separate control word is held and used to select the desired data stream (SDF or SDS) to be sent to each recorder. A sync signal, which indicates the gap period, is sent to each recorder. Tape recorder status is sent back to the Processor by two control signals from each recorder.

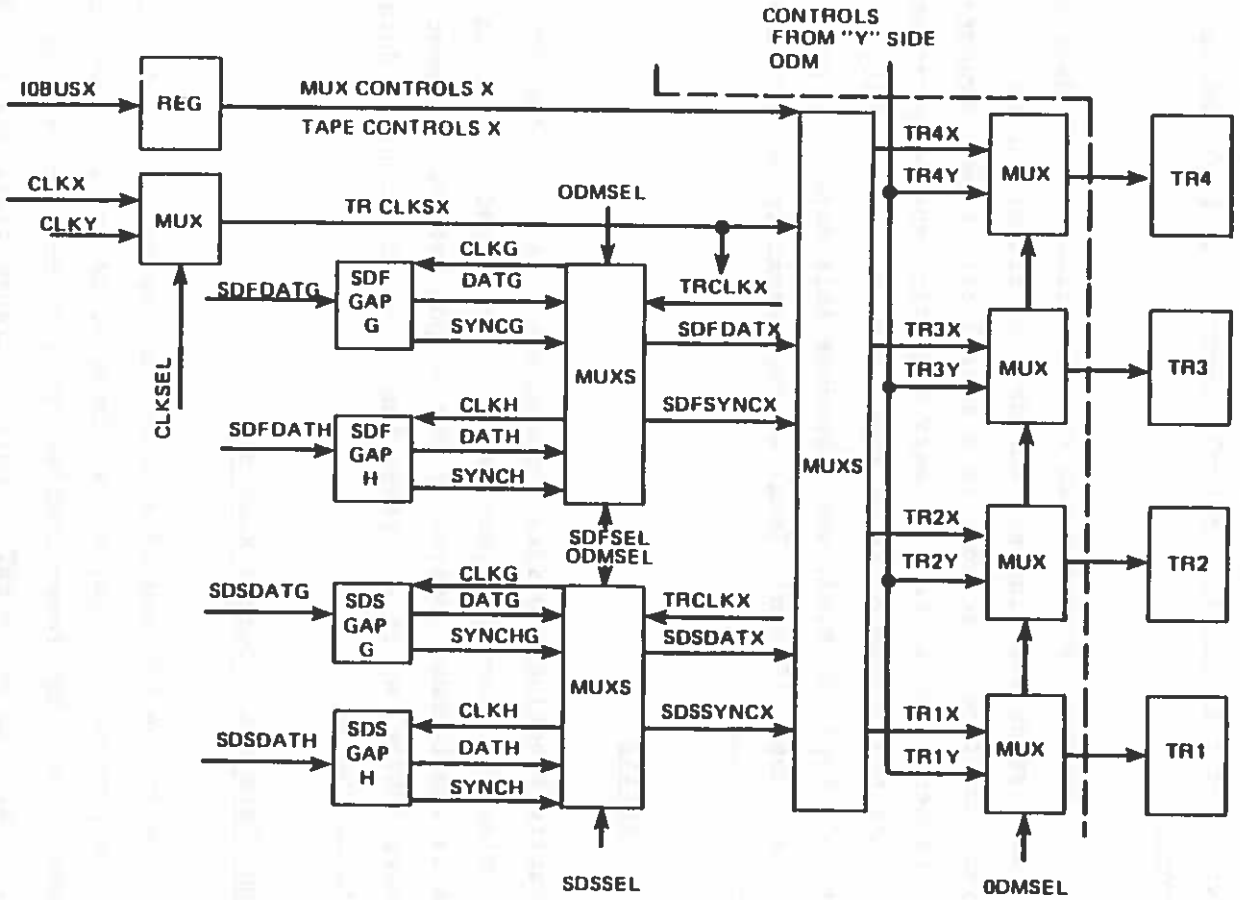

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Figure 2.1.3.2-9. Tape Recorder Write Controls

These signals are:

Beginning of Tape
End of Tape

These signals are received as shown in figure 2.1.3.2-1.

2.1.3.2.7.2 Data Storage

The Data Storage function is implemented by four identical primary tape recorders each with their associated control, record, playback and data buffering electronics.

Each of the four primary recorders can record serial digital data at any one of the three data rates and playback the data at either one of two data rates. Data played back from a recorder is a serial bit stream, synchronized with the proper frequency clock. Each primary magnetic tape recorder can record a digital data bit stream of 66.56 kbps (400 minutes capacity), 665.6 kbps (40 min) or 1331 kbps (20 min), and reproduce this data at a rate of 1331 kbps (20 min) or 2662 kbps (10 min). Total storage capacity per primary recorder is 1.67×10^9 bits.

2.1.3.2.7.3 Data Security

The Data Security function provides cryptographic security for RTD or stored data transmissions from the spacecraft to the ground. The plain text of the data streams is input under control of the Output Data Multiplexer to one of three encrypters (BBT's) which enciphers the data and outputs a data stream of encrypted data to the OSU.

2.1.3.2.7.4 Output Data Mux - Output Routing

Output data flow to the OSU and BBTs (shown in figure 2.1.3.2-10) is controlled by three processor output words. These words contain Power Enables for the Data Transmitters, BBT Power Enables, bits to route data from recorders to BBT's, bits to route BBT outputs to transmitters via the OSU, and bits to select clock frequencies for the BBT's. The BBT Power Enable signals

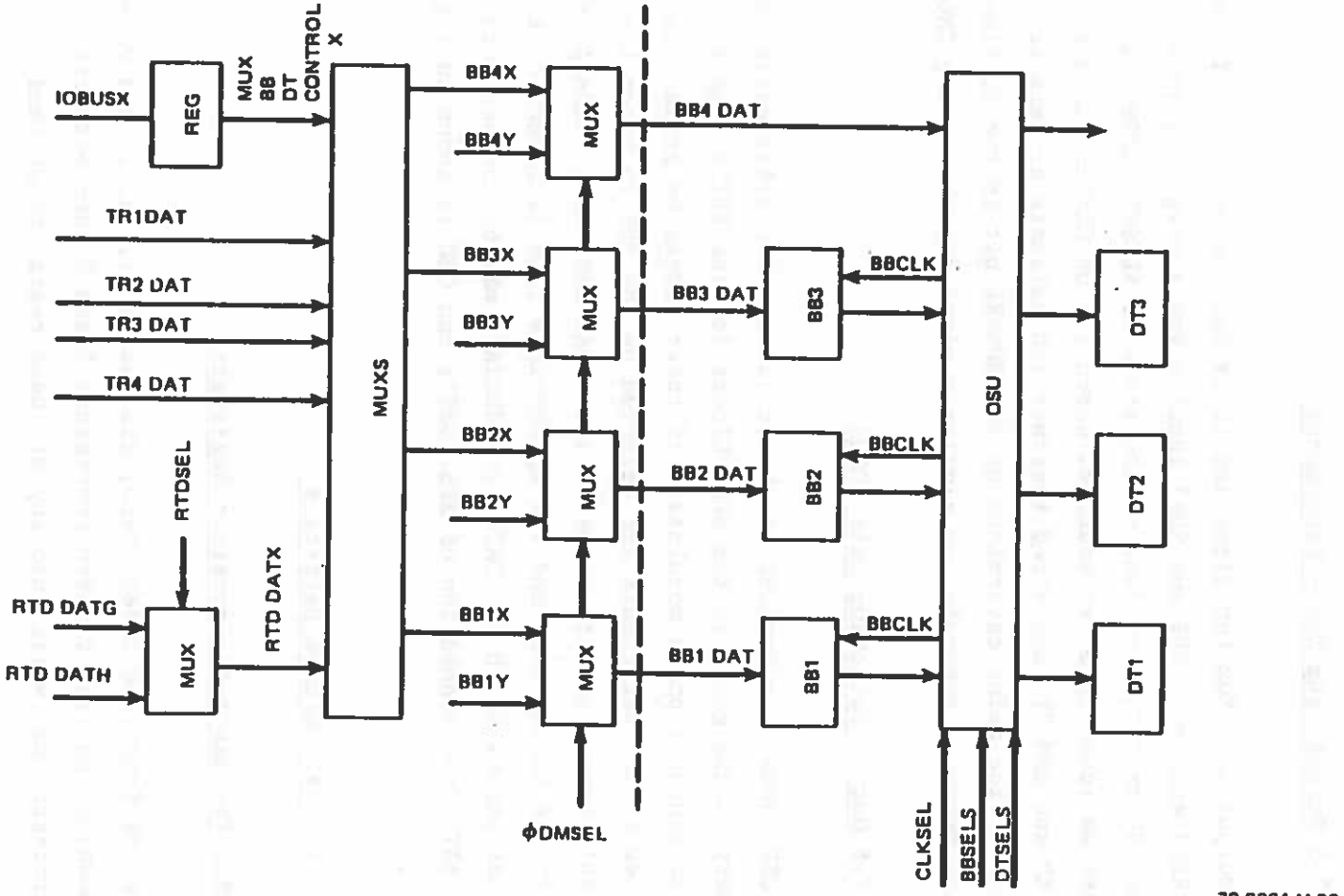


Figure 2.1.3.2-10. Output Data Routing

are also used to determine whether the data will be sent clear or encrypted. As far as hardware is concerned, any data source (RTD or recorder) may be connected to any BBT, and any BBT may be connected to any of 4 independent transmitter inputs (again, only 3 are used operationally).

2.1.3.2.7.5 Output Data Mux - Redundancy

The Output Data Mux functions are fully duplicated in I/O Y. Data (SDF, SDS and RTD) and sync (SDF and SDS) input signals originate in either Formatter "G" or "H", depending on the state of SDFSEL, SDSSEL and RTDSEL. Clocks are selected from two sources, depending on CLKSEL. Line driver outputs of ODM "X" and ODM "Y" are wired together and tristate drivers are used, with the active device being determined by the ODMSEL bit in the Configuration Word. Tape recorder controls are similarly wired together using CMOS switches.

2.1.3.2.7.6 Output Switching Unit (OSU)

The OSU contains redundant clock oscillators and differential drivers for the primary clocks going to the SPS. Clocks for the BBT's come directly from the OSU to minimize phase modulation of these clocks by primary data. The frequencies of the BBT clocks are selected by the SPS to match the data going to each BBT. Encrypted data (BxDATA) and clear text data (RxDATA) from each BBT are routed to the OSU, and the appropriate type is selected. Each pair of transmitter inputs (such as ODATA1 and ODATA5) may be connected to the data from any BBT. Interconnection of SPS, BBT's and OSU is shown in figure 2.1.3.2-11.

2.1.3.2.8 Special Purpose Registers

2.1.3.2.8.1 Processor-to-Processor Registers

There are four 16-bit registers, designated R1, R2, D1 and D2 which serve as a communication link between processors C and D when both are in use. Either processor may write into any of these registers or read out of any of

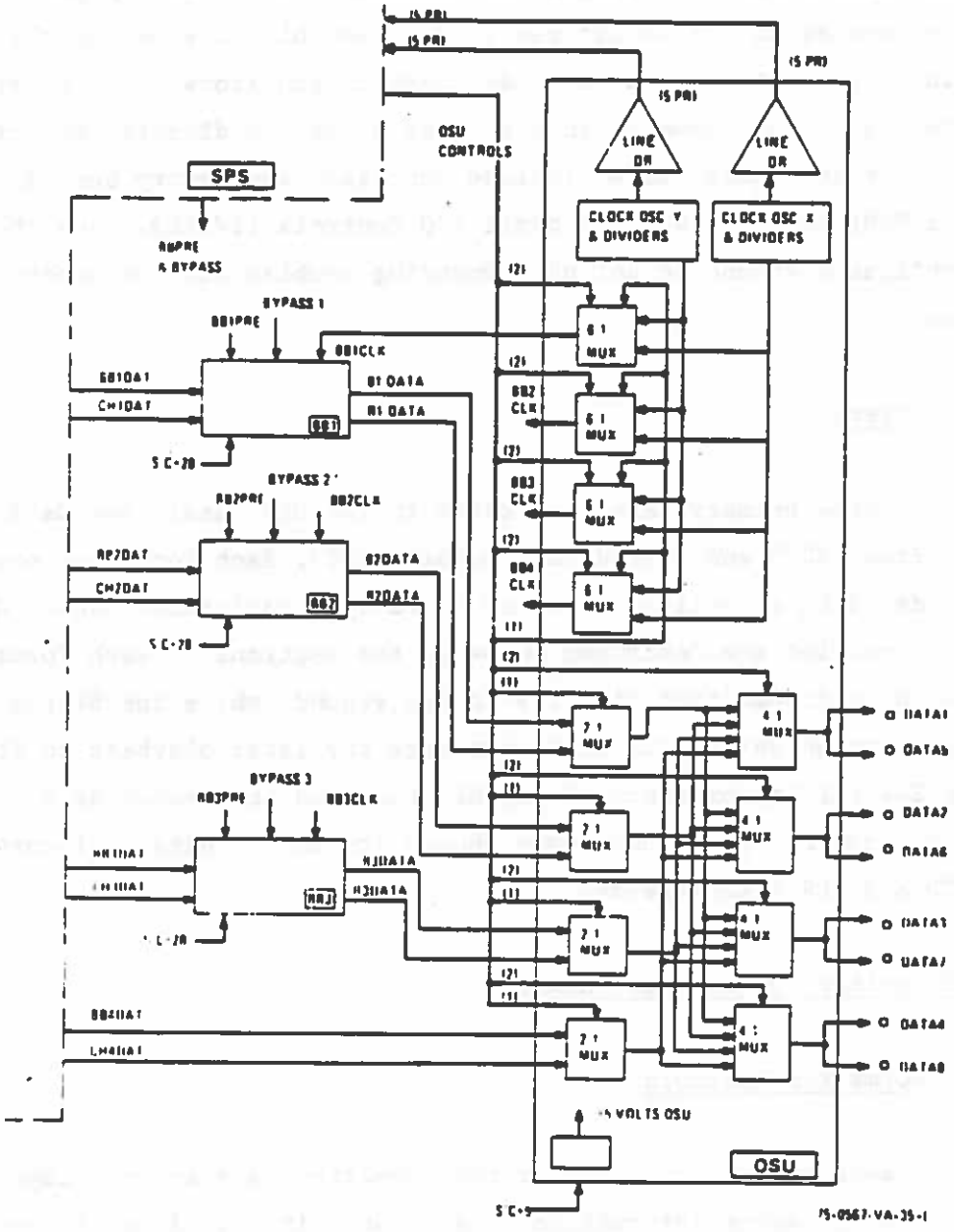


Figure 2.1.3.2-11. BBT's and OSU

them. The communication protocols are determined by the software running in the two processors.

2.1.3.2.8.2 Configuration Register

The bits which select the primary or redundant block for any particular function are located in one 16-bit register. These bits are set by the processor in response to uplink commands. Certain functions vital to receiving and interpreting uplink commands in the first place are directly selected by spacecraft interface lines. These include processor and memory bus selection (PROCSEL and MEMBUSSEL) as well as basic I/O Controls (IFSEL). Thus the system can be reconfigured around an uplink commanding problem without depending upon uplink commands.

2.1.3.3 Formatters

There are three primary data formatters in the OLS: Real time Data (RTD), Stored Data Fine (SDF) and Stored Data Smooth (SDS). Each formatter provides digitized video data as well as line and frame synchronization codes. Other types of data carried are described below in the sections on each formatter. Real Time Data is transmitted directly to the ground, while the Stored Data streams are recorded on the OLS tape recorders for later playback to the ground. The Special Sensor Processing (SSP) function is treated as a fourth formatter in terms of redundancy, even though its output data is incorporated into the RTD and SDS data streams.

2.1.3.3.1 Formatter Controls and Memory

2.1.3.3.1.1 Formatter Controls

Formatter mode control and some of the formatter data are provided by the processors. The processor information is available in both I/Os if they are both powered. The interface select (IFSEL) from the spacecraft determines which I/O actually provides output words to the Formatter Buses and which I/O

provides the input flags from the formatters to the processor. (Reference figure 2.1.3-2.)

Based on uplink or stored commands, the processor selects which formatters are selected, which video sources are selected, which set of encoder information is used for sampling, which clock source drives the formatters, and which modes the formatters use. (Ref. Figures 2.1.3-4 and 2.1.3-5). The processor sends ancillary data and telemetry data to the formatter memory for use in the SDF and SDS formatting. The processor sends direct mode data message information to the RTD formatter. The processor sends offset information to a register in the formatter and this information is used in the RTD, SDS, and SDF formatters. The processor sends mode and type information to the SSP formatter based on the information in the uplink memory. The processor sends format information to the SSP memory based on the information in the uplink memory. The processor sends special sensor power enables and serial commands to the SSP hardware based on real time or stored commands. (Reference Figures 2.1.3.3-1 and 2.1.3.3-2.)

The formatters use the power as selected during the turn on sequence, the selected video, sensors, clock, encoder, and processor information to generate formatted data as described in the Data Specification (IS-YD-821).

The data processing function converts the four analog outputs (or their redundant counterpart) of the Channel Analog Electronics (LF, LS, TF and TS) into digital formats in three basic data management modes: Real Time Data (RTD), Stored Data Fine (SDF), and Stored Data Smooth (SDS). Special sensor data as processed by the Special Sensor Processor (SSP) is formatted in the RTD and SDS data streams. The hardware used to format these data streams is described in the following sections.

2.1.3.3.1.2 Formatter Memory

The Formatter Memory consists of a 4-K word by 18-bit core memory and associated access logic. This word length is needed for holding the SDS video data (8 bits of L data and 10 bits of T data) in a single memory location.

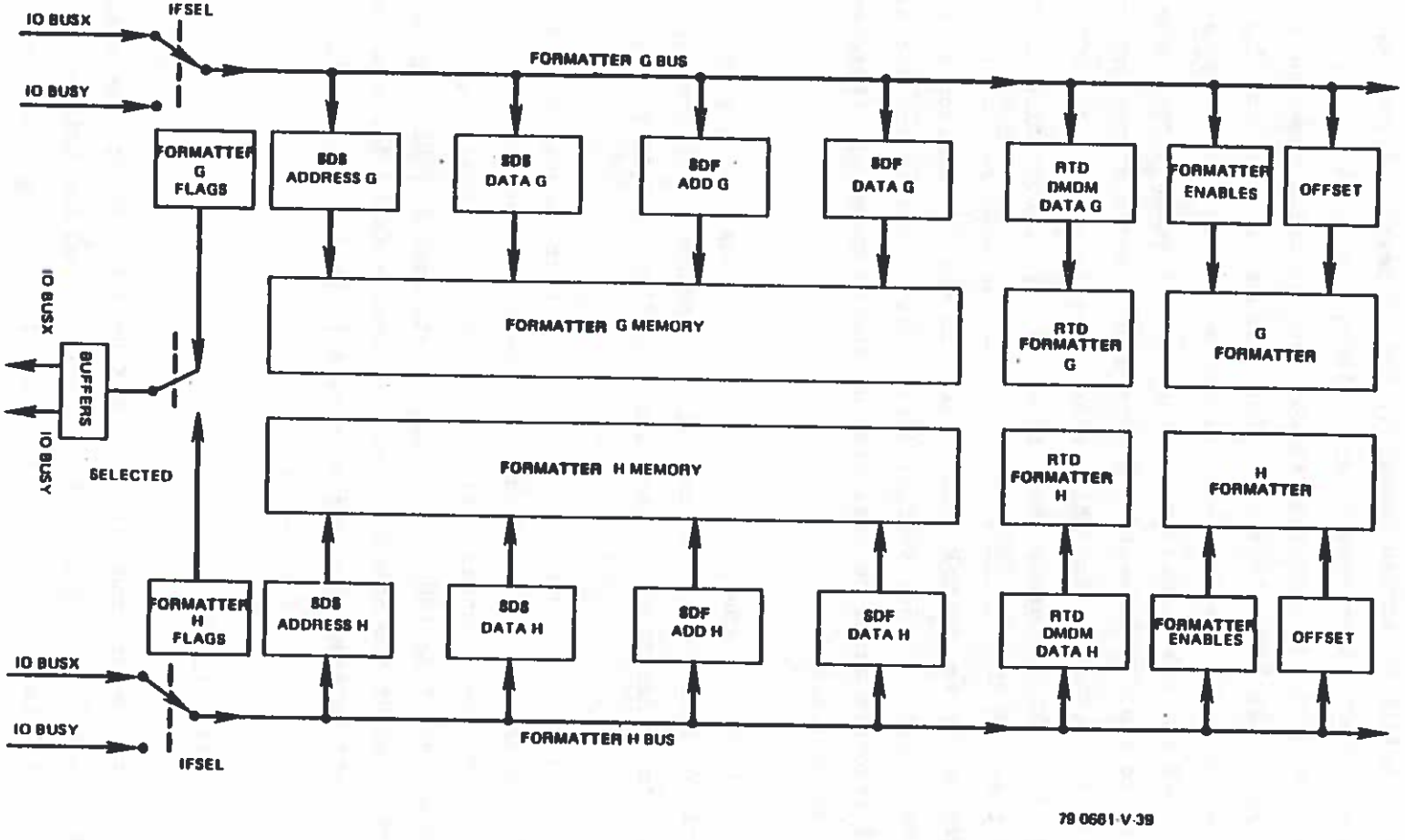


Figure 2.1.3.3-1. Formatter Bus - SDS, SDF, RTD

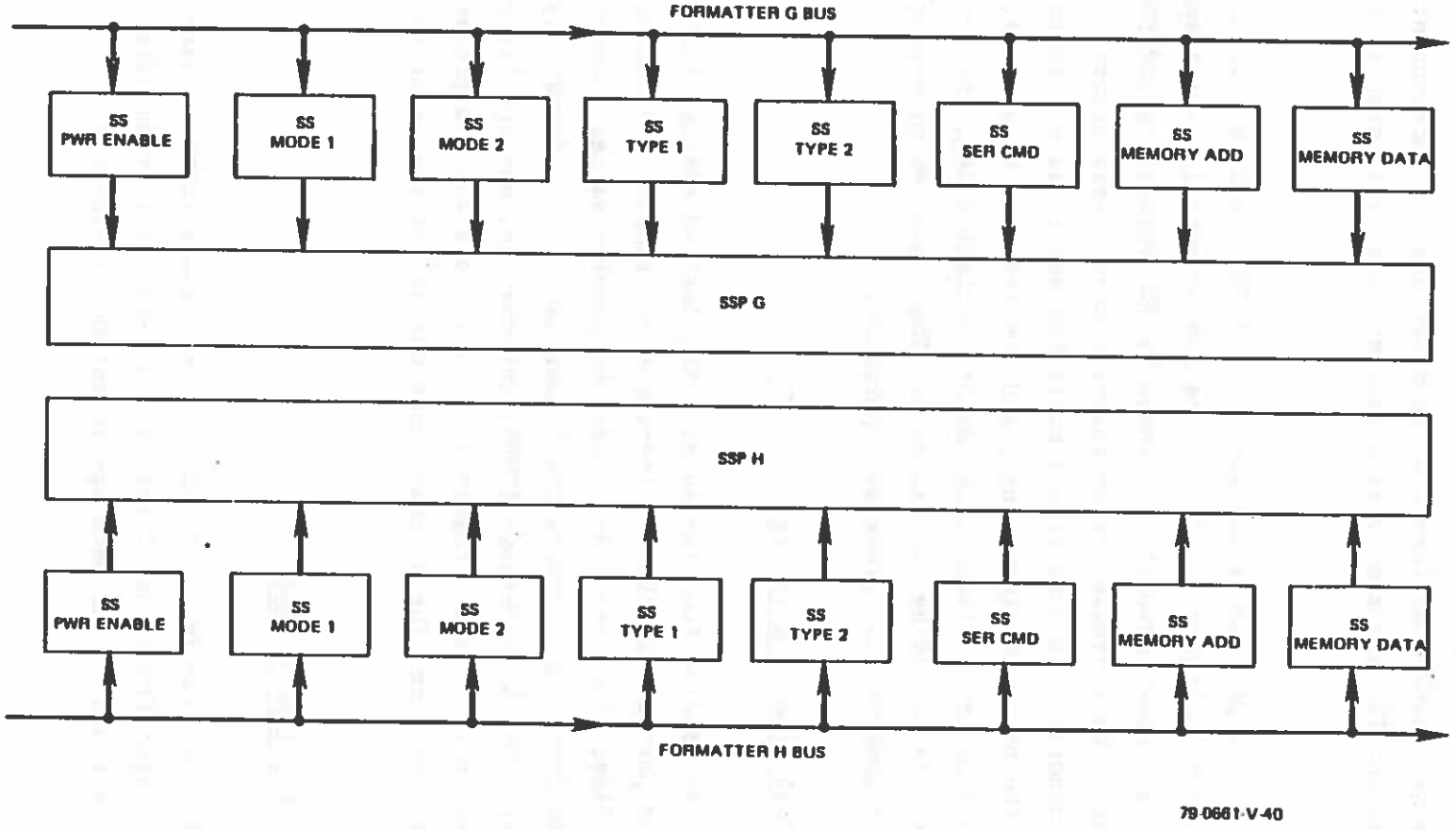


Figure 2.1.3.3-2. Formatter Bus - SSP

There is a Formatter Memory with its associated controls in each formatter section (G and H). Whenever a formatter section is powered up, the formatter memory is available. A failure in a formatter memory section would necessitate powering up the other formatter and using the SDF and SDS sections from the other formatter, since the formatter memories are not independently cross-connected. The SSP memory is a separate unit discussed in paragraph 2.1.3.3.5.1.

Access by the processors and the SDF and SDS formatters is on a priority basis. As shown in figure 2.1.3.3-3, the SDS Integration write and read accesses have highest priority, followed by SDF Formatting and SDS Formatting read requests. The processor write requests have lowest priority. When a request is honored, the appropriate multiplex switch is closed to place the address on the memory address lines, and, in the case of a write, place the data on the data input lines. After an appropriate delay, the output data is available and is caught by the requester. There are two processor write access ports to accommodate dual processor operation.

2.1.3.3.2 Real Time Data Processing (RTD)

The RTD processing function selects the desired analog inputs for the fine and smoothed portions of the RTD transmission, samples the analog values at the proper fixed clock rate, digitizes the sampled values, formats the samples into a frame format and formats the frames into a line format. Synchronization codes, Direct Mode Data Message (DMDM) information, and Special Sensor data are included in the format. Figure 2.1.3.3-4 shows the RTD processing function in block diagram form. The diagram shows one of the two identical redundant RTD sections.

2.1.3.3.2.1 RTD Line Format

The RTD line is made up of Video Frames, Blank Frames, Alarm and Line Sync Frame and Subsync Frame (see figure 2.1.3.3-5). Further details on the RTD format can be found in the Data Specification (IS-YD-821).

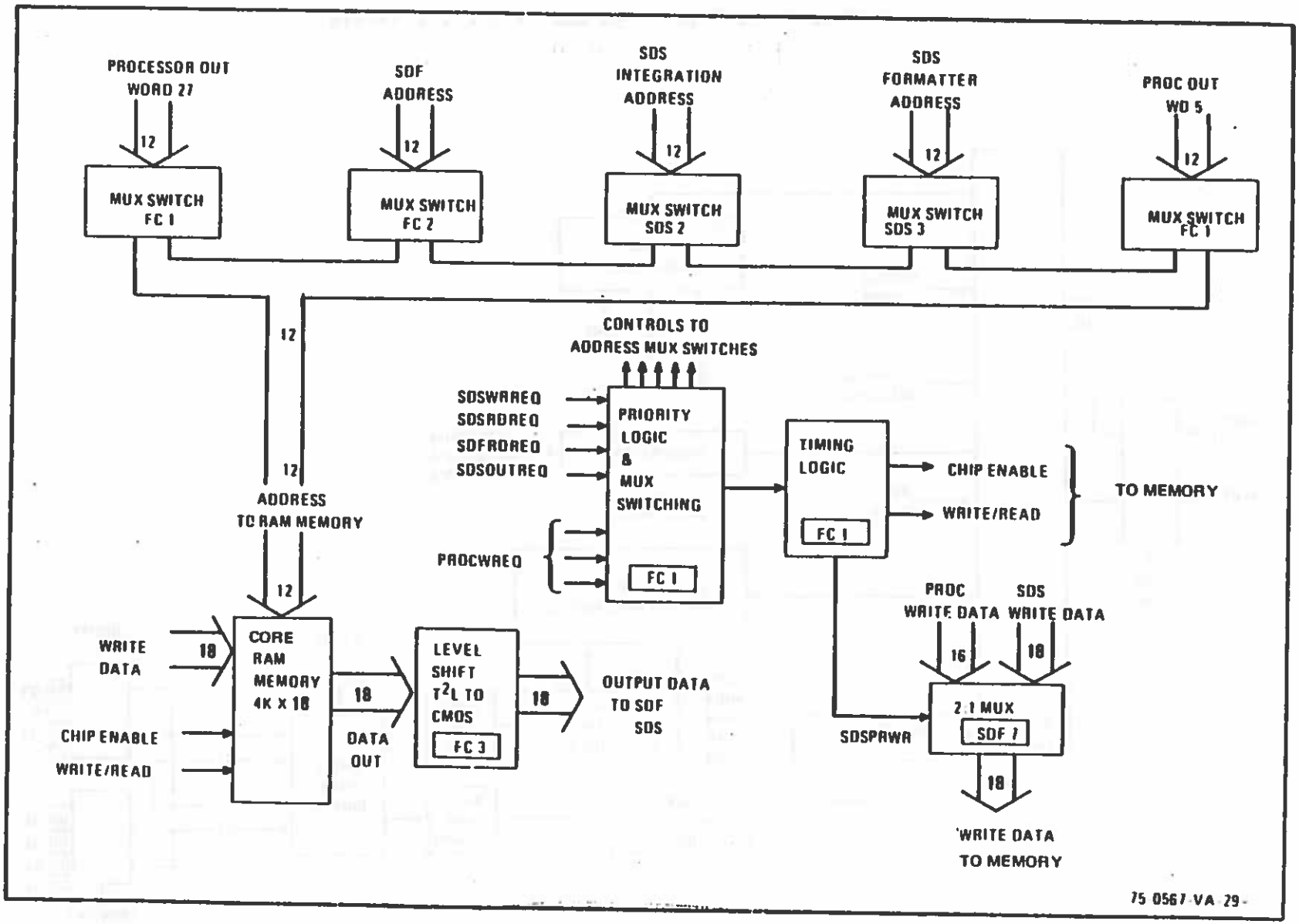


Figure 2.1.3.3-3. Formatter Memory Access

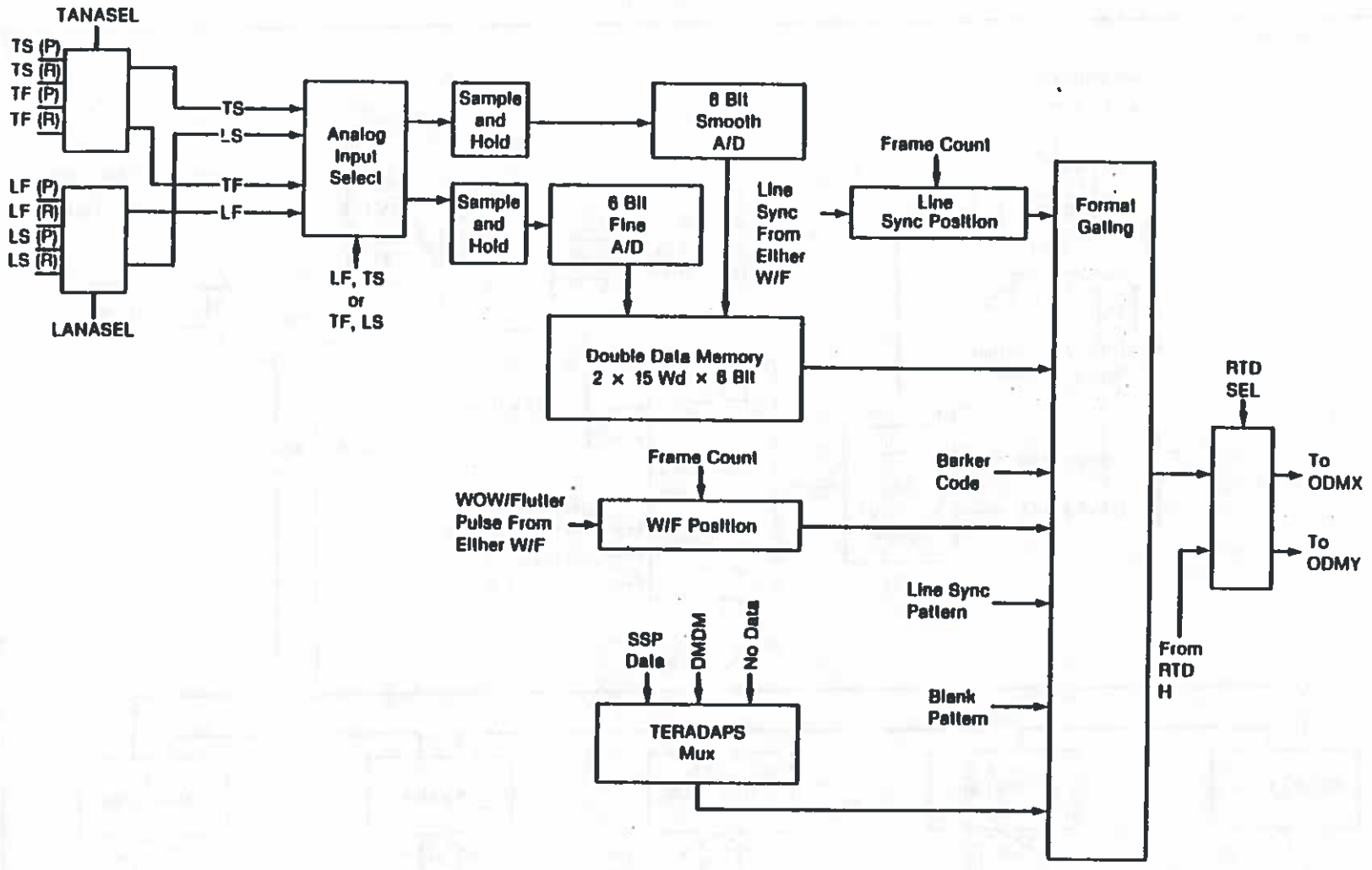
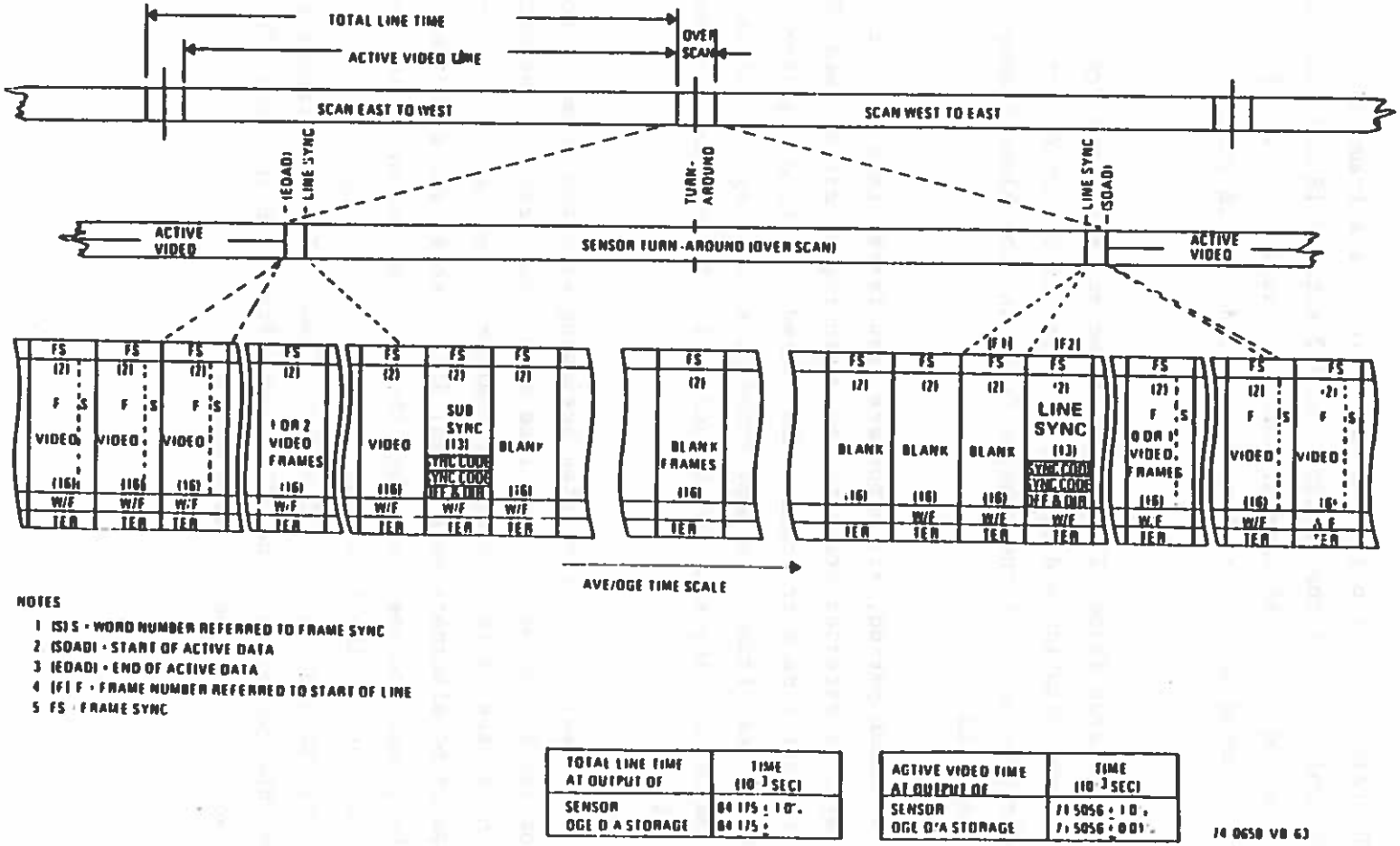


Figure 2.1.3.3-4. RTD Processing Block Diagram



NOTES

1. (S) S - WORD NUMBER REFERRED TO FRAME SYNC
2. (SOAD) - START OF ACTIVE DATA
3. (EOAD) - END OF ACTIVE DATA
4. (F) F - FRAME NUMBER REFERRED TO START OF LINE
5. FS - FRAME SYNC

TOTAL LINE TIME AT OUTPUT OF	TIME (10^{-3} SEC)
SENSOR	84.175 ± 1.0
OGE'D A STORAGE	84.175 ±

ACTIVE VIDEO TIME AT OUTPUT OF	TIME (10^{-3} SEC)
SENSOR	78.5056 ± 1.0
OGE'D A STORAGE	78.5056 ± 0.01

74 0658 VB 63

Figure 2.1.3.3-5. Real Time Data (RTD) Line Format

The RTD Video Frame is 150 bits long, and is subdivided into eighteen words. The frame format is repetitive and is output at a bit rate of 1.024 MHz.

The RTD Video Frame is organized with word 1 as a frame sync to maintain proper synchronization at the decoder. Word 2 through 16 are video data with 6 bits of Fine and 2 bits of Smooth. Word 17 contains the wow/flutter (W/F) count as it occurred in the previous frame, and word 18 contains Teradaps data.

The RTD Line Sync Frame, RTD Subsync Frame and RTD Blank Frames are used to provide synchronization and fillers outside the region of active video data. The Teradaps words of the subsync frame and the blank frames contain special sensor data.

In the overscan period, all zeros are transferred into the Data Memories until Line Sync is detected prior to the beginning of active data. The frame bit count at which line sync occurred is stored in a hold register for transfer in the next frame. The next frame after line sync contains an alarm code followed by the line sync count, and in the frame after that the samples of video begin.

Data Frames cease to be formatted beginning with the frame following the detection of the End of Active Data line sync. That frame is the RTD Subsync Frame, which is used by the ground deformatter to locate the line sync reference pulse on alternate scan lines. This enables one direction line scans in the ground equipment although the data was collected in alternate directions. As before, the frame bit count at which line sync occurred is stored for transmission in the RTD subsync frame. RTD Blank frames are used to fill the interval between the RTD Subsync Frame and the next RTD Line Sync Frame which begins another line format.

2.1.3.3.2.2 RTD A-to-D Converters

L and T video inputs are selected independently from their primary or back-up sources. A processor output bit selects either LS and TF or TS and LF data mode in response to a stored or real time command. Video sampling begins at the line sync pulse entering the active scan and ends at line sync leaving active scan. The Fine video is sampled at a 102.4 kHz fixed rate, and converted to a 6-bit digital value using a successive approximation A-to-D converter as shown in figures 2.1.3.3-6 and 2.1.3.3-7. One smooth sample value corresponds to five fine samples in the along-scan direction. Thus, the smooth video is sampled at a 20.48 kHz fixed rate, held, and converted to an 8-bit digital value using a similar A-to-D. It should be noted that no along-track smoothing of RTD smooth video is done in the AVE. The A/D transfer functions are given in figure 2.1.3.3-8.

2.1.3.3.2.3 RTD Double Data Memory

The Double Data Memory is a data storage buffer which holds the data until clocked out by the timing commands. A full frame (15 fine samples and 3 smooth samples) of video is accumulated in one-half of the 8-bit Double Data Memory while the other halt is being read out by the Memory clock gating. The data is then output to the RTD formatting circuits.

2.1.3.3.2.4 RTD - Ancillary Data

The Teradaps bits of every frame consist of either Direct Mode Data Message (DMDM), special sensor data, or a fixed "No Data" code. The DMDM data is obtained from the processor. Special sensor data is obtained as needed from the active SSP unit.

2.1.3.3.2.5 RTD Format Controls

The RTD frame format contains 150 bits, so a decimal modulo 150 counter is decoded to generate start and stop signals for each type of information which is to be gated into the output data stream (see Figures 2.1.3.3-9 and

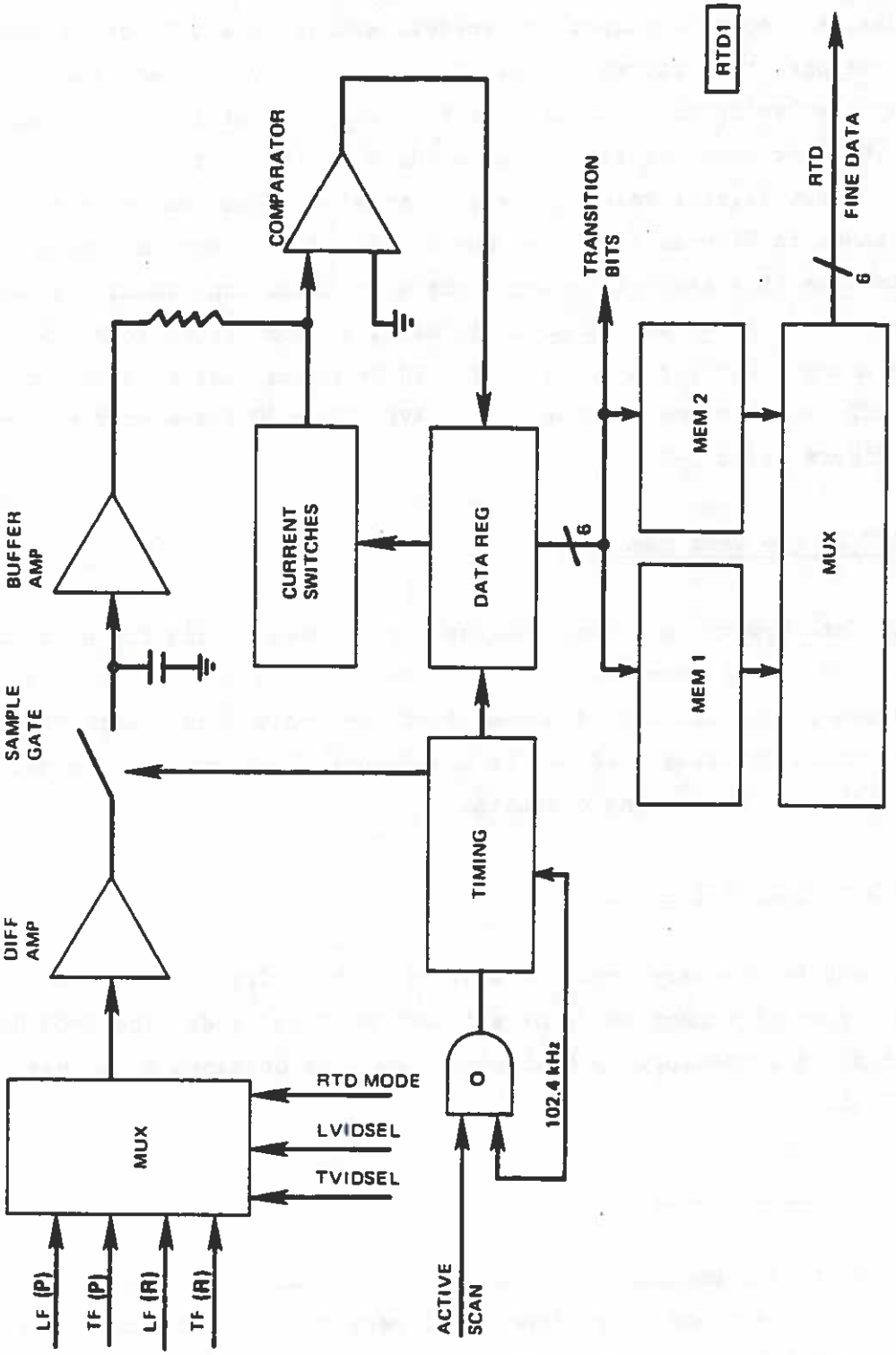


Figure 2.1.3.3-6. RTD Fine A/D Converter

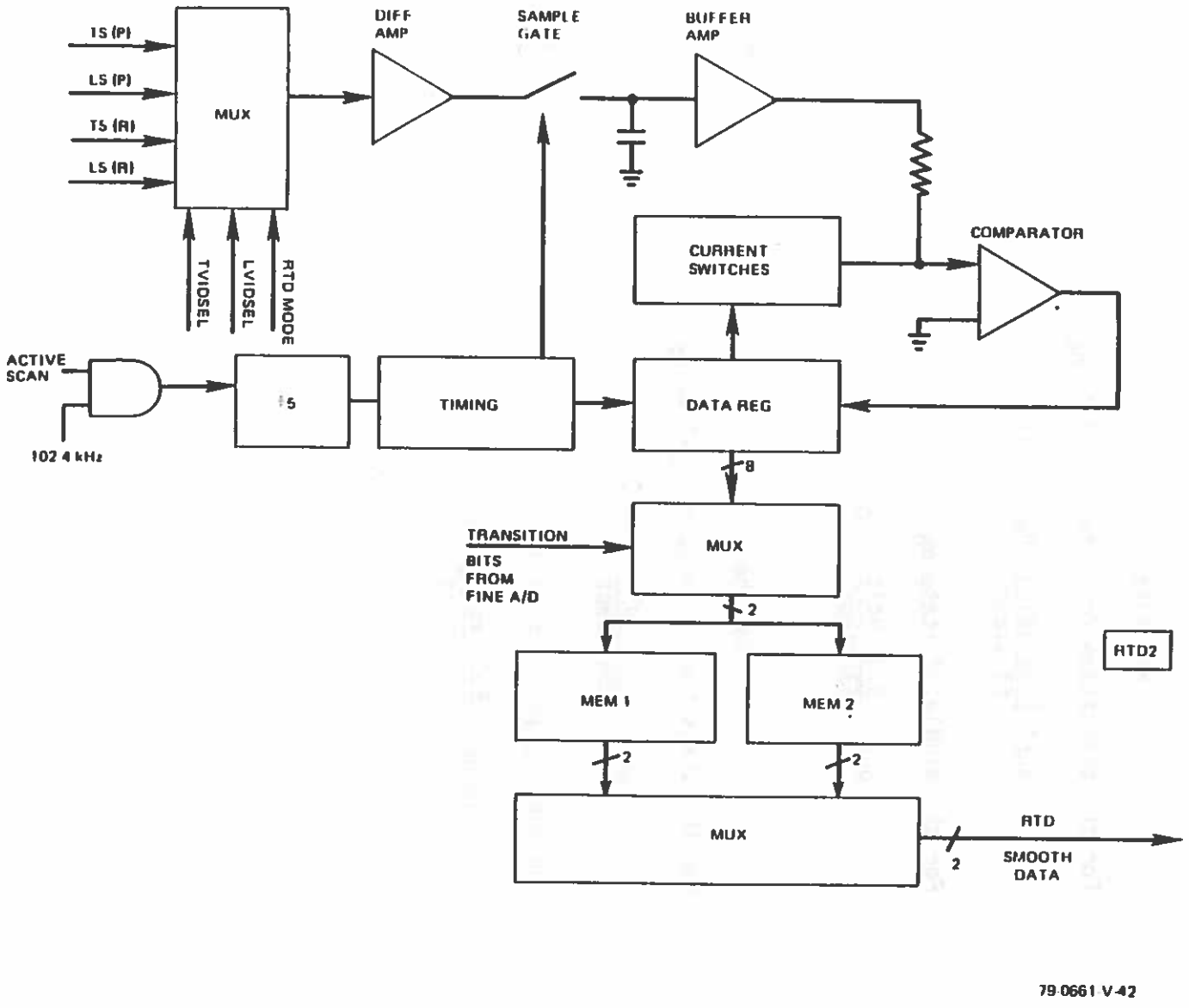


Figure 2.1.3.3-7. RTD Smooth A/D Converter

RTD Fine

For the transition from state n_0-1 to n_0

$$V_{input} = \frac{5.00 \text{ volts}}{63 \text{ steps}} (n_0 - 0.5)$$

For the middle of state n_0

$$V_{input} = \frac{5.00 \text{ volts}}{63 \text{ steps}} (n_0)$$

RTD Smoothed

For the transition from state n_0-1 to n_0

$$V_{input} = \frac{5.00 \text{ volts}}{255 \text{ steps}} (n_0 - 0.5)$$

For the middle of state n_0

$$V_{input} = \frac{5.00 \text{ volts}}{255 \text{ steps}} (n_0)$$

Figure 2.1.3.3-8. RTD A/D Transfer Functions

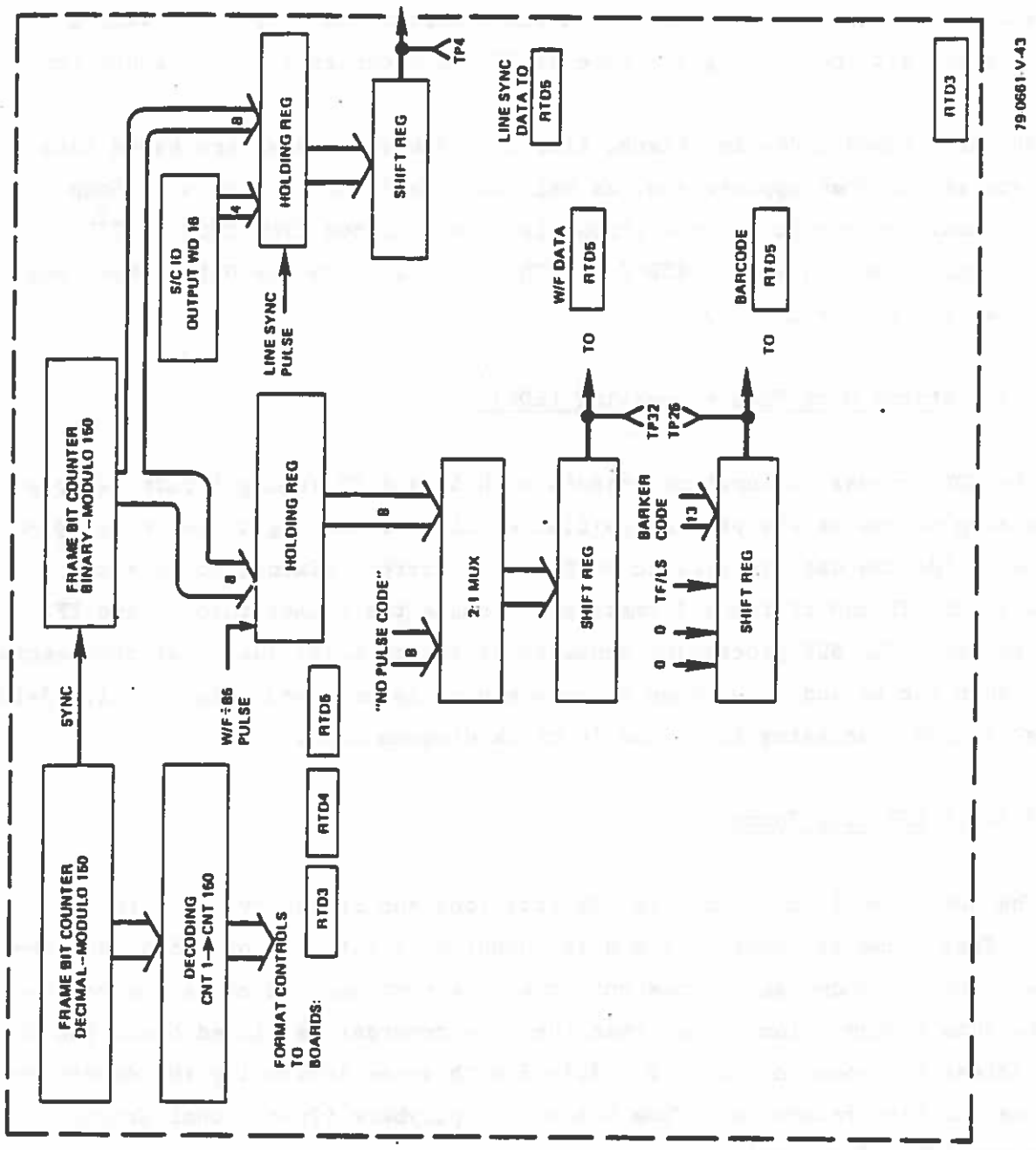


Figure 2.1.3.3-9. RTD Format Controls

2.1.3.3-10). A binary count is also kept for each bit of a frame, and at the Line Sync pulse this count is sampled and held, to become part of the following Line Sync or Subsync frame The spacecraft I.D. code from the processor is sampled at the same time. The binary bit frame counter is also sampled at every "wow/flutter + 85" pulse (every 166 us nominal), and the result is put out in the following frame. This information is used by ground equipment to correct RTD Video for wow and flutter. If no "wow/flutter 85" pulse occurs in a frame, a specific "No Pulse" code is output A fixed Barker code (13 bits) with a variable tag bit identifying the type of RTD data occurs first in every frame.

Specific fixed codes for Blank, Line Sync Subsync frames are gated into the data stream when appropriate, as well as Offset and Direction of Scan information. The resulting data stream is level shifted from CMOS to T^2L sent through a mux to select RTD G or RTD H, and sent to the Output Data Mux sections (see figure 2.1.3.3-11).

2.1.3.3.3 Stored Data Fine Processing (SDF)

The SDF processing function accepts both LF and TF analog inputs, samples the analog values at the proper wow/flutter clock rate, digitizes the sampled values, holds the data in elastic buffers for correct timing, formats the samples into TF and LF frame formats and formats the frames into LF and TF line formats. The SDF processing consists of two parallel identical processors - one each for LF and TF - whose outputs may be interleaved. Figure 2.1.3.3-12 shows the SDF processing functions in block diagram form.

2.1.3.3.3.1 SDF Line Format

The SDF video frame format is 208 bits long and is subdivided into 33 words. This frame is repetitive and is output at a bit rate of 665.6 kHz. The frame format is shown as it goes onto the tape recorder, which is the reverse of the data transmission format when the tape recorder is played back. The SDF line format is shown in figure 2.1.3.3-13 with arrow indicating the direction of time for both record (AVE Time Scale) and playback (Operational Ground Equipment (OGE) Time Scale).

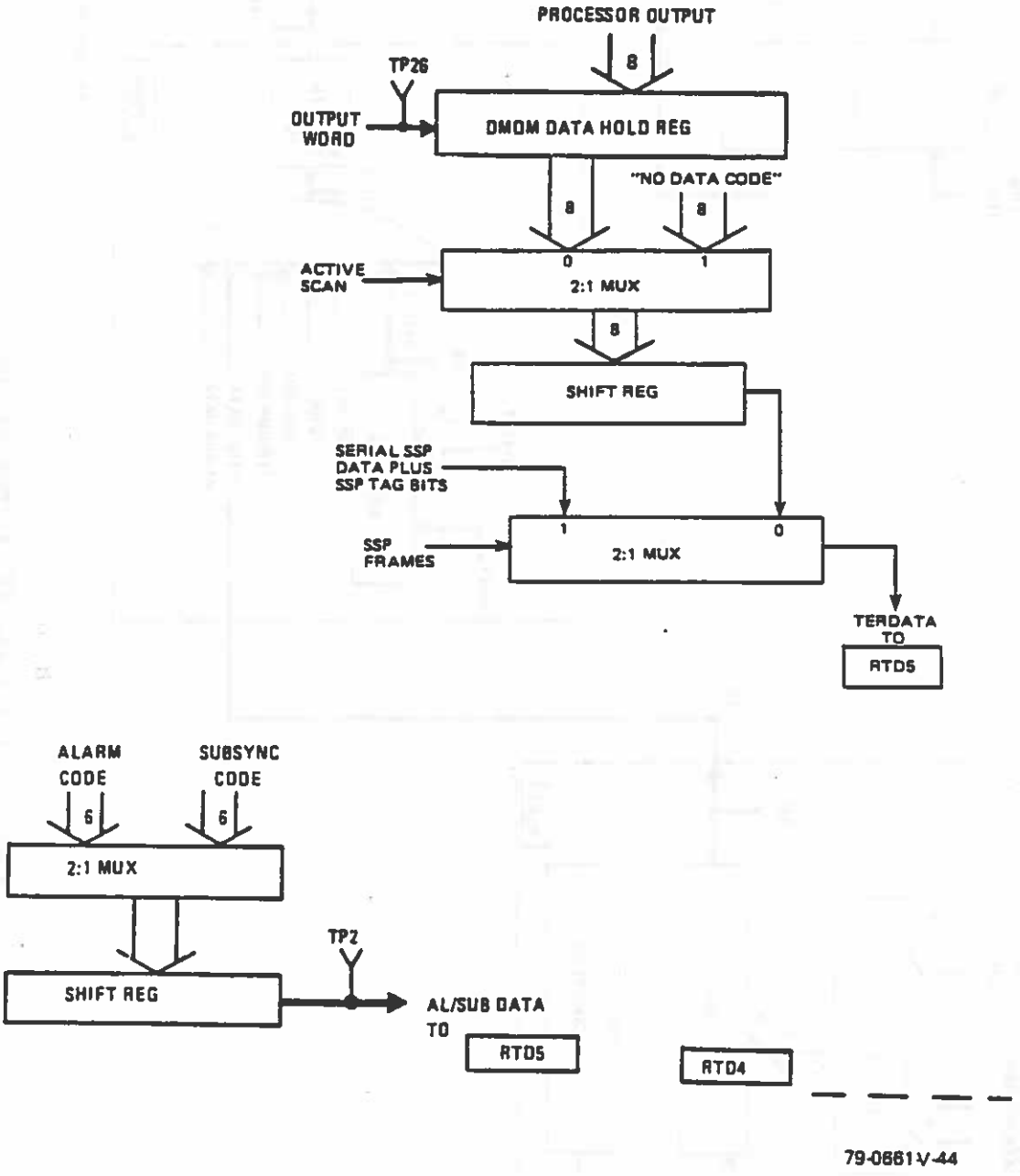


Figure 2.1.3.3-10. RTD-SSP and DMDM Data

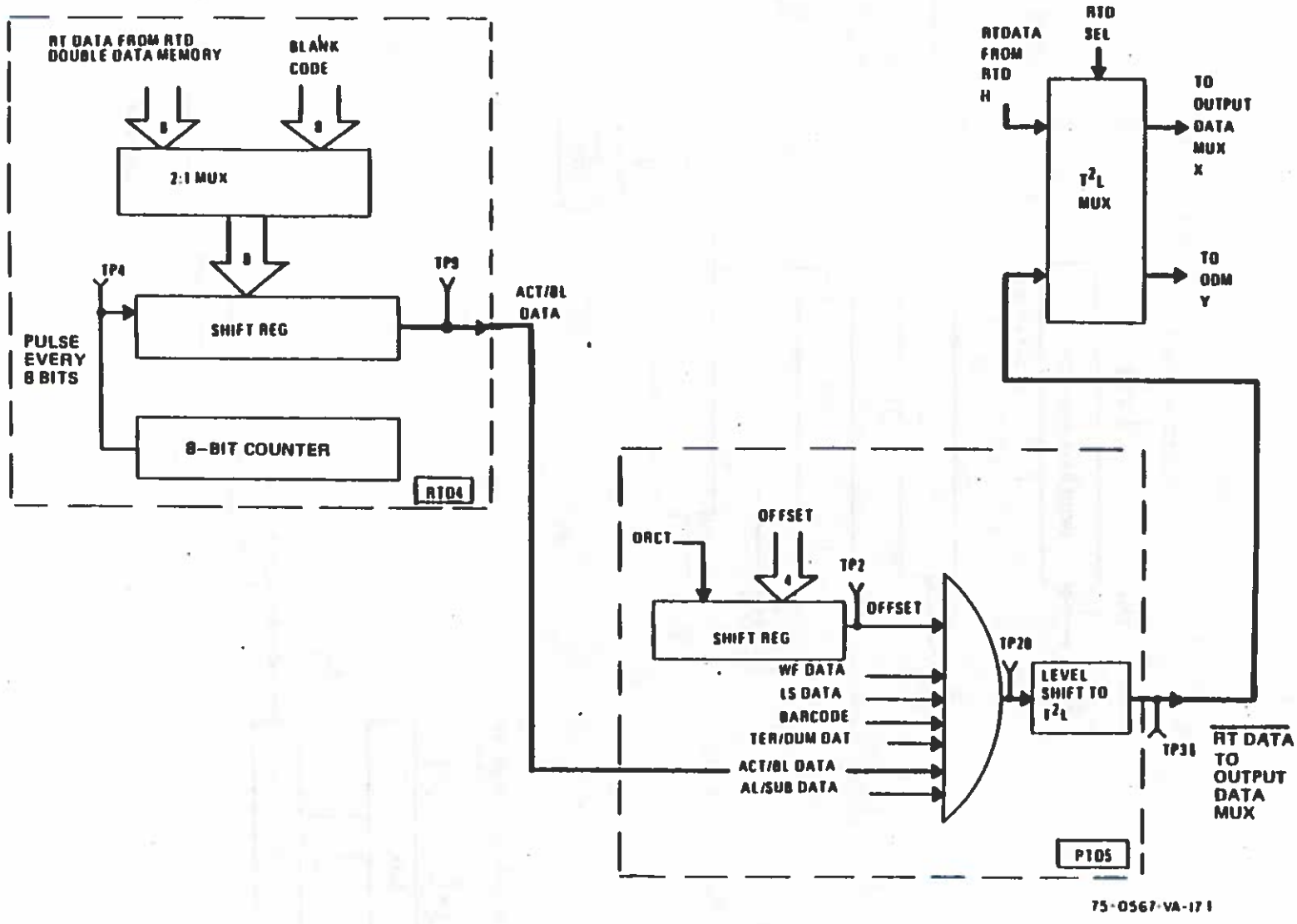


Figure 2.1.3.3-11. RTD Format Gating

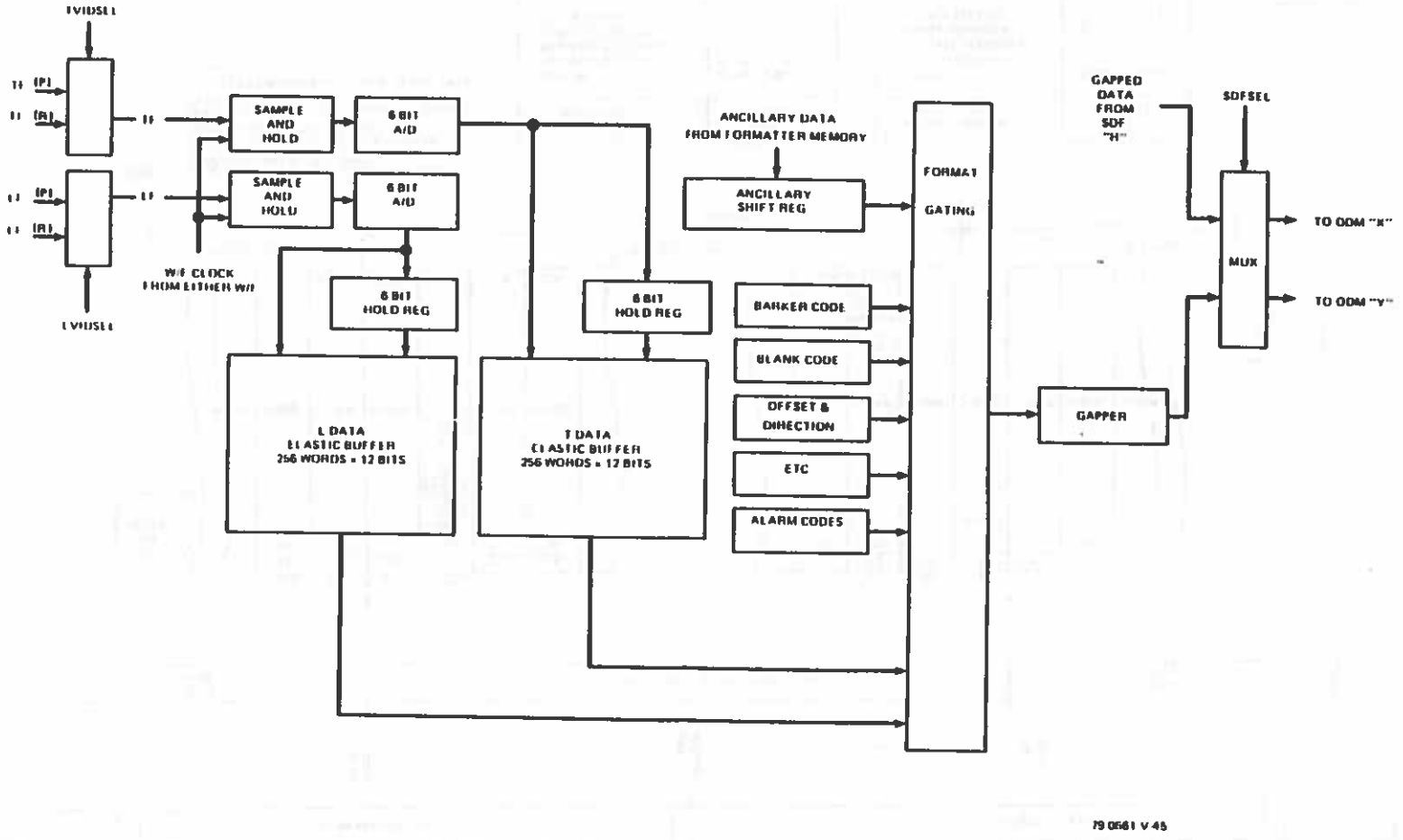


Figure 2.1.3.3-12. SDF Processing Block Diagram

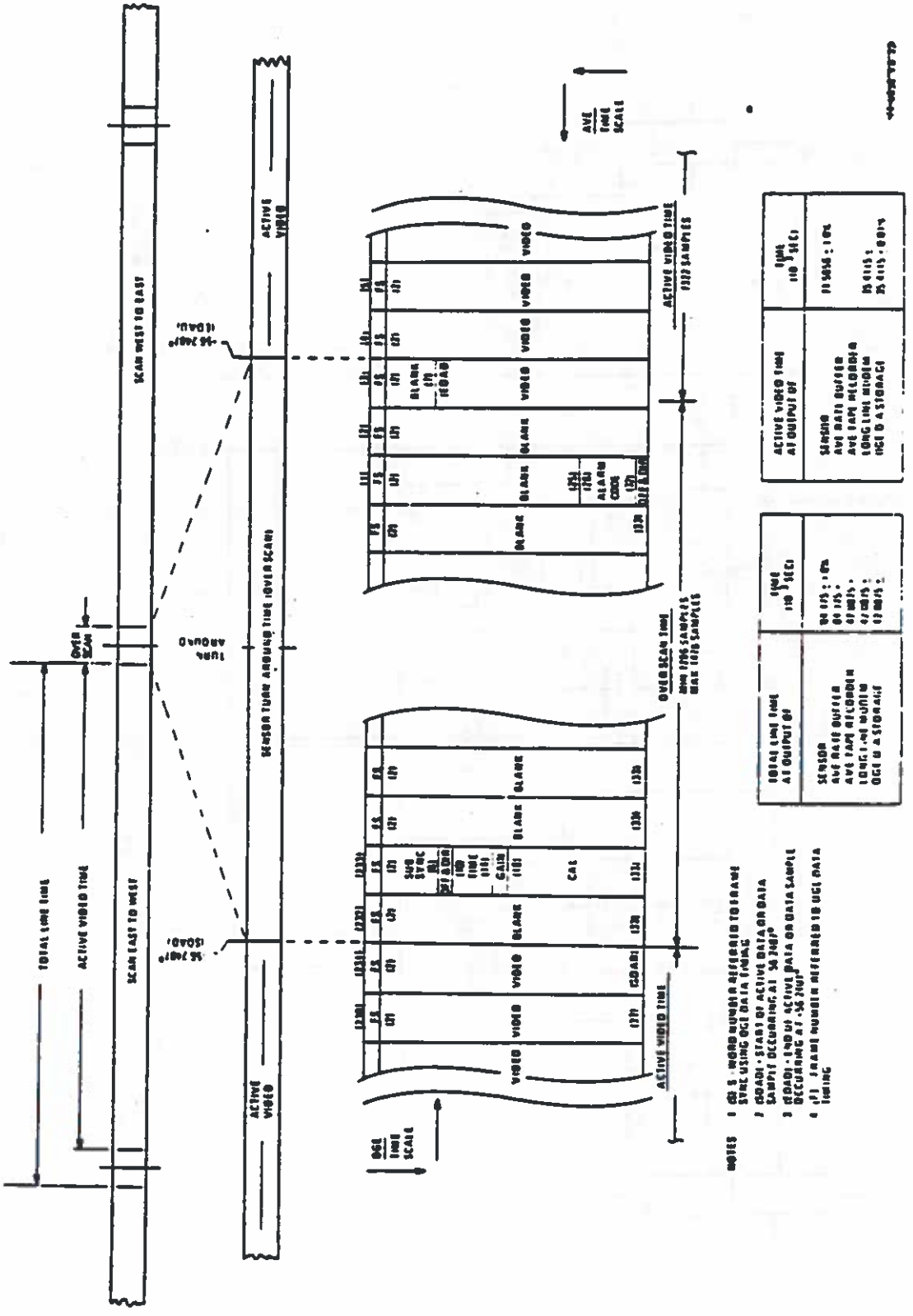


Figure 2.1.3.3-13. Stored Data Fine (SDF) Line Format

Further details on the SDF format can be found in the Data Specification (IS-YD-821).

The SDF Line Sync Frame, SDF Subsync Frame, and SDF Blank Frame are used to provide synchronization and fillers outside the region of active video data. The line format figure indicates the placement of the SDF Video Frames, the SDF Blank Frames, the SDF Subsync Frame and the Line Sync Frame.

2.1.3.3.3.2 SDF A-to-D Converters

LF and TF video inputs are selected, independently, from their primary or redundant analog sources.

The fine video (both L and T) is sampled at a "Wow/Flutter ÷ 5" rate (nominally 102.4 kHz). The first sample occurs at a point (VCOSET) which is time-corrected to make it line up with the actual 996th delphi pulse (Start of Active Data), thus correcting for differential delays of video and encoder information. Parallel 6-bit successive approximation A-to-D converters are used for L and T video, and the 6-bit samples are loaded alternately into holding registers to reduce the speed of data through the elastic buffers. This continues until 7322 samples have been digitized, which coincides with End of Active Data (EOAD). (See figure 2.1.3.3-14.) The A/D transfer functions are shown in figure 2.1.3.3-15.

2.1.3.3.3.3 SDF Elastic Buffers

Elastic buffers, each 12-bits wide and 256-bits long, are required because the A-to-D converters provide data at a nonuniform wow/flutter clock rate, while the SDF Formatter requires data at a fixed clock rate. The buffers start out empty at the beginning of scan, and they are allowed to accumulate 128 loads (256 video samples) before the formatter begins to output data. Inputs then continue simultaneously until End of Active Data when the inputs are cut off and the formatter empties the buffers. (See figure 2.1.3.3-16.)

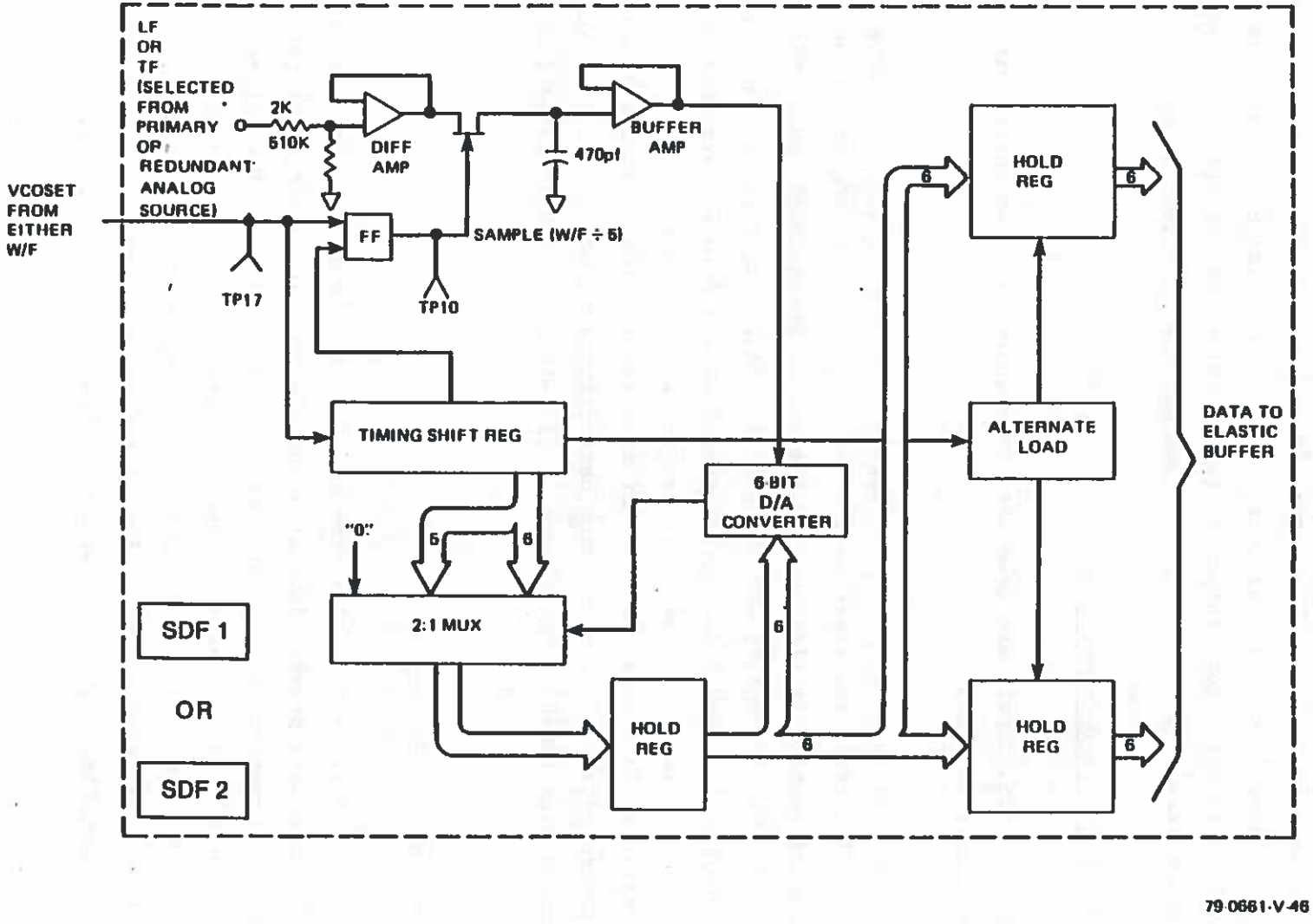


Figure 2.1.3.3-14. SDF A/D Converter

SDF Fine

For the transition from state $n_0 - 1$ to n_0

$$V_{input} = \frac{5.00 \text{ volts}}{63 \text{ steps}} (n_0 - 0.5)$$

For the middle of state n_0

$$V_{input} = \frac{5.00 \text{ volts}}{63 \text{ steps}} (n_0)$$

Figure 2.1.3.3-15. SDF A/D Transfer Functions

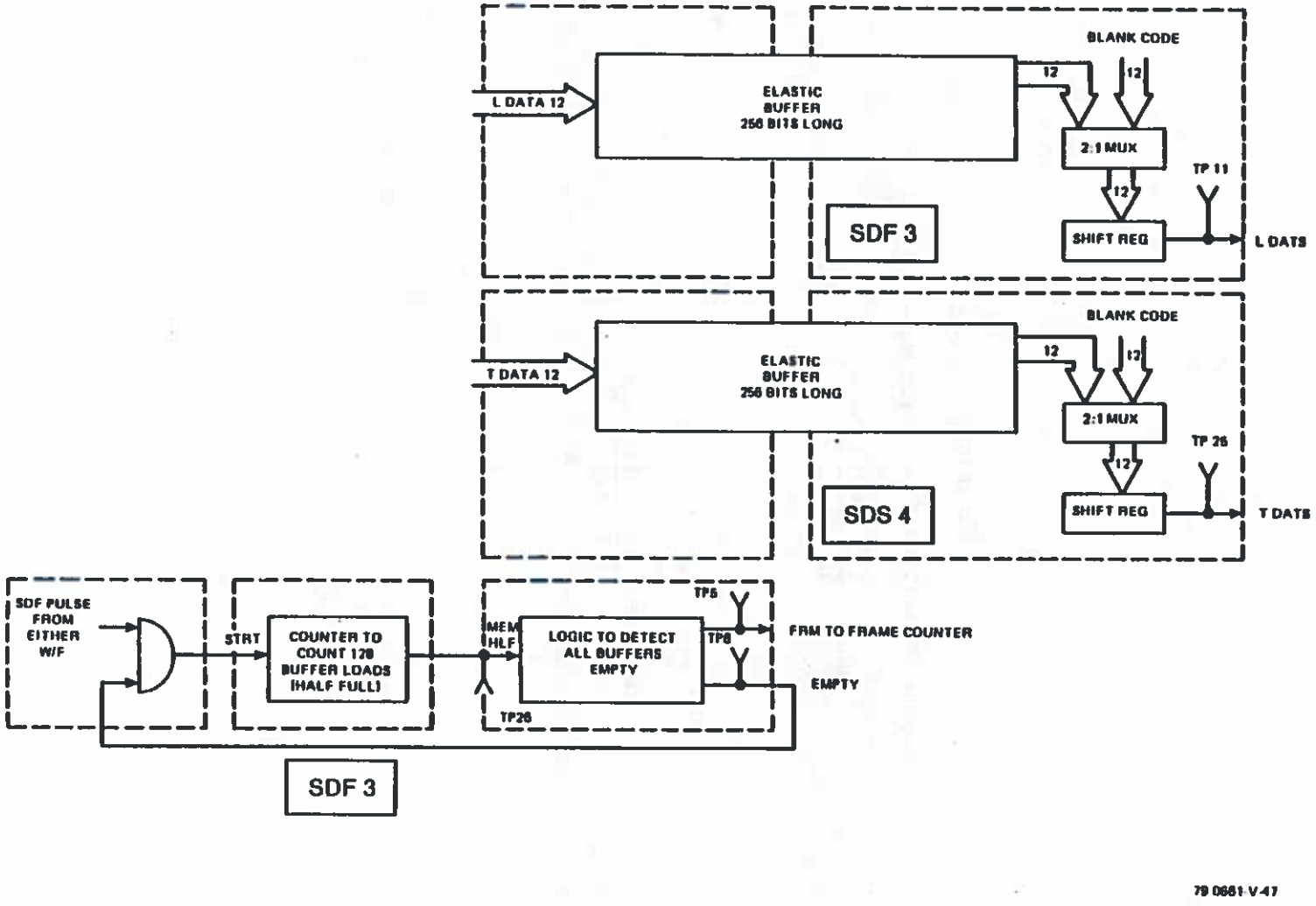


Figure 2.1.3.3-16. SDF Elastic Buffers

2.1.3.3.3.4 SDF Format Controls and Ancillary Data

The SDF frame has 208 bits, so a modulo 208 counter is used for format control. As stated in the paragraph above, the format controls and elastic buffers run together, with the formatter putting out a subsync frame, then video frames as long as video is available, then switching to line sync frames and blank frames at the end-of-scan region. (See figures 2.1.3.3-17, -18, -19.) Fixed Barker codes with tag bits unique to SDF are inserted into each L and T frame.

SDF has its own access to a fixed area of the Formatter Memory which contains ancillary data. The ancillary data includes present L channel and T channel gain states, T channel calibration values, PMT calibration value, vehicle I.D. and Location Data. Scanner offset information is output by the processor. Elapsed time data is read from the Elapsed Time Clock (in either I/O).

2.1.3.3.3.5 SDF Format Gating, Interleaving and Gapping

The various components of the L and T data streams are gated together, level shifted to TTL levels and the resulting 665.6 kHz streams are then either selected or interleaved, depending upon the desired mode. Interleaved data is at a 1331.2 kHz bit rate. A tape recorder test input is provided to allow a simple pattern to be recorded for bit-error rate checking at either 665.6 kHz or 1331.2 kHz. A test output is provided to allow the OLS Test Equipment to receive prerecorded data during ground testing. The tape recorders require a gap of 320 bit times following every 12,480 bits of data in order to keep internal synchronization. This gap is inserted by using an elastic buffer which receives continuous SDF data at its input, and puts out data at 40/39 of the input rate with a gap after every 12,480 bits. The 40/39 clock will come from either I/O. The data and sync signals out of the gapper are multiplexed to select SDF "G" or "H" and steered to the tape recorders by the Output Data Mux (see Figures 2.1.3.3-20 and 2.1.3.3-21.)

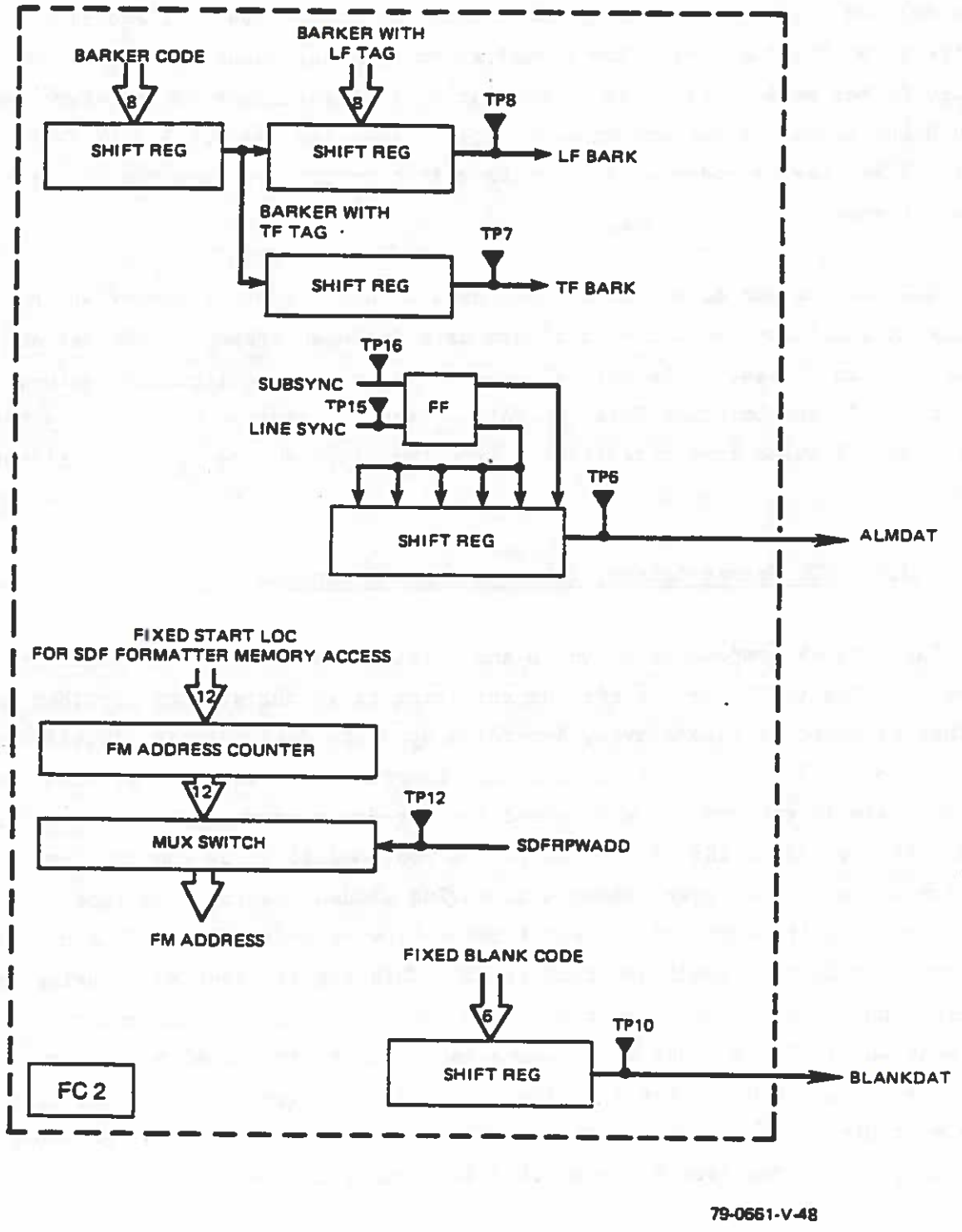


Figure 2.1.3.3-17. SDF Ancillary Data

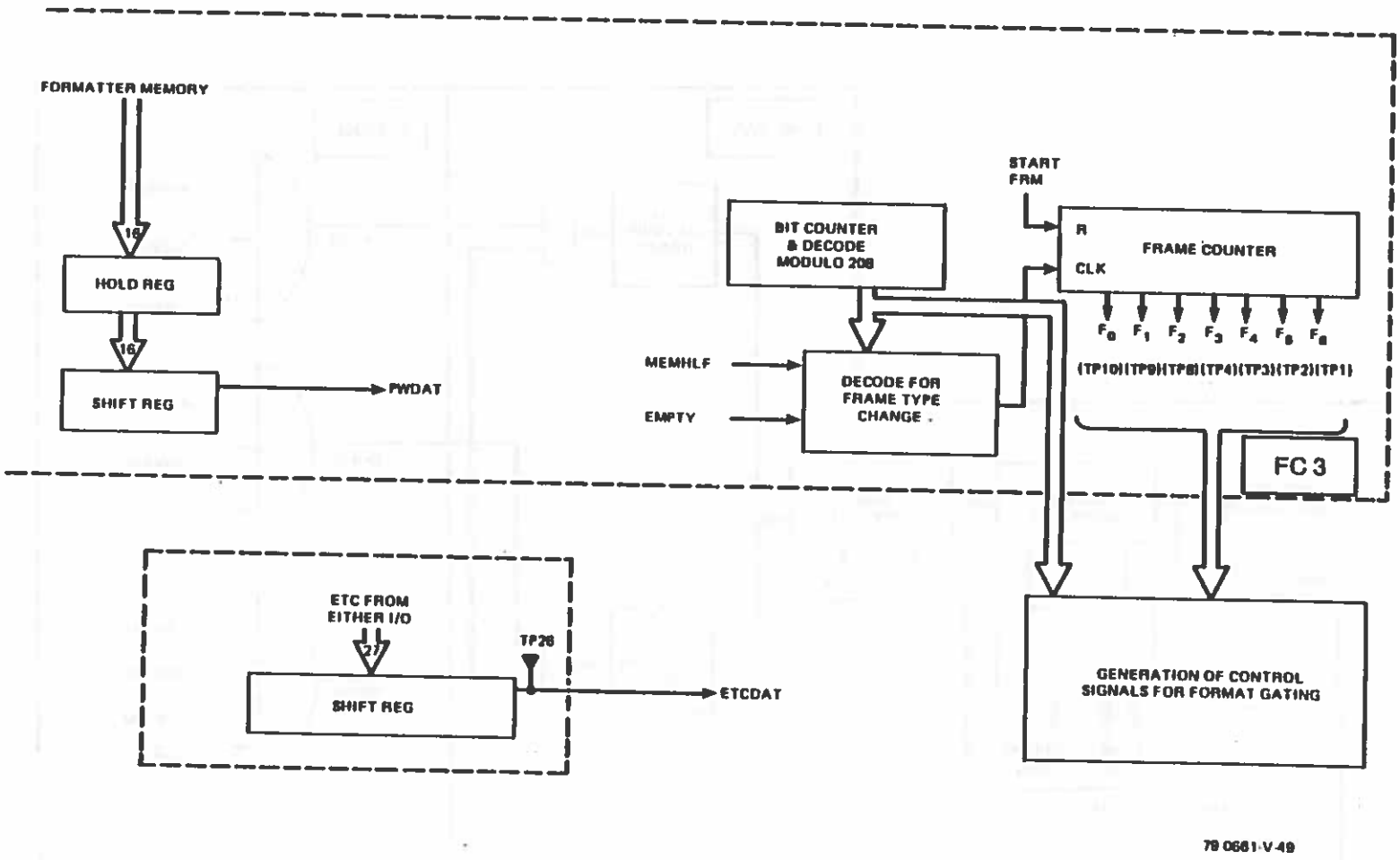


Figure 2.1.3.3-18. SDF Format Control and Ancillary Data

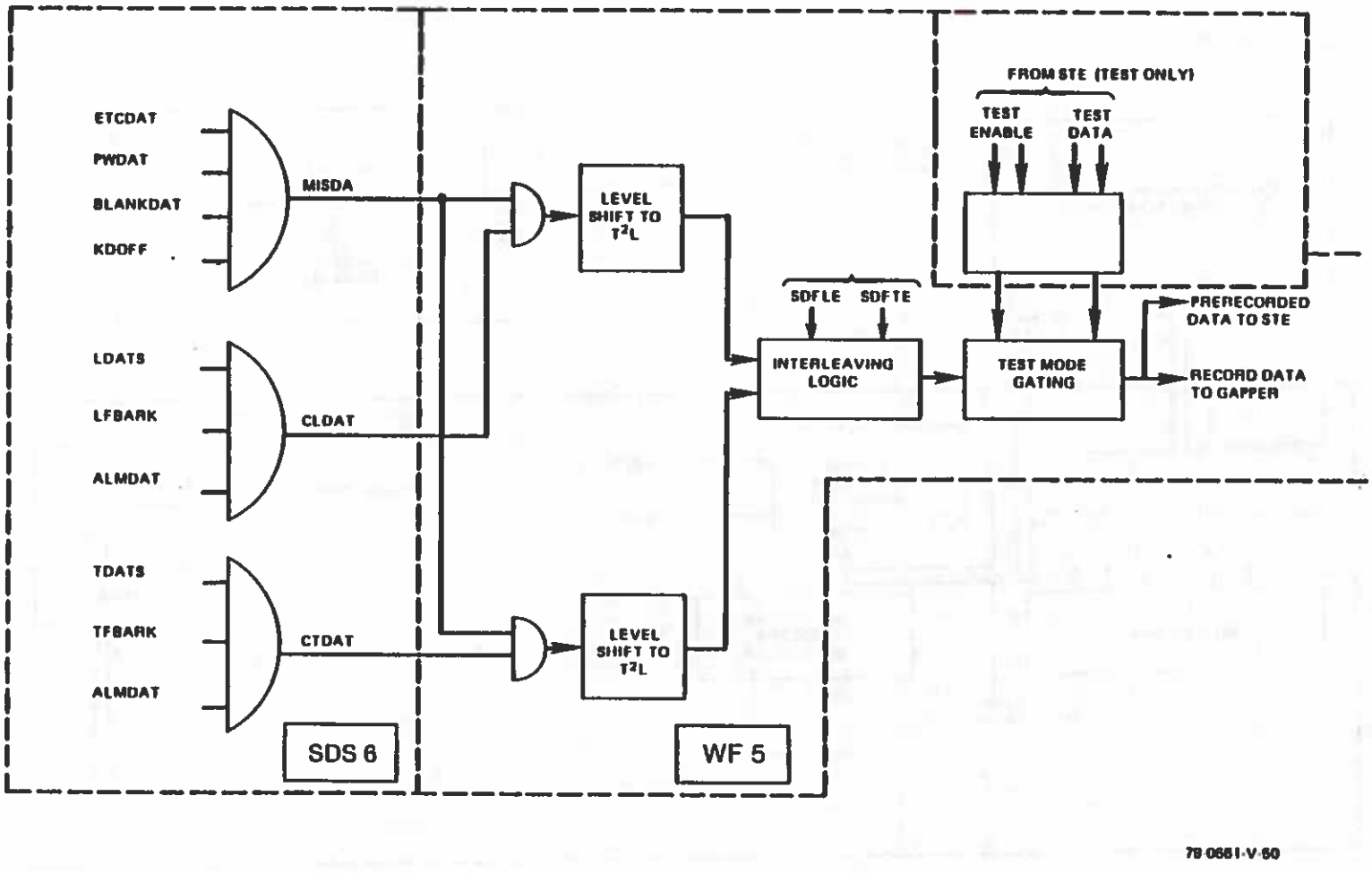
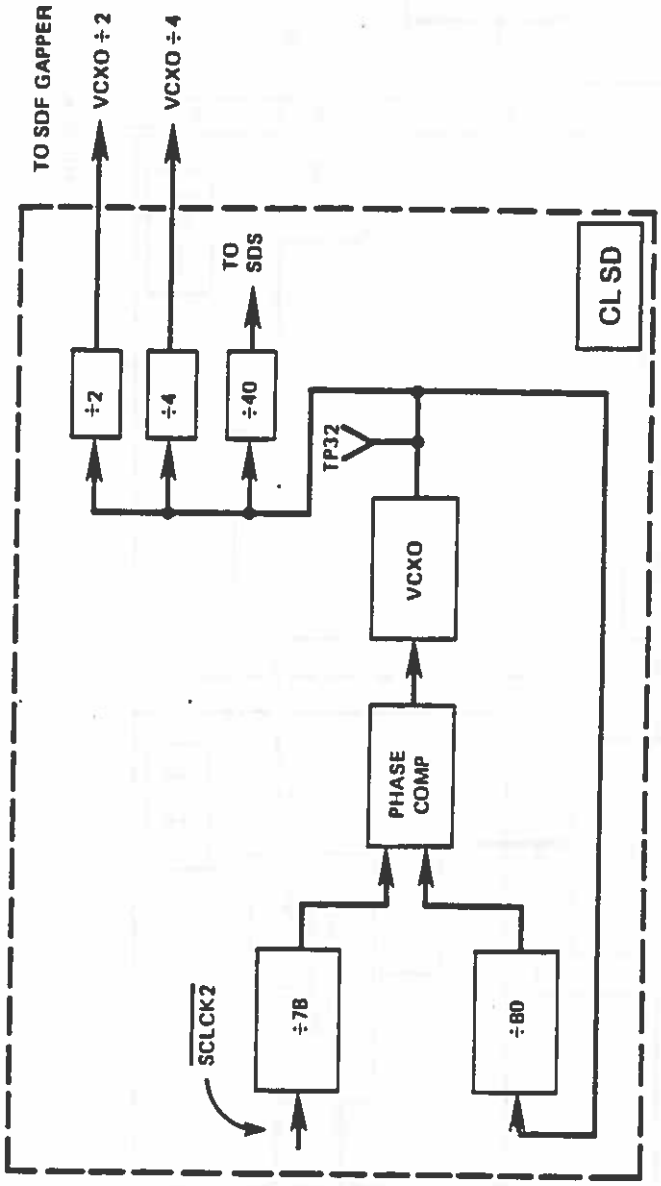


Figure 2.1.3.3-19. SDF Format Multiplexing



79-0661-V-51

Figure 2.1.3.3-20. Gapper VCXO

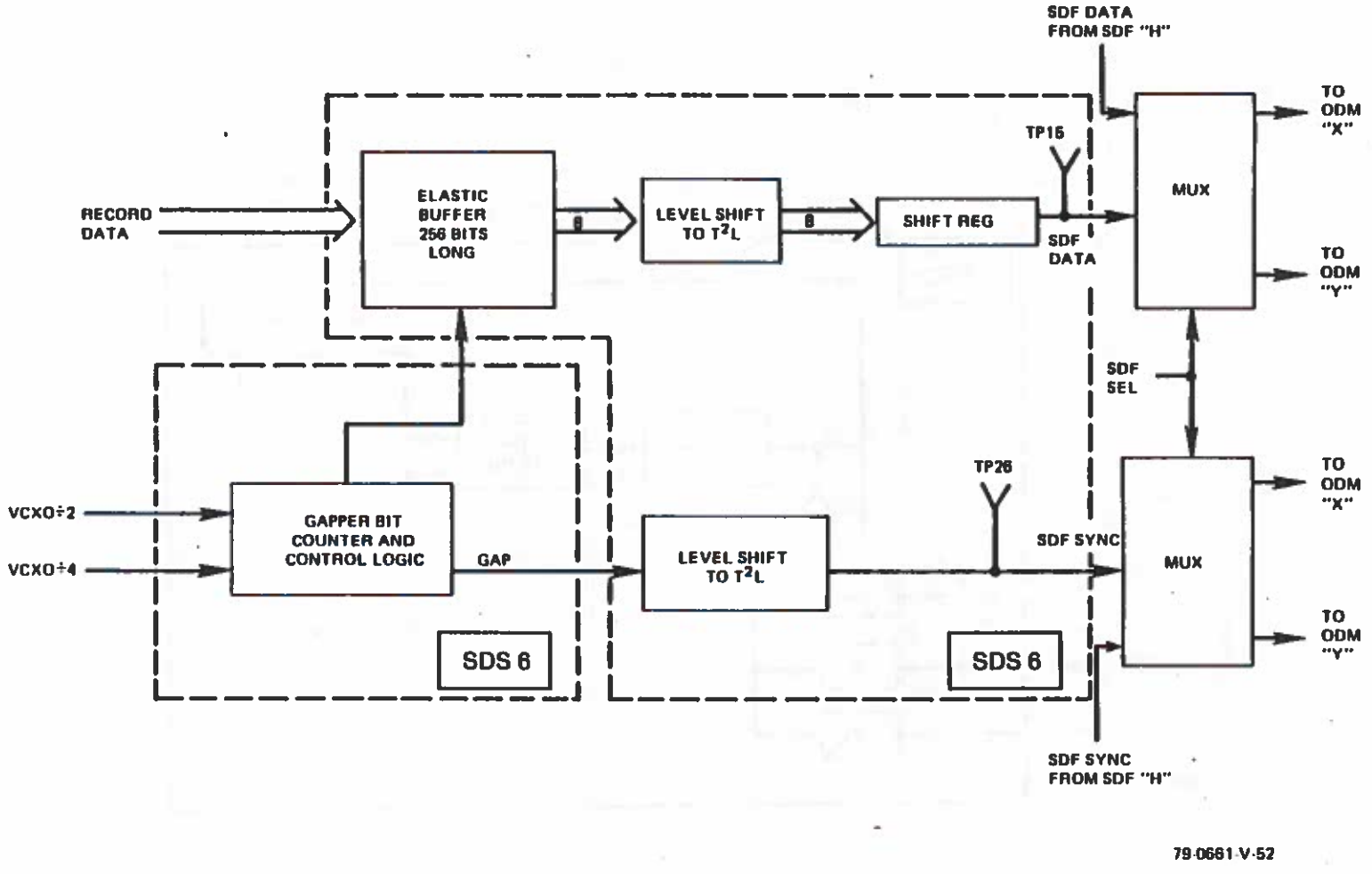


Figure 2.1.3.3-21. SDF Gapper

2.1.3.3.4 Stored Data Smoothed Processing (SDS)

The SDS processing function accepts both LS and TS analog inputs, samples the analog values at the proper wow/flutter clock rate, digitizes the sampled values, averages the sampled values along track for five scan lines, formats the averaged samples into LS and TS frame formats and formats the frames into LS and TS line formats. The SDS processing consists of a time-shared A/D converter followed by two parallel identical processors, one each for TS and LS, whose outputs are interleaved. Figure 2.1.3.3-22 shows the SDS processing function in block diagram form.

2.1.3.3.4.1 SDS Line Format

The SDS Video Frame format is 208 bits long and is subdivided into 28 words. This frame is repetitive and is output at a bit rate of 33.28 kHz. The SDS line format is shown in figure 2.1.3.3-23 with arrows indicating the direction of time for both record (AVE Time Scale) and playback (OGE Time Scale). Further details on the SDS formats can be found in the Data Specification (IS-YD-821).

SDS Video Frame is organized with words 1 through 27 containing 7 bits of smoothed video data. Word 27 contains mode tag bits and special sensor data while word 28 contains a frame sync. Each even bit in the 7-bit video data word is complemented. The T video word contains the 7 MSB's of the 8-bit T value. The L video word contains the 6 bit L value plus the LSB of the T value.

The SDS Line Sync Frame, SDS Subsync Frame, and SDS Blank Frame are used to provide synchronization, ancillary data, and fillers outside the region of active video data. The line format figure indicates the placement of the SDS Video Frames, the SDS Blank Frames, the SDS Telemetry/SSP Frames, the SSP Frames, the SDS Subsync Frame and the SDS Line Sync Frame.

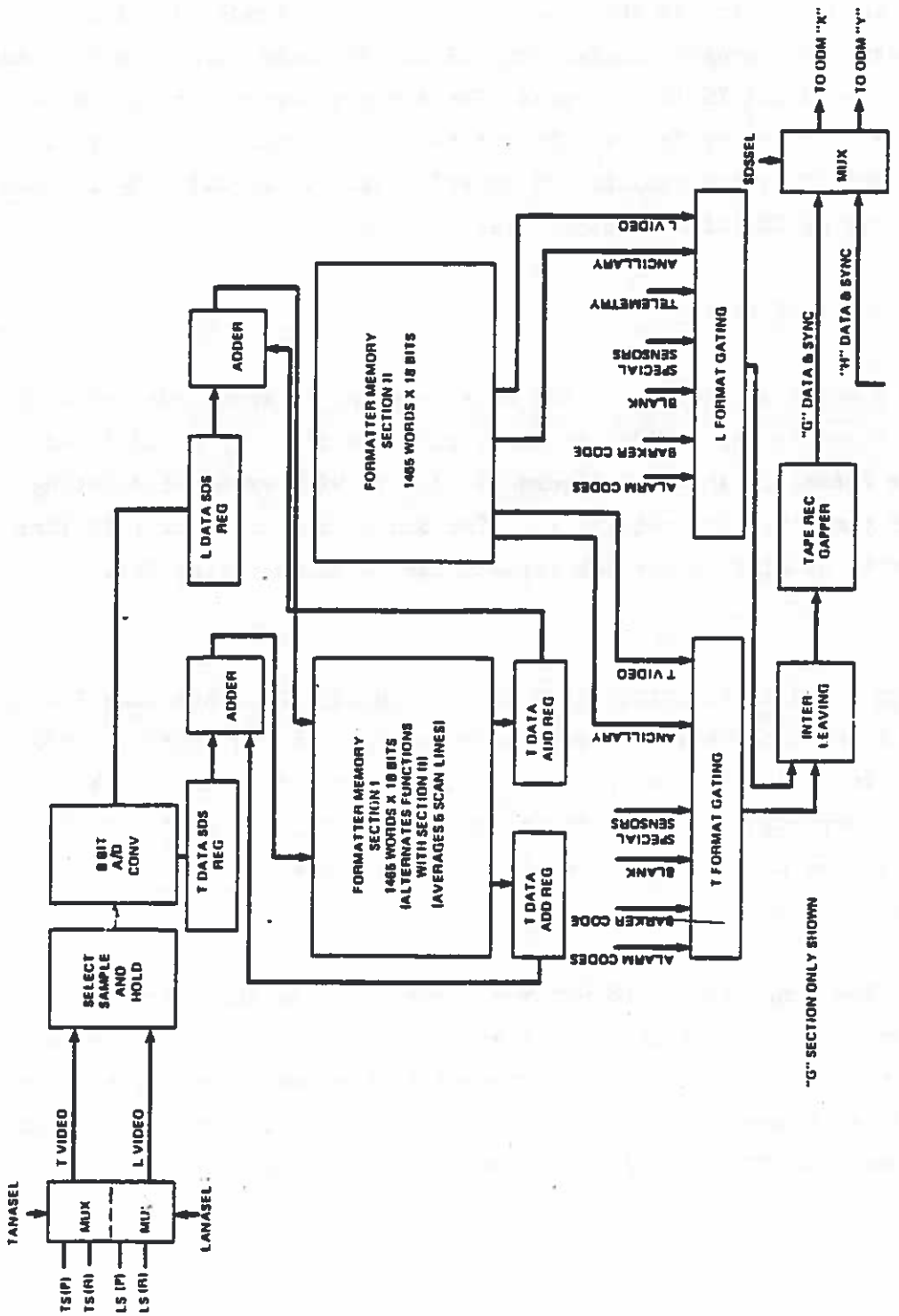
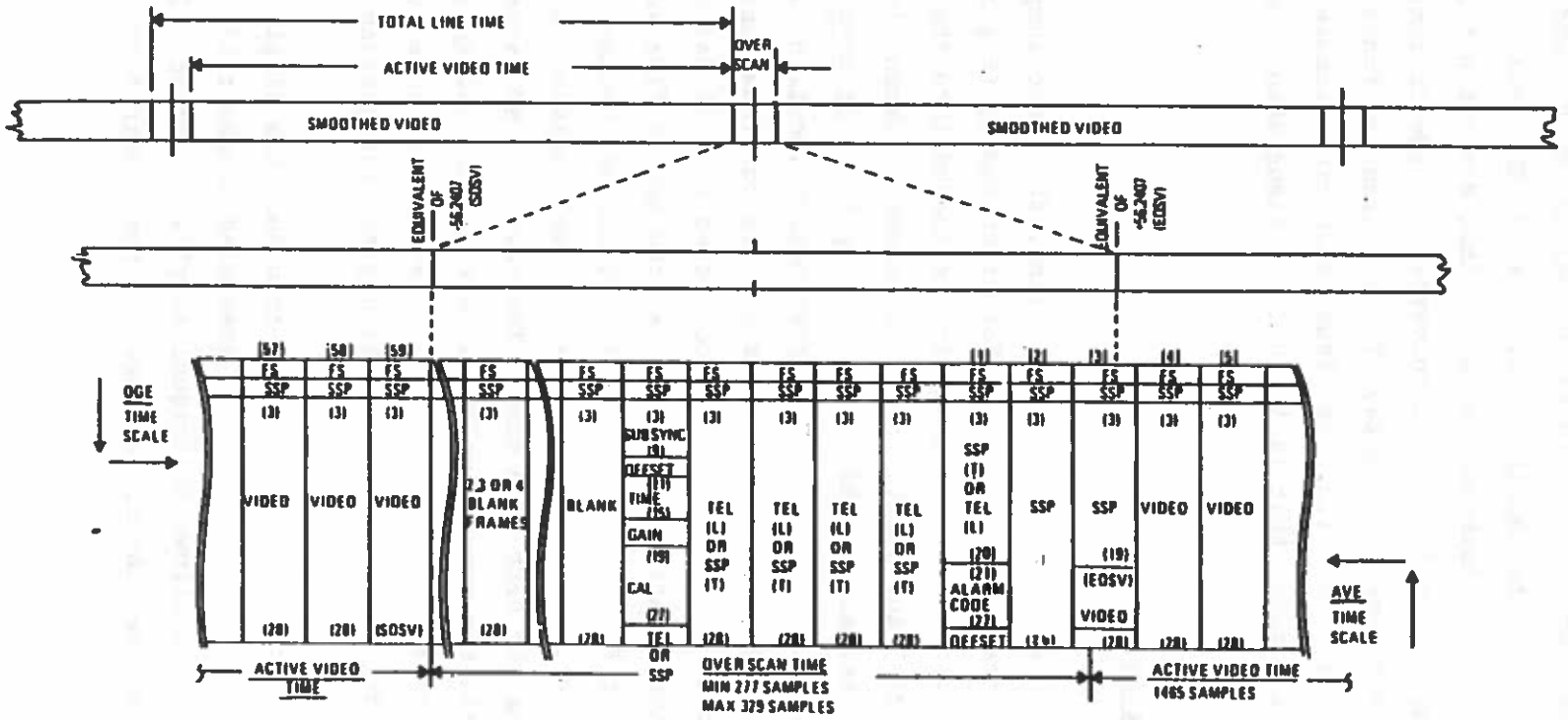


Figure 2.1.3.3-22. SDS Block Diagram



NOTES

1. (S) S = WORD NUMBER REFERRED TO FRAME SYNC USING OGE DATA TIMING
2. (SOSV) = START OF SMOOTHED VIDEO DATA SAMPLE OCCURRING AT +56.240?[0]
3. (EOSV) = END OF SMOOTHED VIDEO DATA SAMPLE OCCURRING AT +56.240?[0]
4. (F) = FRAME NUMBER REFERRED TO OGE DATA TIMING

TOTAL LINE TIME AT OUTPUT OF:	TIME (10^{-3} SEC)
SENSOR	84.175 ± 1.0%
AVE RATE BUFFER	420.875 ±
AVE TAPE RECORDER	10.522 ±
LONG LINE MODEM	10.522 ±
OGE D/A STORAGE	10.522 ±

ACTIVE VIDEO TIME AT OUTPUT OF:	TIME (10^{-3} SEC)
SENSOR	71.5056 ± 1.0%
AVE RATE BUFFER	
AVE TAPE RECORDER	
LONG LINE MODEM	8.7143 ±
OGE D/A STORAGE	8.7143 ± 0.01%

75-0561-VA-27-1

Figure 2.1.3.3-23. Stored Data Smoothed (SDS) Line Format

2.1.3.3.4.2 SDS A-to-D Converters

LS and TS video inputs are selected, independently, from the primary or redundant analog sources. The Smooth video (8 kHz bandwidth, both L and T) is sampled at a "wow/flutter + 25" rate (nominally 20.48 kHz). The position of the first sample is corrected in a fashion similar to that described for SDF. A single 8-bit successive approximation A-to-D converter is used to sample L and T video alternately (see figure 2.1.3.3-24). The A/D transfer functions are shown in Figures 2.1.3.3-25 and 2.1.3.3-26. Thus, each video sample at the SDS A/D converter represents a pixel that is 1.5 nmi (in along scan direction) by 0.3 nmi (in the along track direction.)

2.1.3.3.4.3 SDS Video Integration

On the first scan line in a group of five scan lines, the video samples are loaded directly into successive locations in Formatter Memory (Figure 2.1.3.3-24). A T sample and its associated L sample are loaded into the same 18-bit word, with 10 bits for T and 8 bits for L. On succeeding scan lines, the present video sample is serially added to the running total of previous samples taken at that angle (i.e., the same Formatter Memory location) and a new sum is loaded back into Formatter Memory. This process continues until 1465 samples of L video and of T video have been collected from 71.549 msec of active scan at a nominal sample rate of 20.48 kHz. At the end of five scan lines, that entire section of Formatter Memory (1465 locations) becomes available to the SDS Formatter, and a different set of 1465 location is used for video integration during the next five scans. The resulting SDS video values in the downlinked data represent pixels that are 1.5 nmi (along scan) by 1.5 nmi (along track), the along scan integration having been done by analog filtering and the along track integration by digital integration.

In order to use the full scale output of the 5-scan sum, the single scan line analog input corresponding to full scale is prescaled to about 4/5 of the available input range. This also allows individual samples to exceed full scale by 25% so that noise may be linearly averaged in the integration process.

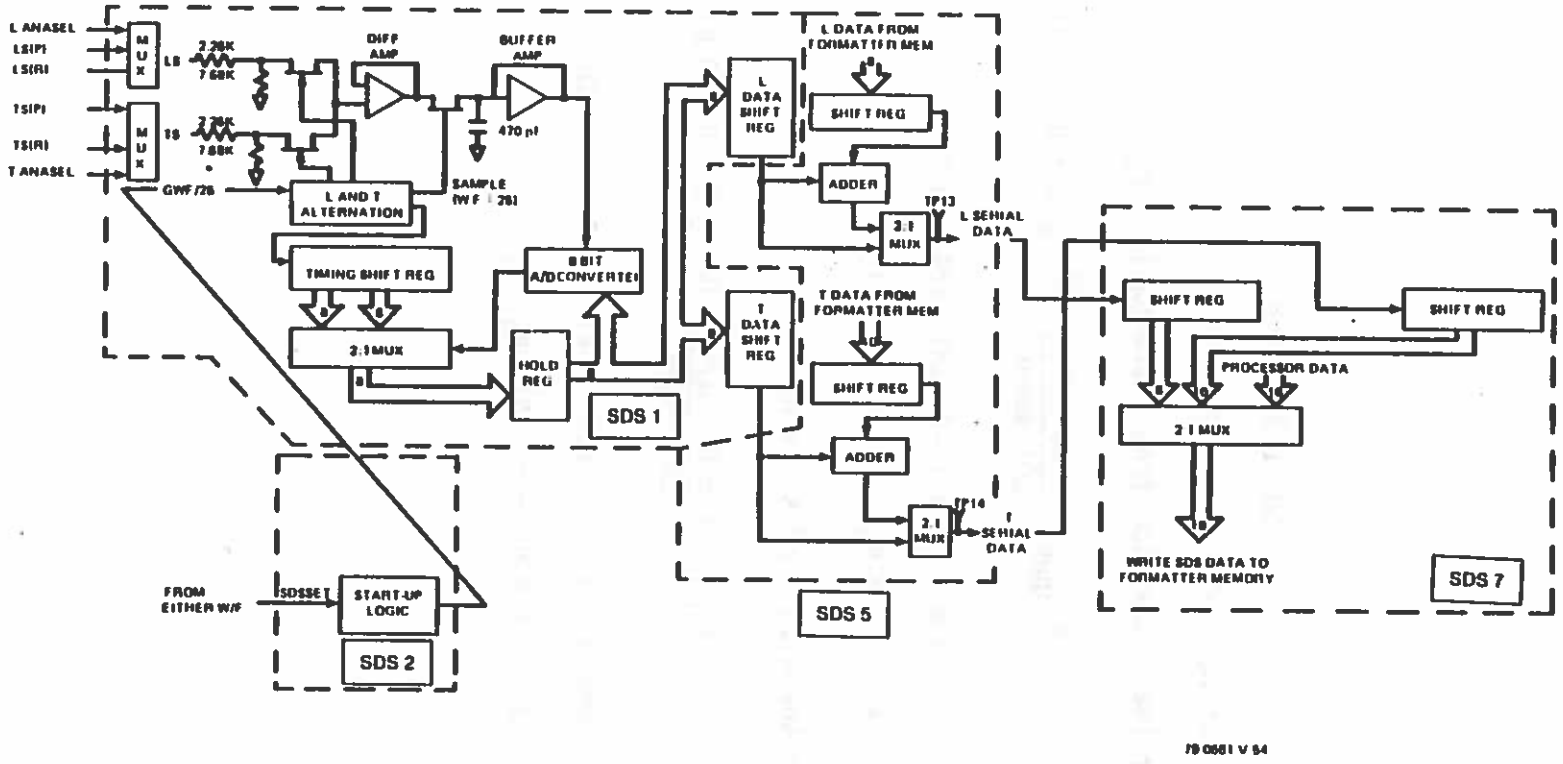


Figure 2.1.3.3-24. SDS A/D Converter and Adders

SDS L Smoothed

Output data state n_o = 0 to 63

For the transition from state n_o-1 to n_o

$$V_{input} = \frac{5.00 \text{ volts}}{204 \text{ steps}} (16\, n_o/5 + B - 0.8)$$

where B = (0.8 X -2) INT (X/4 + 0.8)

and X = n_o - 5 [INT (n_o/5)]

For the middle of state n_o

$$V_{input} = \frac{5.00 \text{ volts}}{204 \text{ steps}} (16\, n_o/5 + B - 0.8)$$

where B = 2.6 + 0.8 (X-2) - INT (X/3 + 0.8)

and X = n_o - 5 [INT (n_o/5)]

Figure 2.1.3.3-25. SDS L Transfer Functions

SDS T Smoothed

Output data state n_o = 0 to 255

For the transition from state n_o-1 to n_o

$$V_{input} = \frac{5.00 \text{ volts}}{204 \text{ steps}} (\text{INT } [0.8(n_o+1)] - 0.8)$$

Exclude values of n_o where $(n_o + 1)$ is a multiple of five.

For the middle of state n_o

$$V_{input} = \frac{5.00 \text{ volts}}{204 \text{ steps}} (\text{INT } [0.8 (n_o + 1)] - 0.3)$$

Exclude values of n_o where $(n_o + 1)$ is a multiple of five.

Figure 2.1.3.3-26. SDS T Transfer Functions

2.1.3.3.4.4 SDS Format Controls and Ancillary Data

The SDS frame contains 208 bits, so a modulo 208 counter is used to control the formatting (figures 2.1.3.3-27 and 2.1.3.3-28). The video samples are read out of the appropriate half of Formatter Memory. Ancillary Stored and Telemetry data is read out of a fixed area in Formatter Memory. The stored telemetry data was received from the spacecraft and buffered by the processor and formatter memory as described in paragraph 2.1.3.2.2.5. Fixed Barker codes with tags, blank codes, alarm codes and subsync codes are formatted and inserted in the data stream where required. Offset data and Elapsed Time data is also put into the data stream. The formatter requests Special Sensor data from the SSP as required for insertion into the format. A line of formatted SDS data requires five scan lines to output, since its video data represents an integration of video samples over the previous five scan lines.

2.1.3.3.4.5 SDS Format Gating, Interleaving and Gapping

The various components of the L and T data streams are gated together and the resulting 33 kHz data streams are interleaved to give a 66.56 kHz data stream (Figures 2.1.3.3-29 and 2.1.3.3-30). A tap is provided to allow the OLS Test Equipment to receive prerecorded data in ground test. A gapper similar to the SDF Gapper is provided for the data going on to the tape recorders by way of the Output Data Multiplexer.

2.1.3.3.5 Special Sensor processing

The Special Sensor Processing section consists of a 1024 word by 16-bit RAM memory, special sensor control circuitry, and circuitry for inserting special sensor data into RTD and SDS data streams. There are two fully redundant SSP sections (see figures 2.1.3.3-31, -32, -33, 34).

2.1.3.3.5.1 Special Sensor Memory

The CMOS Random Access memory used for Special Sensor processing is divided into two identical 512 word by 16-bit halves. One half is used for

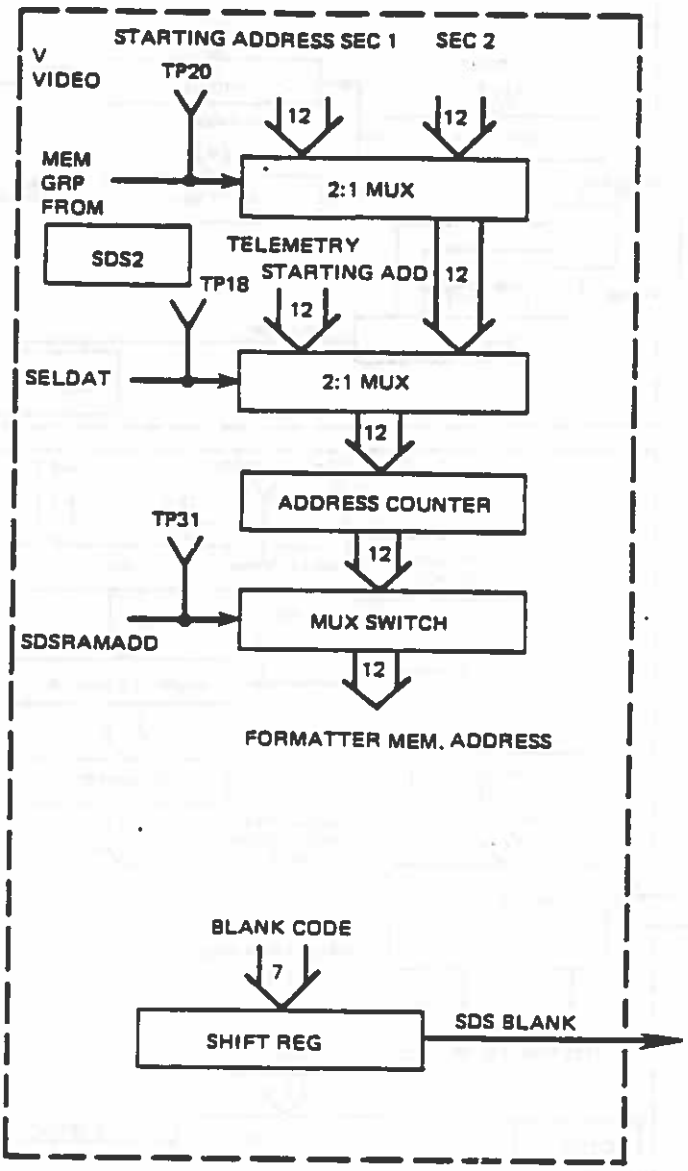


Figure 2.1.3.3-27. SDS Formatter Memory Addressing

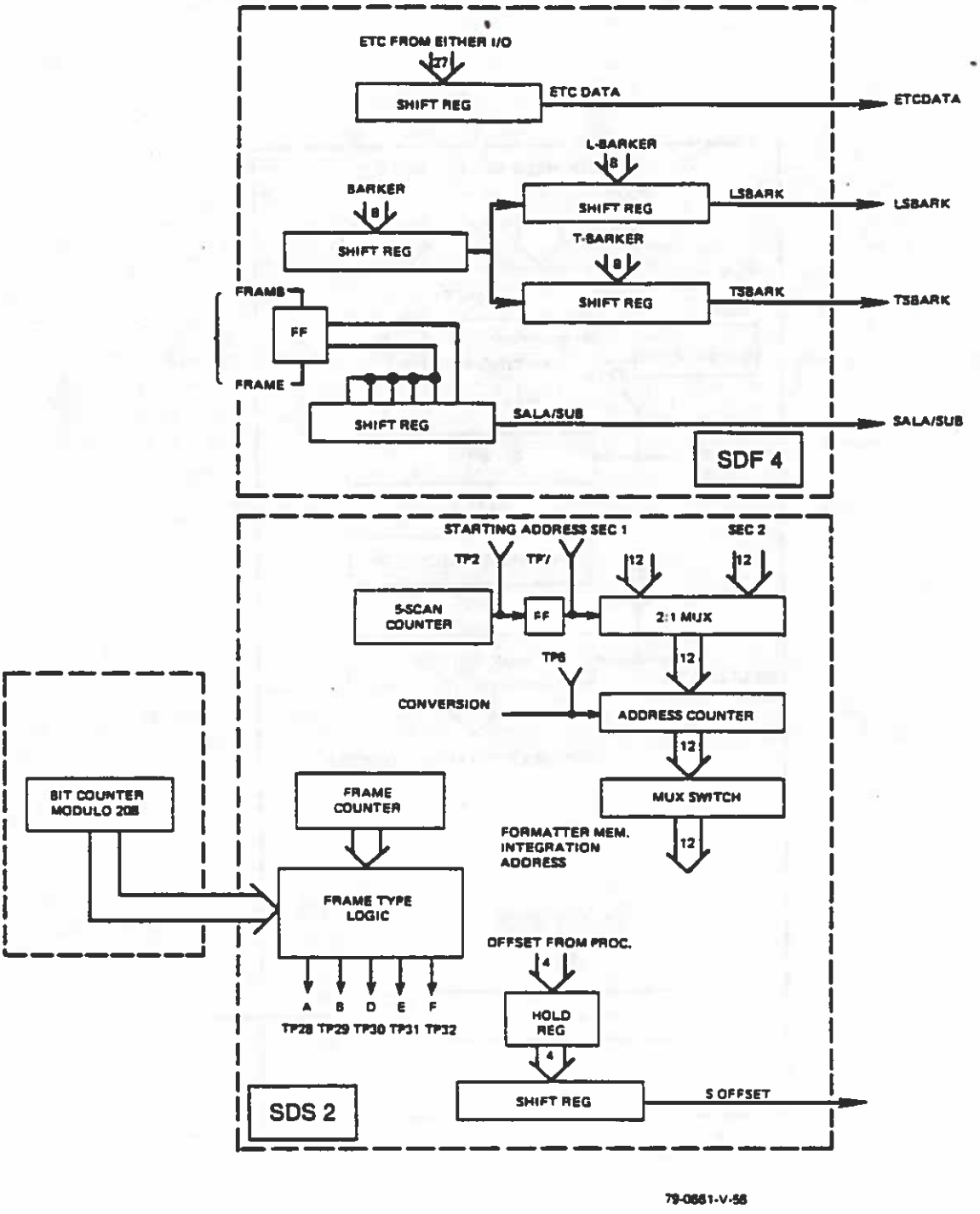


Figure 2.1.3.3-28. SDS Format Controls

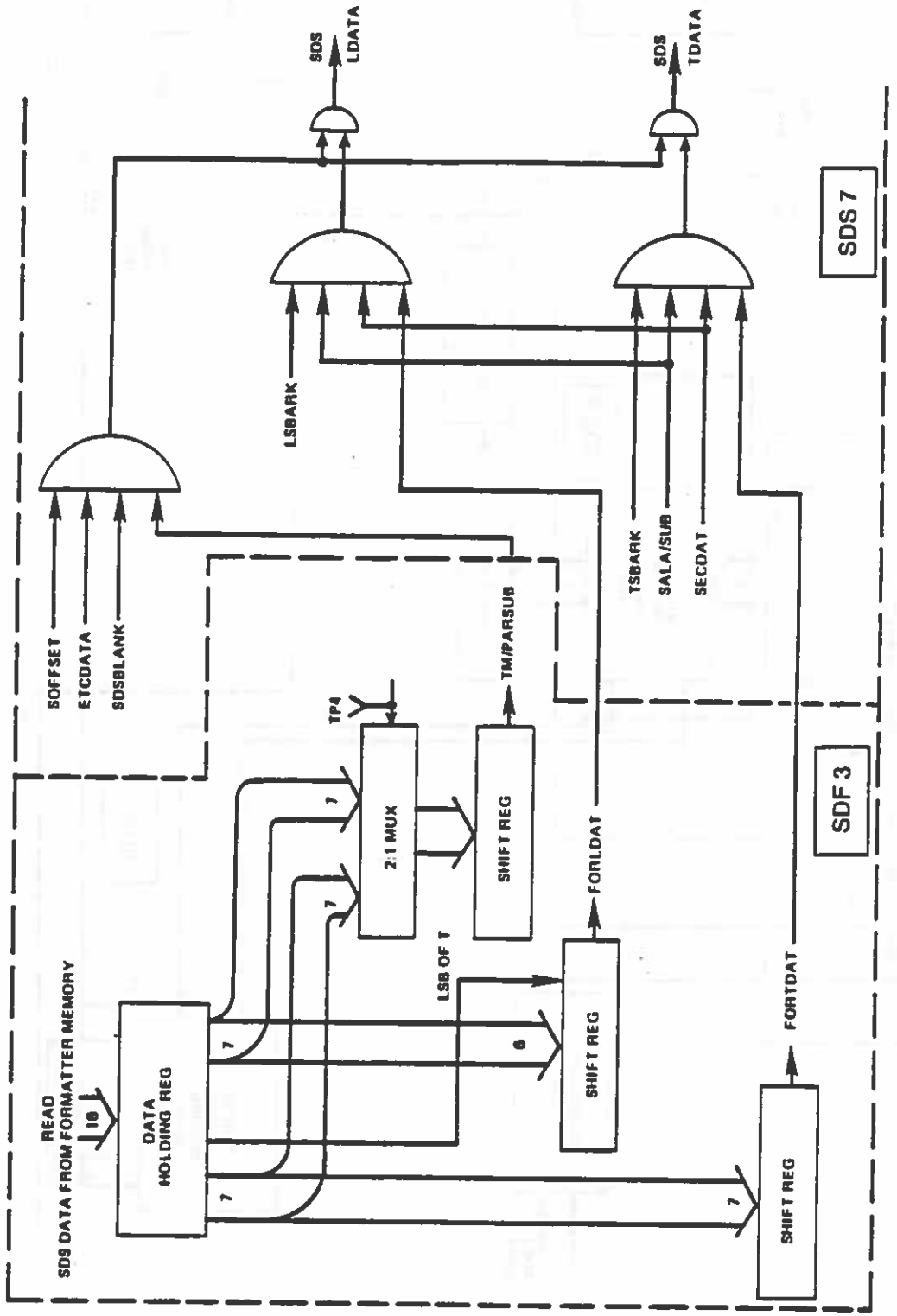


Figure 2.1.3.3-29. SDS Format Gating

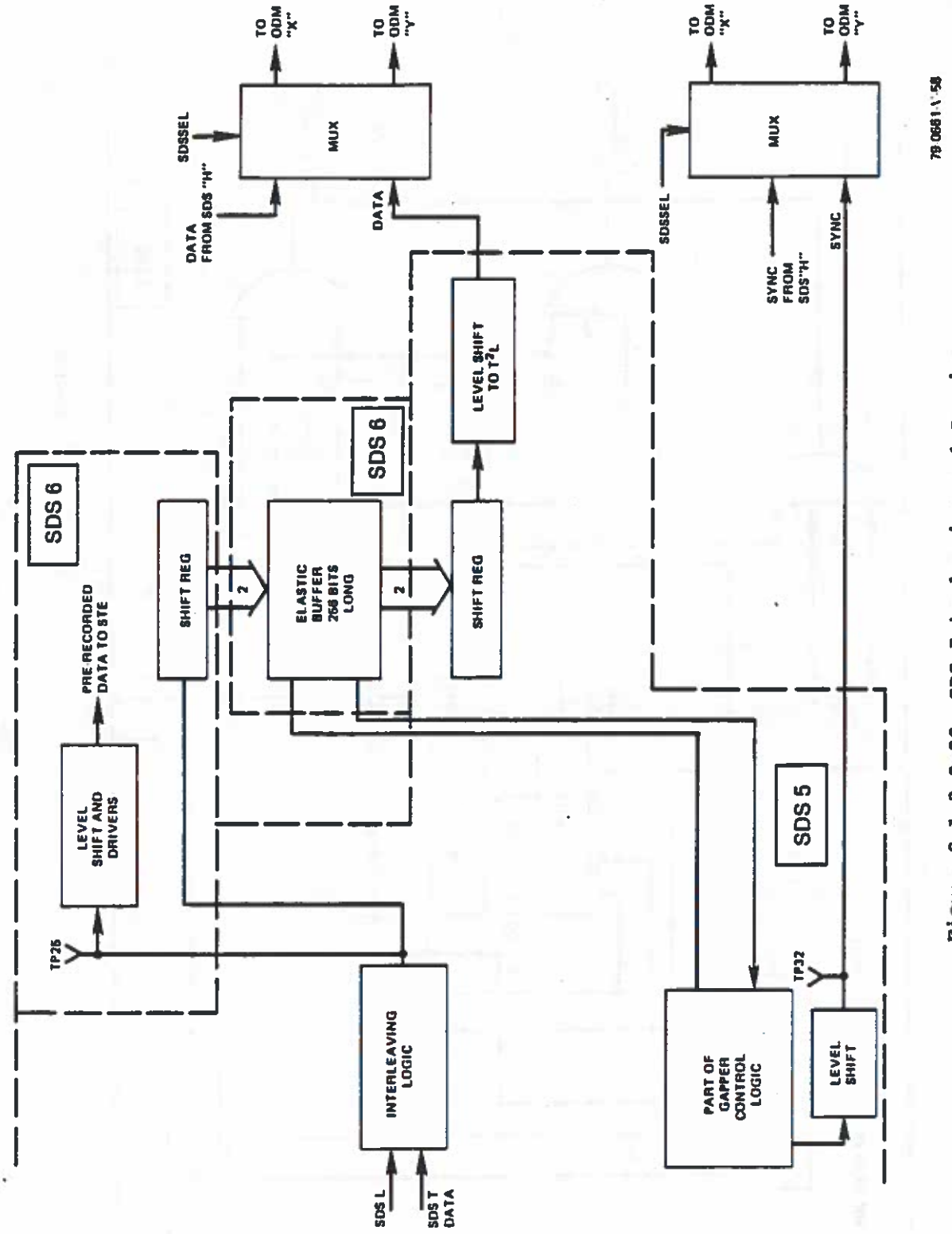
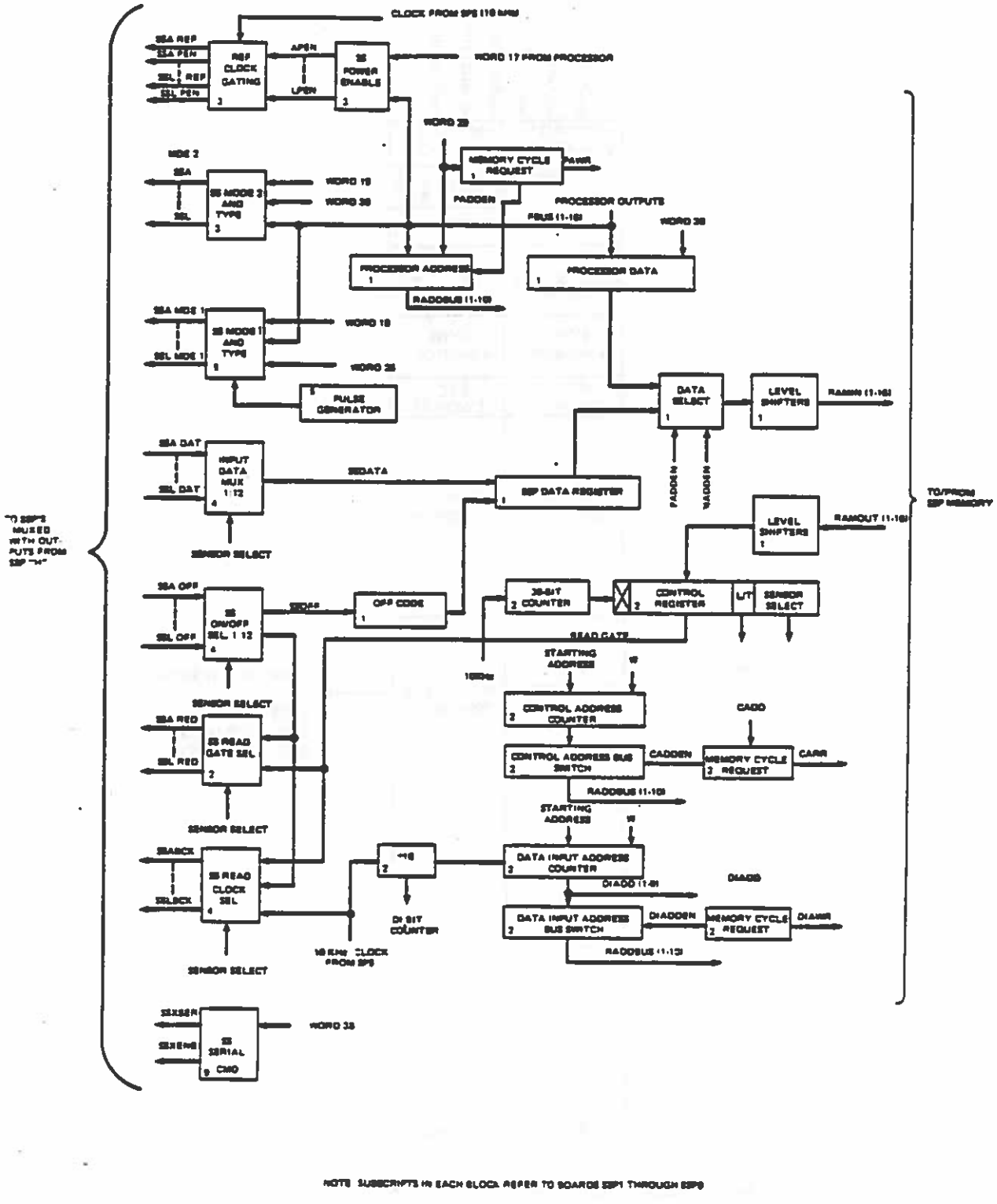


Figure 2.1.3.3-30. SDS Interleaving and Gapping



NOTE: SUBSCRIPTS IN EACH BLOCK REFER TO BOARDS SSP1 THROUGH SSP8

79-0061-V-4B

Figure 2.1.3.3-31. SSP Interface Hardware

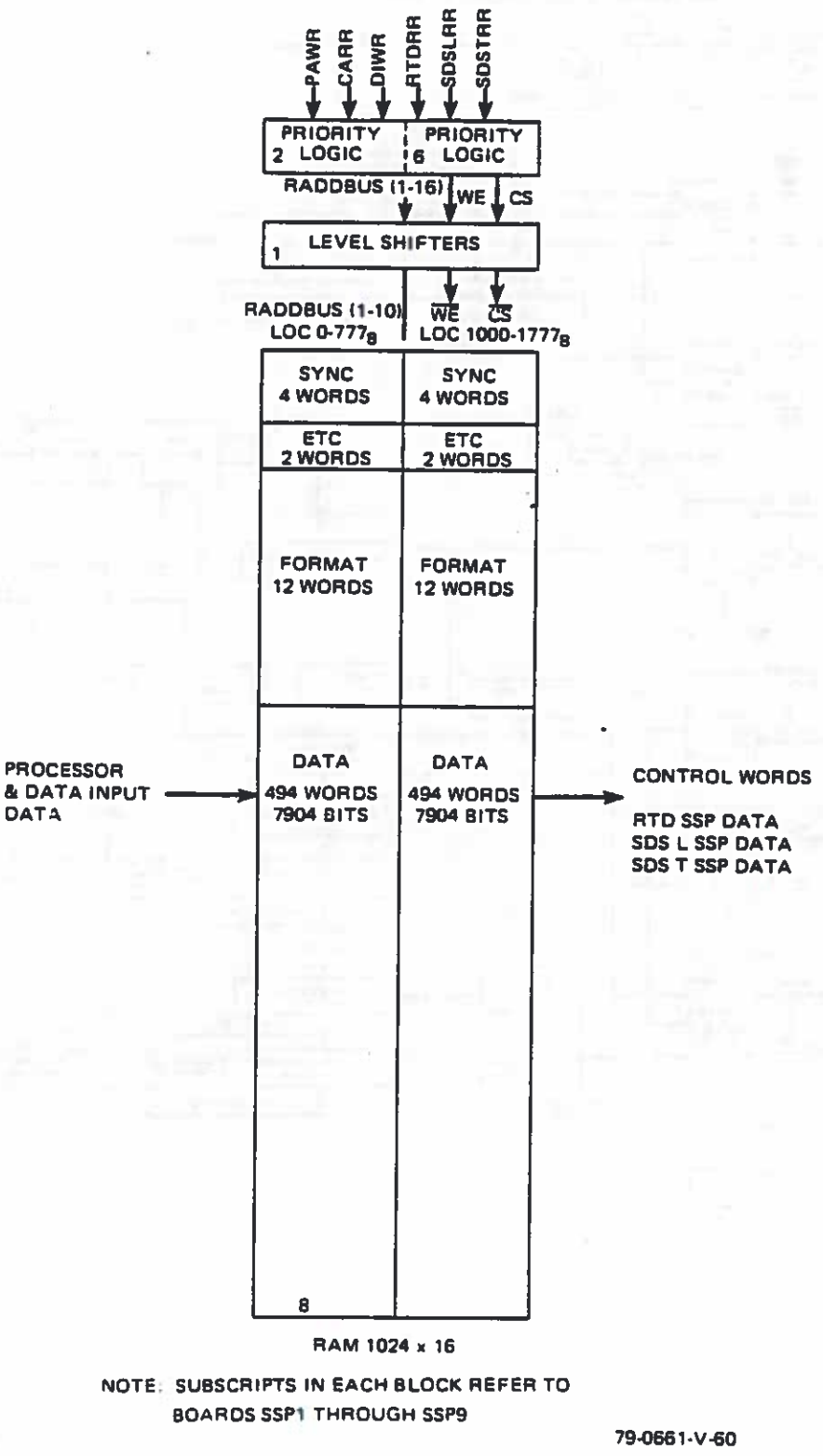


Figure 2.1.3.3-32. SSP Memory

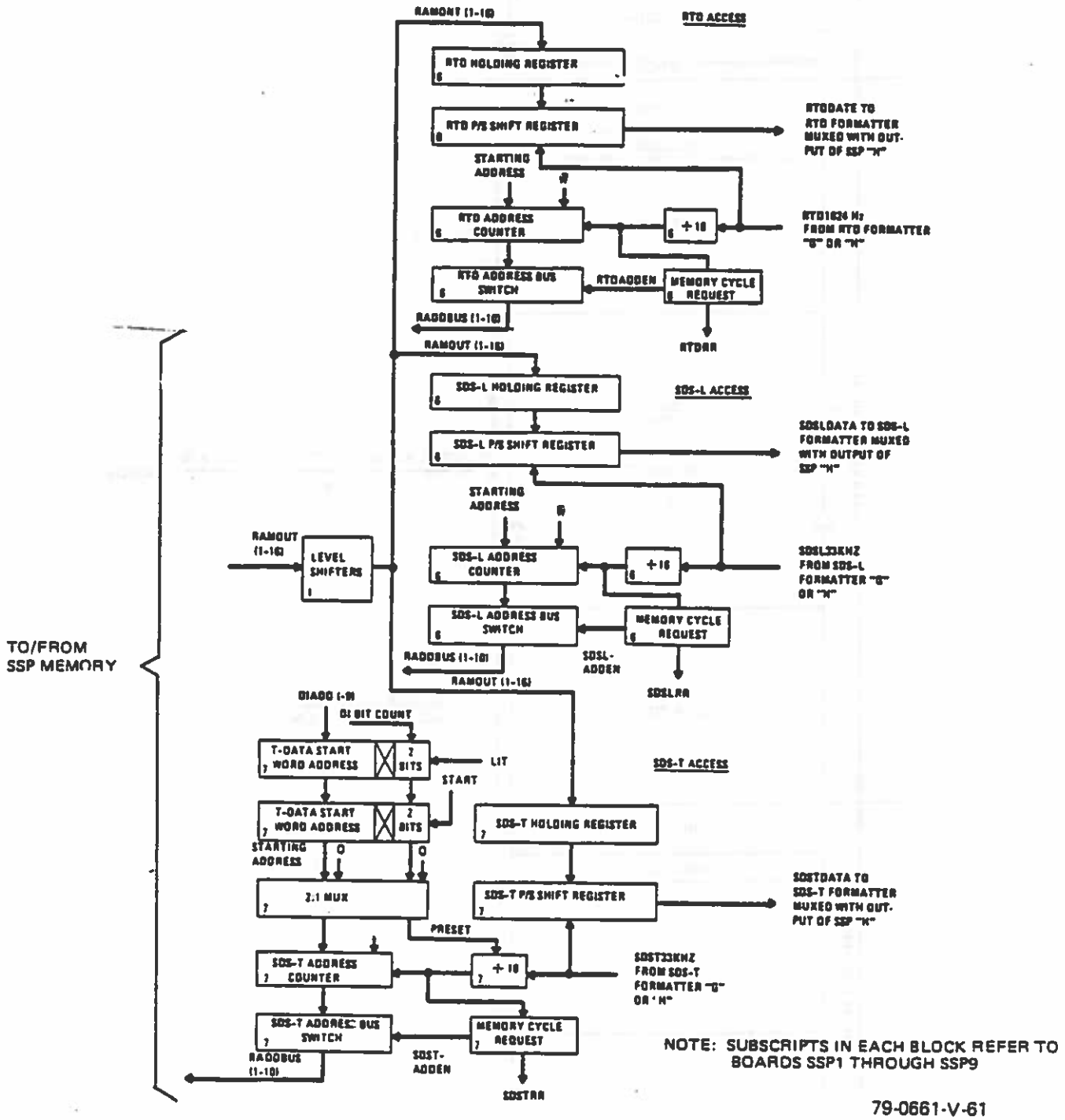


Figure 2.1.3.3-33. SSP Output Data to Formatters

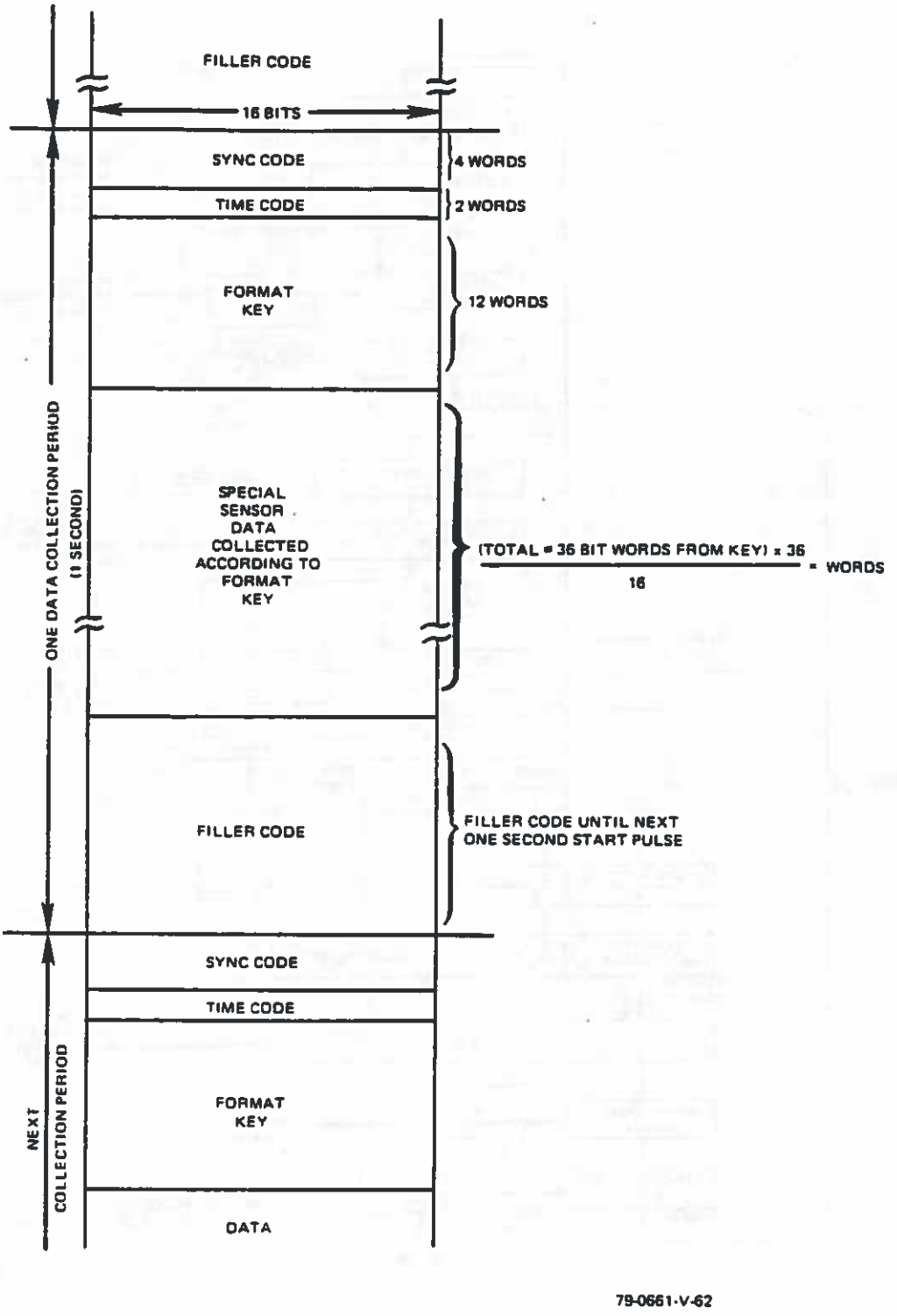


Figure 2.1.3.3-34. SSP Format

sensor control and inputting of SSP data while the other half is being read out by the formatters. The functions of the two halves are swapped once per second. There is priority logic to order the various memory accesses which are taking place independently and simultaneously. When a mode requiring SSP data (e.g., RTD or SDS) is turned on, the processor outputs 4 words of sync code, 2 words of Elapsed Time Count and 12 words of Special Sensor Formats to each half of SSP memory. This information is used to control the special sensor interrogation for that second, and then appears at the beginning of the SSP data stream to the formatters in the following second, followed by the special sensor data. The processor outputs ETC and a "start" bit every second to control the swapping of the SSP memory halves.

2.1.3.3.5.2 Special Sensor Control

Special Sensor Power Enable, Mode changes and serial commands are generated from either real time or stored commands. The 10 kHz reference clock is sent to all sensors whose power is enabled. The SSP control logic steps through the format words in the SSP memory and sends the Read Gate and Read Clock to the appropriate sensor for the correct number of bit times. The format word indicates the sensor to be interrogated, whether its data is to appear in the SDS-L stream or T-stream, and the number of 36-bit words of data to be received from the sensor. As the data is received serially from the sensor it is loaded sequentially into the memory. If a sensor indicates that is in an "off" state, a special 36-bit filler word is loaded into the memory in place of each data word. After all of the sensors indicated in the format words have been interrogated, the remainder of the memory is filled with the same 36-bit filler words.

2.1.3.3.5.3 Formatter SSP Access

RTD Access. - The RTD formatter provides a 1024 kHz serial clock during those periods when SSP data is to be inserted into the RTD data stream. The contents of the SSP RAM are read out sequentially, beginning with the sync code, followed by the ETC, the format words, the SSP data and filler words as required to fill out the rest of the one second period.

SDS-L Access. - The SDS-L access is similar to the RTD access, except that the clock rate is only 33 kHz. The data is read out sequentially following the format codes, and since sensors assigned to SDS-L will be interrogated first, all of their data will appear, followed by as much SDS-T data and/or "filler words" as required to fill out the rest of the 1-second period.

SDS-T Access. The SDS-T access is more complicated, since it is desired to skip over the SDS-L data following the format words, and put out only data from the sensors assigned to SDS-T. The circuitry must record the word and bit within the memory where the SDS-T data started, since this point depends on the format information. Aside from this variable starting point of the data, the SDS-T access is similar to the SDS-L access.

2.1.3.3.5.4 Special Sensor Setup

Either during the memory load process or by loading page zero of Uplink Memory, location 037_8 should be loaded with the pulse or level type information for the SSP "Mode one" lines and location 040_8 should be loaded with the pulse or level information of the "Mode two" lines. Page 0 location $041\text{-}054_8$ should be loaded with the number of thirty-six bit words to be sampled, whether they are in the SDS-L data format or the SDS-T data format and the order that the sensors are to be sampled. Location 041_8 contains the information about the first sensor to be sampled. The contents of locations 041 through 054 must be such that all of the sensors to be included in the SDS-L format are sampled before any sensors are sampled for the SDS-T format. All of the sensors with zero word counts must be together and must be the last sensors sampled.

When RTD or SDS are being formatted, and until RTD and SDS are turned off, SSP formatted data will appear on the SDS or RTD data streams with the format specified by the contents of the uplink memory. In RTD the first bit received after the header information is the first bit received from the first sensor sampled. SDS prerecord data has the same SSP bit order as RTD. The OLS tape recorders reverse this order for downlink data.

The SDS L data format contains 18, 16-bit header words and at least 50, 36-bit data words. The SDS T data format contains 18, 16-bit header words and at least 98, 36-bit data words. The RTD data format contains 18, 16-bit header

words and at least 139, 36-bit data words. In each of the formats specific bits are dedicated to special sensor data. In ground processing these bits are extracted from serial data and the SSP synchronization pattern located which defines the start of an SSP one second frame. Further details of SSP formats are in the Data Specification (ID-YD-821).

2.1.4 Power Supply System

The function of the OLS power supply is efficient, reliable level shifting of the spacecraft bus dc prime power voltages to the various voltages required by OLS. This level shifting is accomplished while maintaining the required bidirectional noise, ripple and ground isolation between the spacecraft bus and the output loads. To achieve high efficiency and reliability, a simple, conventional design mechanization with modular redundancy is used.

The OLS power supply system is considered in the subsections which follow as consisting of functionally four parts:

Main Power Supply - converts the +28V dc spacecraft source to most of the regulated and unregulated dc voltages used in the OLS. This supply is made up of two supplies each capable of powering the OLS, to provide redundancy.

High Voltage Power Supply - converts main power supply outputs to the high voltage dc required to power the photomultiplier tube (PMT).

+5 Voltage Spacecraft Conditioning - provides +5V dc to interface circuits that must be powered whether the OLS is on or off.

T Cone Heaters - provides +28V dc from the spacecraft bus to warm the T channel cone cooler upon command.

2.1.4.1 Main Power Supply

The main power supply consists essentially of two identical redundant power supplies. At the dual supply outputs, full cross-strapping between the loads and the redundant supplies is provided by latching relays with low ON resistance, high OFF resistance, and low standby power. The ON/OFF status of the individual supplies and the cross-strapping is directly controllable through S/C interface signals.

Figure 2.1.4-1 is a simplified block diagram of the OLS main power supply. Figure 2.1.4-2 is a detailed block diagram of the OLS power distribution system showing the sources of power supply system EST voltages.

The primary functional blocks in the dual power supply channels shown on Figure 2.1.4-1 are:

Fuse - rated at 7 amperes to provide decoupling of a faulted supply from the prime power bus.

DC to DC Converter - consisting of the following:

Line Filter - a pi-section to provide ripple isolation.

Inverter - a two-transistor, high efficiency, 150 watt, 25 kHz, dc to ac inverter.

Transformer - a centertapped primary, multiple centertapped secondaries transformer which provides the isolation of S/C return from signal ground.

Rectifier/Filters - provides 6 full wave rectified Vdc outputs, each with an L-C lowpass filter. These five outputs are: +20, +13.6; +6.6, (-)13.8, and (-)20 volts.

Regulators - conventional, series-regulated, current limited power supplies to provide low ripple, low source resistance outputs. The regulated voltages provided are:

+5.3V (D) to digital users
+12.0V (A) to nonpulsating analog and digital users
+12.0V (D) to digital users
-12.0V (A) to both analog and digital users
+12.0V (M) The only nonredundant power supply regulator is backed up by both the +12V $(D)_1$ and the +12V $(D)_2$ regulators by means of diode or-gating their outputs to +12V(M).

The +12V (M) supply, whose unregulated input voltage is obtained by diode or-gating voltages from both sides, provides an "unswitched" voltage to the ENPA, to the Drive Motor Electronics, and to the digital chips that do the signal cross-strapping between the primary and redundant digital blocks. These interfaced chips must be powered ON when either digital block is ON.

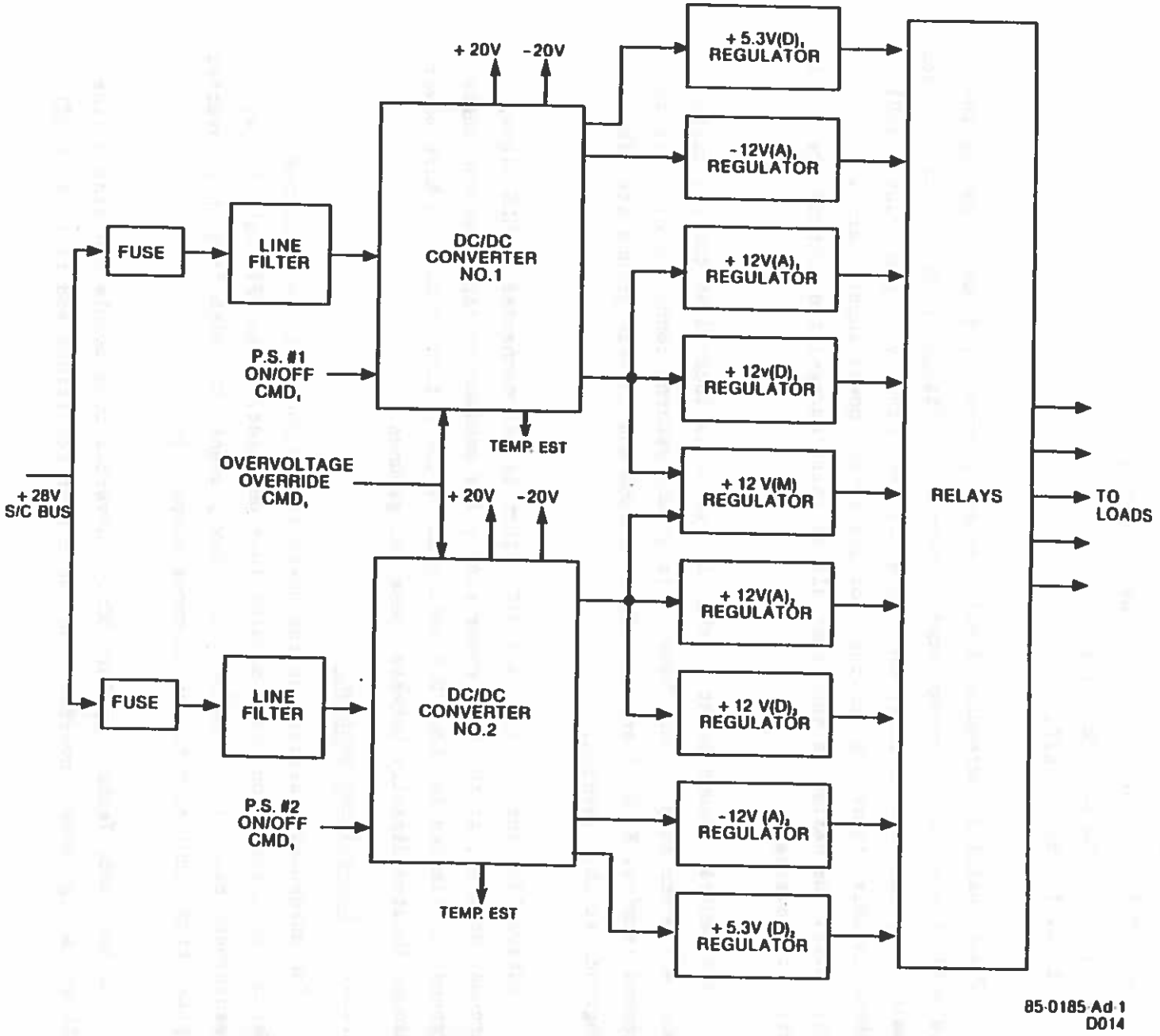


Figure 2.1.4-1. Simplified 5D-3 OLS Main Power Supply

In addition to the regulated outputs, the main power supply also supplies the following unregulated voltages:

+4.4V (U) to the HVPS and ENPA

-11.2V (U) to the I/O, formatters and ENPA

-13.2V (U) to the DME and HVPS

-19.4V (U) to the HVPS

These auxiliary unregulated voltages are derived by diode or-gating the outputs of appropriate unregulated or regulated voltages from each of the dual main power supplies as shown on Figure 2.1.4-2. Other voltages (+20V, -20V) shown in this figure are provided for use by the power supply series regulator. The design is such that all of these unregulated outputs are short circuit protected.

The central ground point of the OLS system is located at the RFI tight box. All power supply loads have their ground returns connected directly to ground terminal E208. Also, the signal ground and chassis ground are tied together at this terminal.

Internally, the OLS system's S/C return is not connected to OLS signal ground. However, at the main power supply the maximum voltages between these grounds is limited to about 0.5 volt peak by the action of back to back power diodes located directly between these two grounds.

2.1.4.1.1 Unregulated Section

The unregulated section of the power supply contains two Assurance Technology Corporation (ATC) modules (one per side) in an RFI tight box with feedthrough capacitors. The RFI tight box prevents the high frequency inverter spikes from coupling onto the numerous output lines.

An Assurance Technology Corp DC/DC Converter cube module contains a line filter, a high power inverter, and the output rectifiers and filters. A TTL

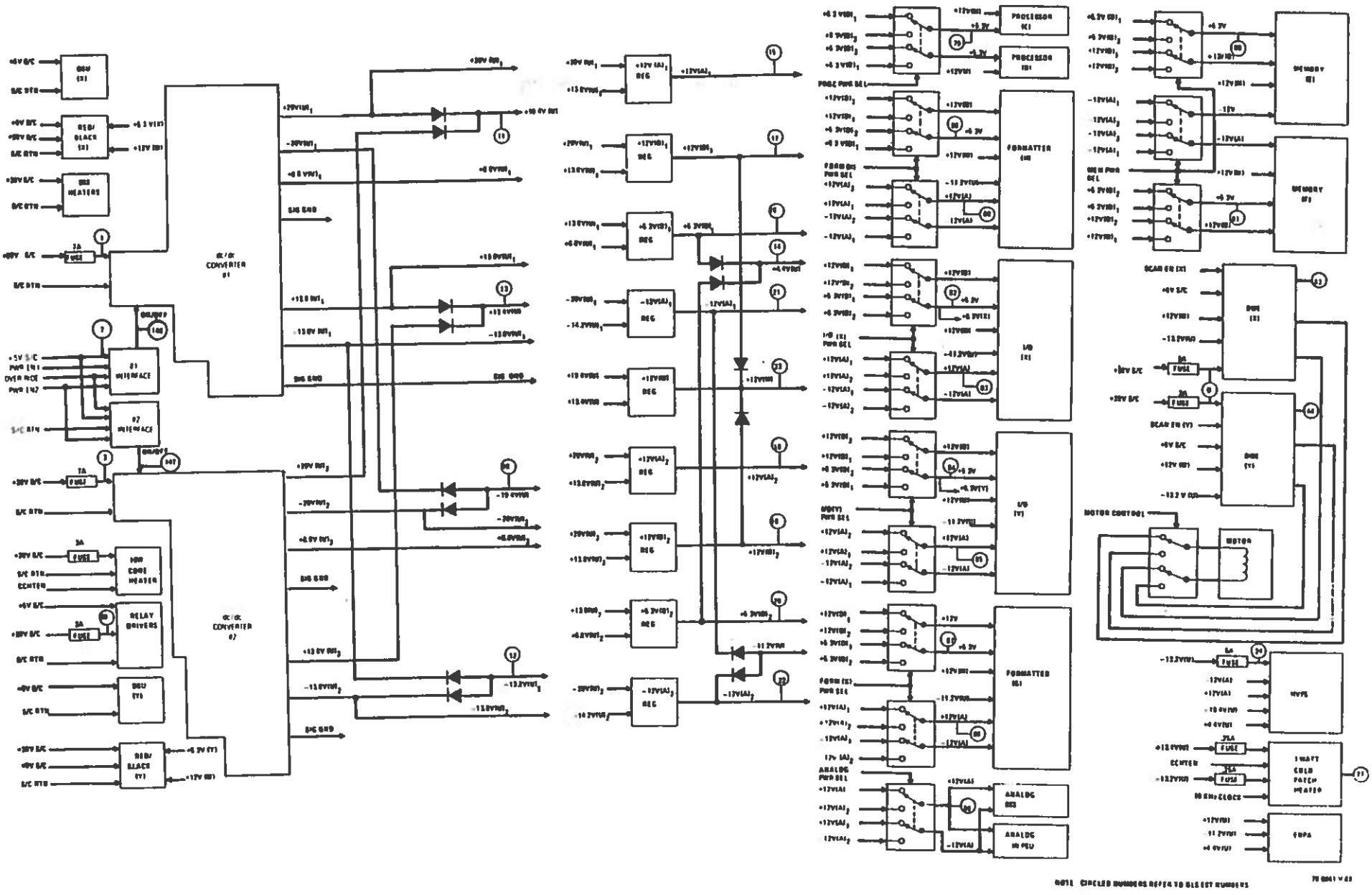


Figure 2.1.4-2 OLS Power Distribution System

compatible input provides efficient solid-state ON/OFF control. Standby current from the +28 volt dc bus is less than 10 milliamperes per side. This module converts the filtered +28 volt dc S/C bus into a 56 volt peak-to-peak squarewave at a frequency of 25 ±4 kHz. To protect the inverter and other circuitry from low frequency, high voltage transients on the prime power bus, this module incorporates a +31.3 ±1 volt automatic overvoltage shutdown feature. To prevent chatter, the positive feedback overvoltage circuit has a small but controlled "dead zone" or hysteresis. Ground control through a S/C input signal can override this overvoltage shutdown feature. However, if a line transient exceeds about 38 volts when the overvoltage protection circuit is disabled by use of the S/C override command, a catastrophic voltage breakdown failure of an inverter switching transistor may occur.

The ATC power supply module also contains the multiple secondary stepdown isolation transformer driving rectifier-filter stages. The outputs are +13.6 volts dc ±2 percent at a load current of 2.8 amperes, -13.8 volts dc ±3 percent at 0.4 amps, +20 volts dc ±3 percent at 60 milliamperes, -20 volts dc ±3 percent at 40 milliamperes and +6.60 volts dc ±2 percent at 5.5 amperes. Hot carrier (Schottky barrier) diodes, which have extremely low forward voltage drop, are used as rectifier diodes in the +6.6 volt supply to improve efficiency.

The minimum overall efficiency of the unregulated section of the ATC power supply is 78 percent. The ATC power supply also incorporates: 1) "soft" start up and 2) automatic shutdown upon overload input current drain followed by self-restart.

2.1.4.1.2 Regulated Section

The regulated section of the main power supply contains nine series-pass, current-limited voltage regulators; four per side (+12V (A), +12V (D), +5V (D), -12V (A)) plus the +12V (M) supply (single). (A) represents analog use and (D) is for digital use. M represents main.

The positive regulators use TO-111 case 2N3752 transistors (30 watts maximum power dissipation at 100°C case temperature) for the series pass transistor. The regulator block is the standard uA723. To obtain high efficiency at the required ripple suppression, a low input-output voltage differential across the series pass transistor is used. This low input/output differential necessitates a second unregulated input voltage to maintain the desired performance from the uA723 regulator block.

Figure 2.1.4-3 is a schematic of the positive type regulator circuit used. The voltage drop across R5 is used for load current sensing. When the voltage drop across this resistor exceeds 0.25 volt, current limiting is initiated. The unusual regulator configuration chosen for the positive regulator has the following advantages over a conventional approach:

Higher efficiency due to lower required voltage drop across the current sense resistor

Better predictability and stability of current limiting with temperature variation

Lower output impedance and improved power supply loop stability

The +12 volt (D) supply uses two 2N3752 series pass transistors in parallel with 0.0909 ohm resistors in the emitters to force equal current sharing. The +5.3 volt regulator also uses two pass transistors in parallel and, for current buffering, uses a third 2N3752 as an emitter follower driver between the uA723 block and the output pair of transistors.

The -12 volt series-regulated current limited supply uses a standard configuration. A DH711117E voltage reference device and an LM108A operational amplifier are equivalent to the uA723 regulator block. A 71SH157 (2N5001) transistor, which is a PNP equivalent of the NPN 2N3752 transistor, is used as the pass transistor.

The current limiting setting for each $\pm$1 percent accuracy voltage regulator is listed in Table 2.1.4-1 along with the power dissipated in the series pass transistor when the output is shorted.

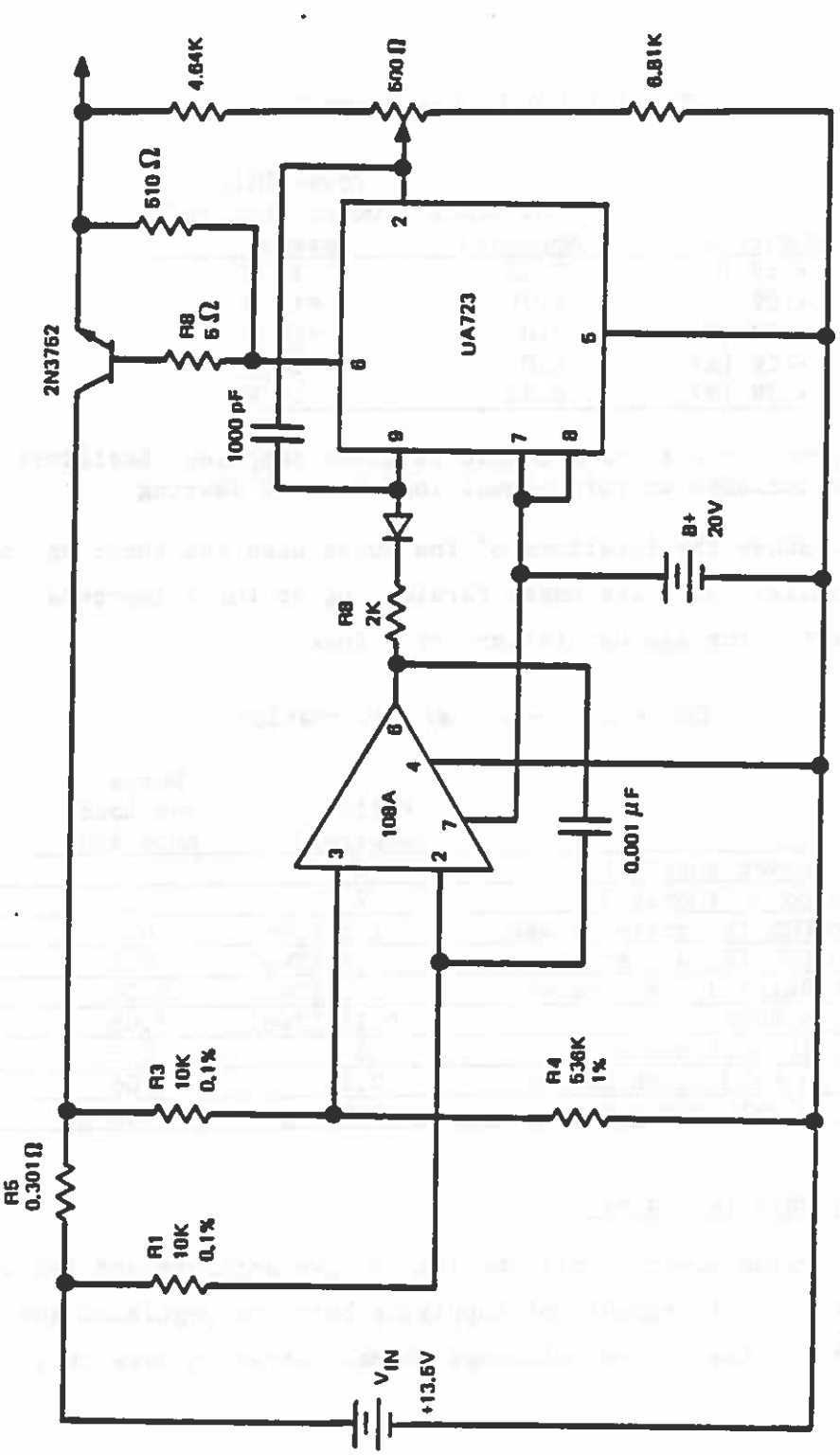


Figure 2.1.4-3. Positive Regulator Circuitry

The maximum power dissipated in a series pass transistor when the output is accidentally shorted has been limited to 19 watts for reliability consideration. The 2N3752 transistors are rated at 30 watts at 100°C case temperature.

Table 2.1.4-1. Regulator Data

Regulator	Current Limit (Amperes)	Power Diss. (Output Shorted) Amperes
+12V (A)	0.83	11 W
+12V (D)	2.75	*17 W
+ 5V (D)	7.0	*19 W
-12V (A)	1.0	13 W
+12V (M)	0.83	11 W

*Two series pass transistors are used in these supplies. Resistors in the emitter have been included to force equal load current sharing.

Table 2.1.4-2 shows the locations of the fuses used and their ratings, and tells whether parallel fuses are used. Paralleling of fuses improves reliability by protecting against failure of a fuse.

Table 2.1.4-2. Fuse Information

Location	Rating (Amperes)	Normal Peak Load (Amperes)
+28 V bus to power supply 1	7	3
+28 V bus to power supply 2	7	3
+28 V bus to DME (X) driver stage	1.5 (Two)	0.5
+28 V bus to DME (Y) driver stage	1.5 (Two)	0.5
+28 V bus to Relay driver boards	1.5 (Two)	0.06
-13.6 V (U) to HVPS	0.25 (Two)	0.03
+28 V bus to 10 watt heater	3	0.3
+13.4 V (U) to cold patch heater	0.25	0.06
-13.6 V (U) to cold patch heater	0.25	0.06

2.1.4.1.3 Power Supply Switching

The 5D-3 OLS system power supply consists of two separate and independent supplies, each of which is capable of supplying both the regulated and the unregulated power for the system. Although normal operation uses only one

supply at a time, both can be enabled simultaneously. Each power supply is controlled by a PWR enable command, which turns on the inverter.

The redundant power switching system is shown in the system block diagram (Figure 2.1.0-2). Power switching to the functional elements of the digital processing subsystem is controlled by ground command through the configuration of 14 magnetic latching relays in the power supply. Each formatter or I/O block can be switched to either power supply bus 1 or 2. (Both can also be switched to the same bus.) The processors and memories can be independently cross-switched between busses; i.e., processor C to power bus 1 and processor D to power bus 2, or processor C to power bus 2 and processor D to power bus 1. Neither both processors nor both memories can be switched to the same power bus by hardware design, but both sets can be activated if both power supplies are enabled. The analog functional block can be switched to either power bus 1 or 2. All power configuration switching using the latching relays is controlled by discrete spacecraft command lines. These command lines are either level discrete or pulse discrete and are listed below:

Power enable 1 (level) - Turns on the inverter on power supply 1 side.

Power enable 2 (level) - Turns on the inverter on power supply 2 side.

Processor Power Select (pulse pair) - Connects processor C to power supply 1 and processor D to power supply 2 or connects processor D to power supply 1 and processor C to power supply 2.

Memory Power Select (pulse pair) - Connects memory E to power supply 1 and memory F to power supply 2 or connects memory F to power supply 1 and memory E to power supply 2.

I/O X Power Select (pulse pair) - Connects I/O X to power supply 1 or 2.

I/O Y Power Select (pulse pair) - Connects I/O Y to power supply 1 or 2.

Formatter G Power Select (pulse pair) - Connects formatter G to power supply 1 or 2.

Formatter H Power Select (pulse pair) - Connects formatter H to power supply 1 or 2.

Analog Power Select (pulse pair) - Connects the analog circuitry to power supply 1 or 2.

Motor Control (pulse pair) - Connects the scanning motor to either DME X or DME Y.

For further details see Section 3.3.1, Spacecraft Commands.

In general, the relays allow either power supply to provide regulated voltages to either load. Also, they effectively permit shorts to ground across the supplies on the source side or the load side of the relays to be cleared from the primary power bus.

2.1.4.2 High Voltage Power Supply

The high voltage power supply (HVPS) assembly supports the electrical operating requirements of the photomultiplier tube (PMT) in the L channel.

Each PMT requires tightly regulated, extremely low ripple, selectable voltages at the following tube elements:

Element	Symbol	Typical Required DC Voltages
Focus	VF	-908 (On) -1075 (Blanked off)
Photocathode	VPC	-1053
Dynode #1	VD	- 735
Plate	VP	- 453
Cone	VC	- 987
Aperture	VA	- 975

The voltages listed above and those shown in Figure 2.1.4-4 are for a typical PMT assembly. It should be noted that different tubes require substantially different voltages to obtain optimum system level performance.

In addition to the above element voltages, the PMT tube assembly contains six dynodes with incrementally decreasing potentials. The incremental values of voltage for the dynodes are obtained from a voltage divider that is integral to the PMT assembly.

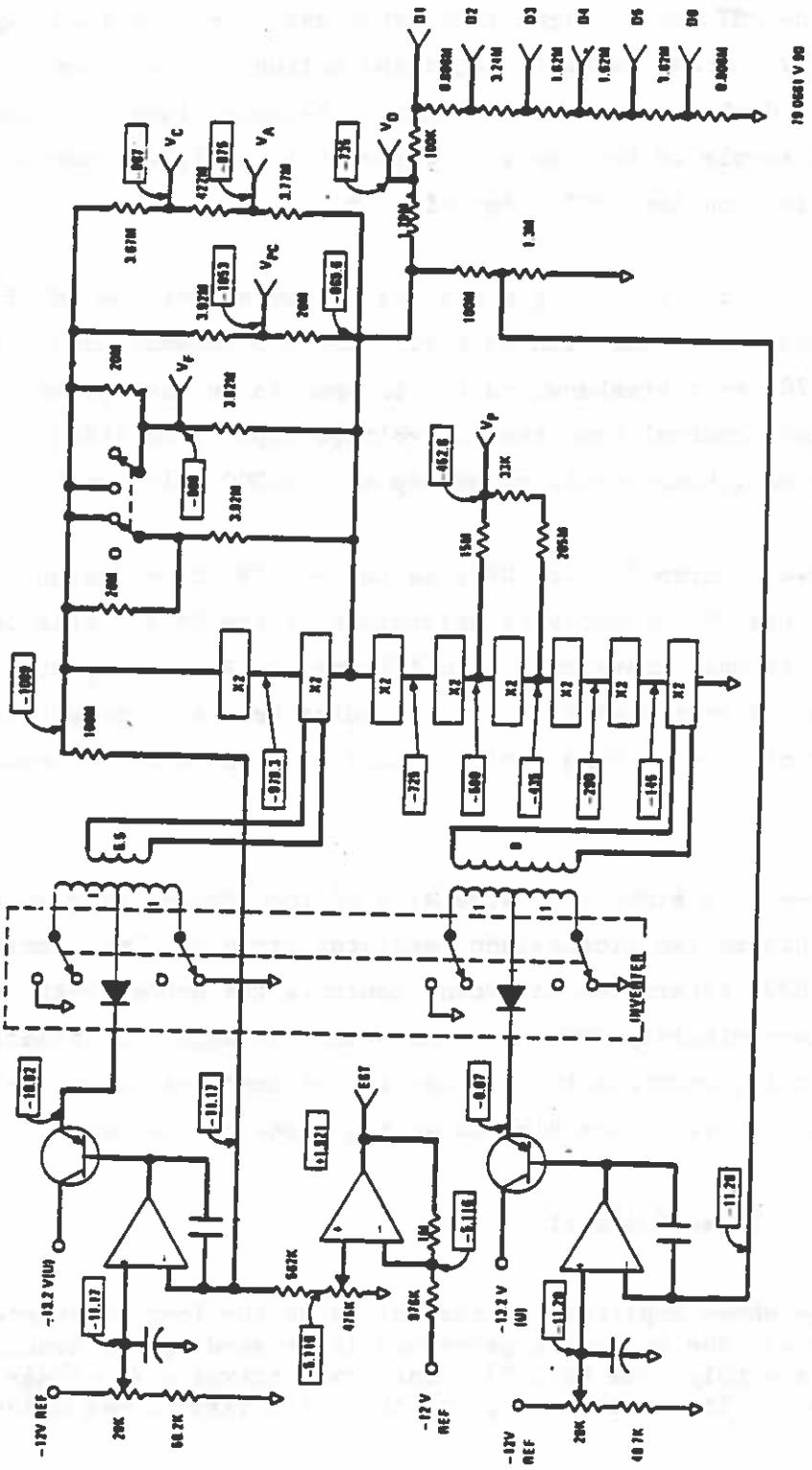


Figure 2.1.4-4. HVPS Simplified Schematic

A high voltage electronic switch is required to switch the focus element voltage rapidly from the PMT ON state to the back biased PMT Blanked OFF state once each scan line for video dark level dc restoration. This switch also acts as a "crowbar" to rapidly blank the PMT and thus prevent permanent S/N degradation of the PMT due to high light level exposure when such exposure level is sensed by the HRD channel. Switching action is analogous to operation of a single-pole, double-throw switch. Thus, a balanced load is presented to the high voltage supply so that switching does not instigate undesired low amplitude long time constant PMT video effects.

State control of the switching action is determined by the PMT BLANK input. An opto-coupler (a LED with an associated phototransistor) integrated circuit with a 1700 volt breakdown rating is used to dc couple the low amplitude PMT BLANK control from the low voltage input side (LED) to the high voltage switch side (phototransistor on top of a -1000 volt supply).

The prime power source for the HVPS is the -13.2V (U) dc output. The ON/OFF state of this PMT assembly is determined by the HVPS uplink command. Typically, this assembly draws only 20 milliamperes. An 0.5 ampere line fuse has been inserted in series with this -13.2 volts bus. A permanent fault on this bus, if not cleared by fuse action, would cause a total OLS system failure.

Figure 2.1.4-4 is a simplified schematic of the complex high voltage power supply, which contains two closed-loop regulator circuits. One supply approximately - 870V referenced to ground controls the dynode voltage. The second supply, approximately 220 Vdc whose output is added to (floats on top of) the first supply, controls the voltage at the emitters of the balanced switch transistors. This is the highest voltage node in the supply.

Loop operation is as follows:

A voltage whose amplitude is controlled by the loop is chopped by a 66-kHz inverter. The ac signal generated is stepped up via transformers. In the dynode supply, the (1:1:9) transformer drives a six-stage diode doubler network. In the other supply, the 1:1:5 transformer drives a

two-stage diode doubler network. After rectification and filtering, both outputs are divided down by 100 meghom resistive divider networks and are then compared against the -12 volt (A) regulated voltage. The HVPS uses the -12 volt (A) supply as a reference and varies directly with variance of that supply.

The voltages listed in Figure 2.1.4-4 are those for a typical PMT assembly. They are shown primarily to aid in understanding circuit operation. A typical HVPS EST voltage for the PMT is +2.10 volts dc. As different PMT tubes require different element voltages, the EST voltage will vary from assembly to assembly. However, once the nominal value has been determined for a particular unit, variances around the nominal should be less than ±1 percent unless a failure occurs.

The photomultiplier tube assembly as purchased from EMR is potted with Solithane 113 compound. The high voltage section of the HVPS is potted with soft, repairable, low outgassing RTV11. To prevent high voltage problems a detailed assembly procedure (9RA4924) has been generated for this assembly. This step-by-step procedure specifies lead placement, cleaning procedure, assemble sequence, potting procedures, and testing operation. The final lower level test is a three day vacuum test.

2.1.4.3 +5 Volt Spacecraft Conditioning

The +5 volt dc spacecraft source is used for the interface circuits that must be powered whether the OLS is on or off. These circuits receive signal inputs relative to spacecraft return. The interface signals are used to configure the latching relays that connect various subsystems to either power supply 1 or power supply 2 of the OLS as well as to enable or disable these power supplies.

Except for fault protection, the +5 volt dc spacecraft source is used without further conditioning by the OLS. Faults internal to the power supply assembly on the +5 volt spacecraft bus have been decoupled from the bus by placing large value, high wattage resistors in series with each user of +5 volts S/C power. Thus, except for shorts to ground on the input side of the

protection resistors, two part failures would be required in an individual circuit before a short would occur across this bus.

2.1.4.4 T-Cone Heaters

These heaters are enabled by a single ground command when (infrequent) discontamination of the T-cone cooler is desired. A low level input on the CCHTEN internal signal line simultaneously turns on the 1 watt cold patch heater circuit and the 10 watt outer stage heater circuit to the T-cone cooler. All voltage inputs to these circuits are fused so that a failure in these circuits cannot cause a permanent line fault.

The 10 watt heater circuit is very simple. A high power PNP transistor is used as a switch between the +28 volt S/C bus and a 78 ohm high power resistor mounted on the outer stage of the T channel cooler.

The inner stage 1 watt heater circuit is more complicated. The heating resistor, the same resistor that is used by the inner stage temperature control loop, is located on the cold patch. A high voltage, low current power source is required to generate the 1 watt in this resistor. A 10 kHz digital clock is used to chop the difference in voltages between the +13.4 volt (U) and the -13.2 volt (U) supplies. A two-stage transformerless diode/capacitor doubler network is then used to generate 47 volt dc (U) across the 2100 ohm cold path heating resistor.

2.1.5 Scanner Monitor and Control

The scanner monitor and control function provides the required scan motion of the OLS line of sight on the scene in conjunction with the along track movement of the spacecraft in orbit.

The scanner monitor and control function has three functional areas:

Scan angle indication
Scanner drive
Image motion compensation

The scan angle indication is accomplished by the main optical shaft angle encoder, two auxiliary encoders, and signal processing electronics. The scanner drive is accomplished with a drive motor and its associated drive motor electronics (DME). The image motion compensation (IMC) is accomplished by an IMC drive mechanism with control electronics.

Figure 2.1.5-1 is a block diagram of the elements of the scanner monitor and control function showing their interrelationships.

2.1.5.1 Scan Angle Indication

The indication of scan angle is provided by a special type of optical encoder subsystem that provides information on three signal lines. A series of 2049 pulses on one signal line are spaced at 2048 equal increments of angle throughout the total ±57.85° peak scan. These pulses which are called Delphi or clock pulses, occur every 0.98551 milliradian of scan angle. A special pulse at the middle of scan (Nadir) is decoded onto a second signal line. On each scan line (half cycle) three special pulses (hack, +1018, and -1018) are decoded and put on the third signal line, called the "control line." The Hack pulse is provided 8.24° or 146 Delphi's on the +Z side of nadir to differentiate -Z (left) from +Z (right). The ±1018 pulses are near the ends of scan at ±57° 28' 55". The nominal scan is ±1024.5 Delphi pulses, or 57.85° peak scan angle. For a full cycle there is a pair of Nadir pulses, a pair of Hack pulses, a pair of +1018 pulses, and a pair of -1018 pulses.

The outputs of the main optical encoder are derived from the signal variations sensed by two detectors that receive image light through a reticle mask. The variations are made proportional to scan angle by reflecting the light from optically flat mirror surfaces (facets) on a polygon faceted ring attached to the shaft of the oscillating scanner. The main optical encoder head, along with a series of 15 front facets on the faceted polygon ring, produces the Delphi pulses and 15 facet-centered fiducial pulses (FID's).

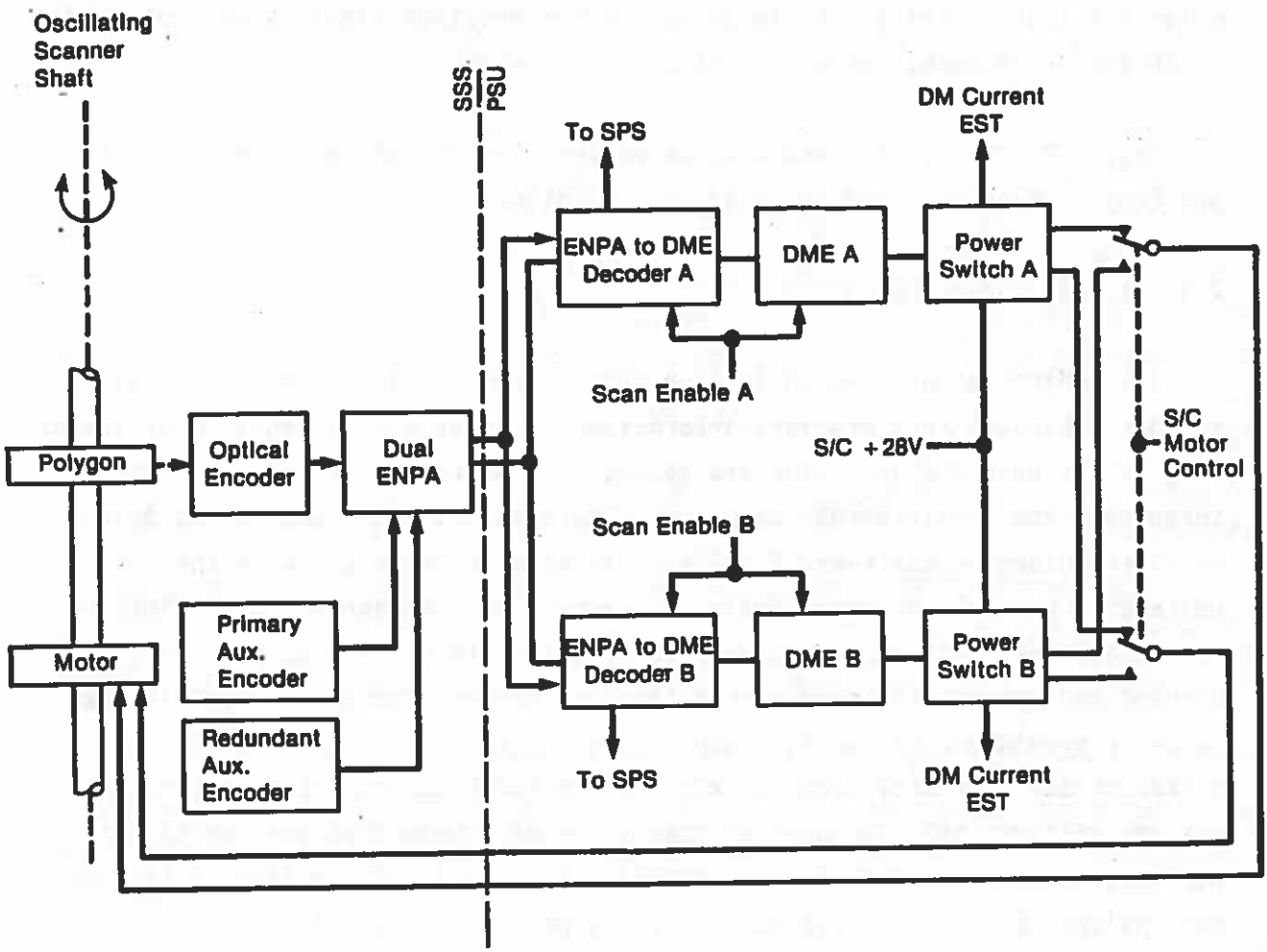


Figure 2.1.5-1. Scan Drive System Block Diagram

The redundant (backup) Auxiliary Encoder, along with a series of four facets on the rear side of the faceted polygon ring, produces BU AUX Nadir and BU AUX Control pulses used for gating the proper FID pulses to generate the Nadir and Control pulses. The primary AUX Encoder, together with four opaque vanes on the oscillating shaft, also produces AUX Nadir and AUX Control pulses.

Figure 2.1.5-2, a top view of the main encoder, shows the Redundant Auxiliary Encoder and the faceted polygon ring.

The main encoder has three (infrared) light emitting diodes (LED's); one serves as the Delphi source and one of two selected by encoder Primary/Backup command serves as the fiducial (FID) source. For high reliability, hermetically sealed high efficiency GaAlAs LED's are used. The reticle/detector assembly in the main optical encoder contains a small silicon photodiode detector behind each of two FID detector slits. The selected detector receives light from the selected FID LED source slit only when 1 of the 15 polygon mirror facets is normal to the optical encoder lens axis. Either the redundant FID 1 or the primary FID 2 LED can be selected, but both cannot be on simultaneously. The Delphi LED emits light through the Delphi source slit of the reticle, which is collimated by the encoder lens, reflected by the polygon facet, passes back through the lens, and is imaged onto the Delphi reticle array of 237 receiving slits. The reticle pattern is shown in Figure 2.1.5-3 and the side view of the main optical encoder is illustrated in Figure 2.1.5-4. Light is received by the long Delphi silicon photodiode when the source slit image passes through an open slit of the Delphi reticle, and is blocked from the photodiode when the image falls on an opaque bar of the reticle. The 50 um wide bars are 100 um apart. There are 146 Delphi pulses between the normal to one facet and the normal to the next facet (except between facets 1 and 2 and facets 14 and 15, where there are 142 Delphi pulses). Thus, the total Delphi pulse count from Facet 8 normal (nadir) to facet 1 or to facet 15 normal is 1018. The facets of the polygon are integral multiples of 0.98551 milliradian, so that images returned simultaneously from adjacent facets are combined in phases (e.g., at Delphi 73, a return from one facet is imaged on slit -73 while a return from the adjacent facet is imaged on slit +73). Initial effective focal length and focus adjustments are necessary to achieve in-phase combining. The angle

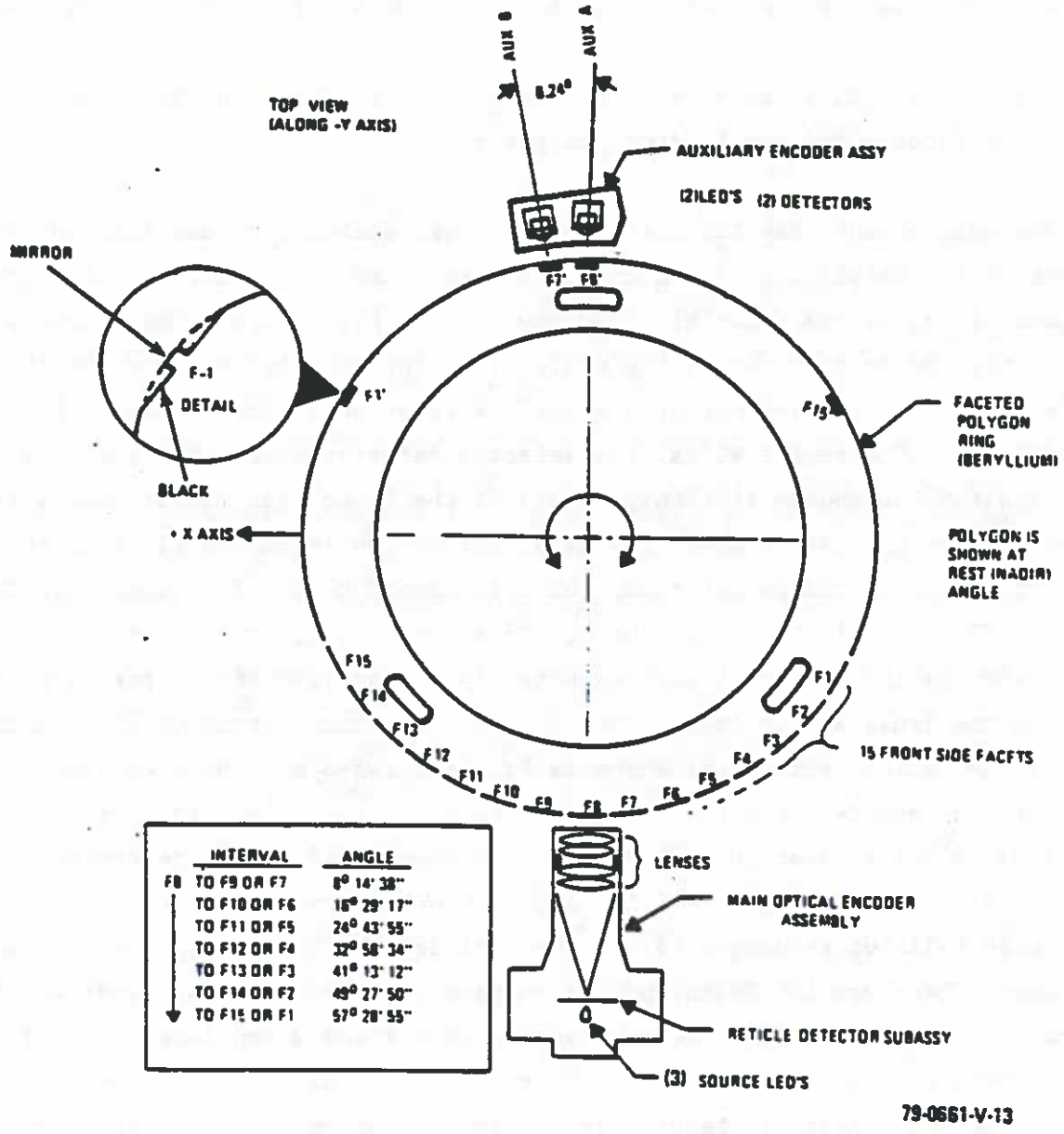


Figure 2.1.5-2. Main Optical Encoder, Top View

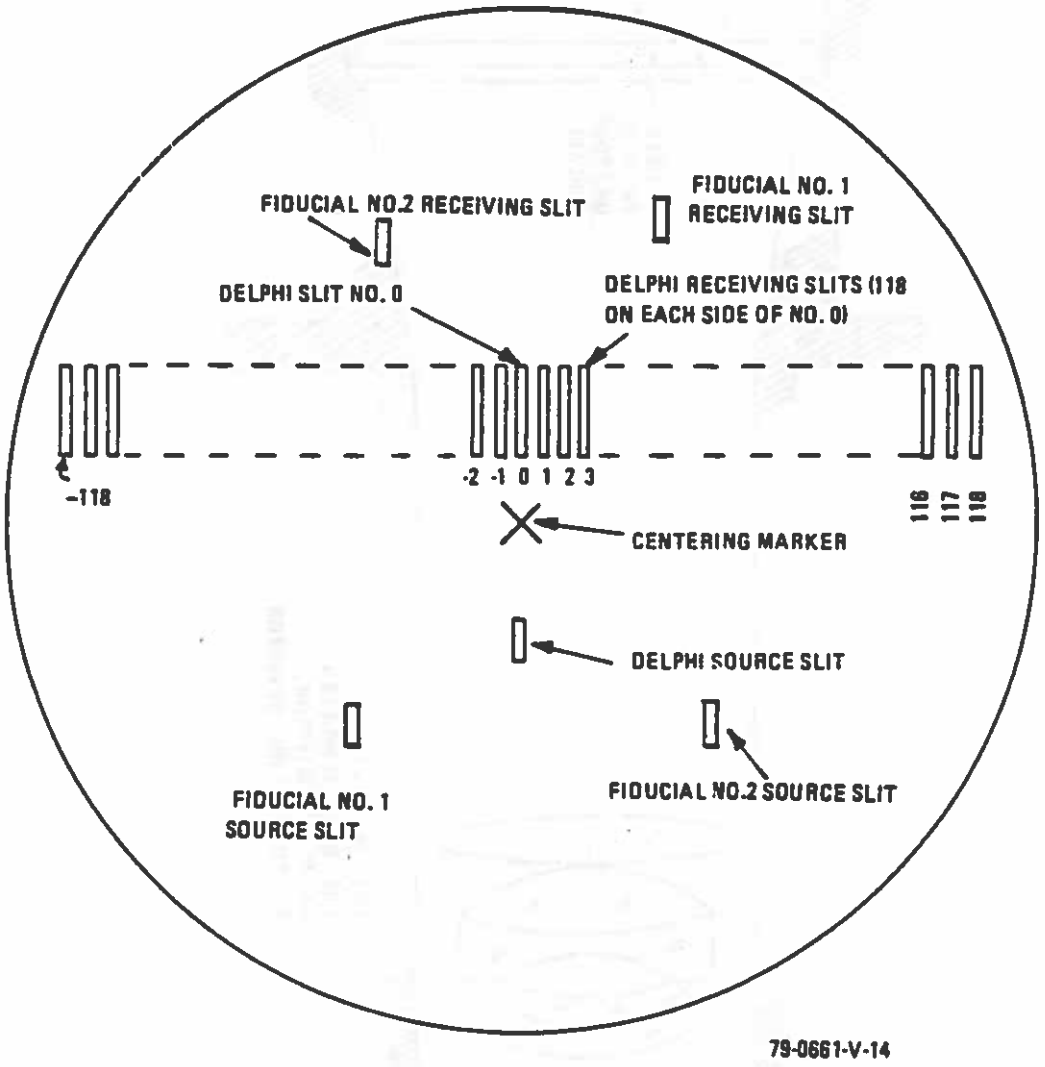


Figure 2.1.5-3. Main Optical Encoder Reticle Pattern

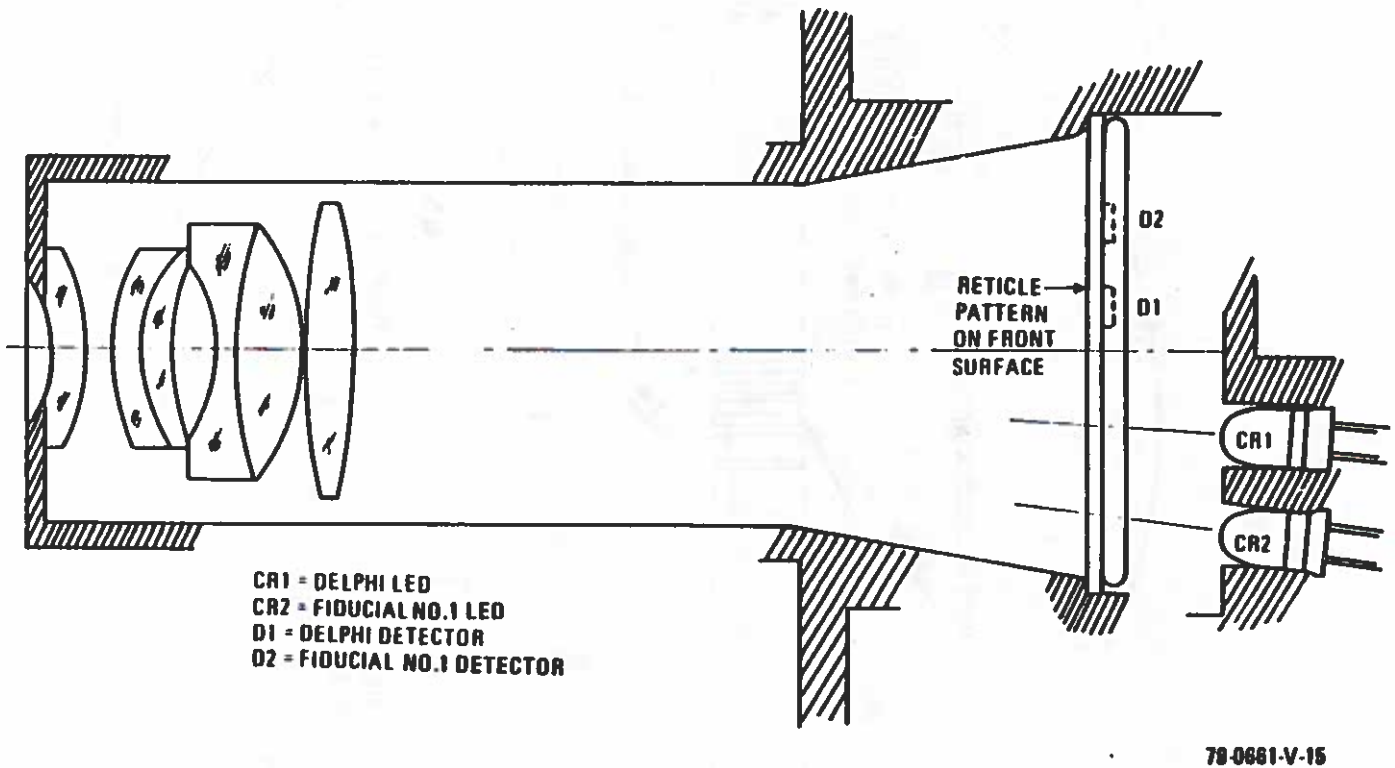


Figure 2.1.5-4. Main Optical Encoder, Side View

between polygon facets is accurate to ±5 arc sec. Sharp "corners" form the intersection of any two adjacent facets. The overall main encoder maximum error is below ±15 arc sec. The encoder lens, which has six elements, provides collimation, flat field correction at the image plane, and an intentional "distortion" in image height function versus angle that results in a linear relationship between shaft angle and Delphi image distance from zero. The zero Delphi pulse is coincident with the FID pulse.

The Delphi pulses vary in their time spacing from 26 microseconds to 193 microseconds as the scan velocity varies from nadir to near peak amplitude. The nominal peak scan amplitude is 1024.5 Delphi pulses (2049 Delphi intervals per scan line).

The main encoder Delphi, FID 1 and FID 2 silicon detectors are coupled to low noise, high gain preamplifiers as an input current. The signals are amplified, low pass filtered, and sent to a threshold crossing detector (LM111 comparator) circuit having a small hysteresis band. The encoder preamplifier (ENPA) electronics also has the logic to use the two auxiliary signals and the FID pulses to form the "nadir out" and "control out" signals to the signal processor.

2.1.5.1.1 Encoder Preamplifier (ENPA)

The ENPA contains transimpedance type preamplifiers for the Delphi, the FID 1, and the FID 2 signal currents, the second stage amplifiers, the thresholding circuits, the logic for forming nadir and contol, and the dc current switching for the selected FID LED and selected AUX encoder LED's. Figure 2.1.5-5 is a block diagram showing the ENPA circuits and their relationship to the encoder.

The three preamplifiers actively bootstrap drive each associated photodiode detector's cathode to reduce the boost of active device noise voltage with detector capacitance. The FID 1 amplifiers, threshold, and logic are completely backed up by the redundant FID 2 hardware. The Delphi first stage output branches into two redundant signal processing paths each containing a second

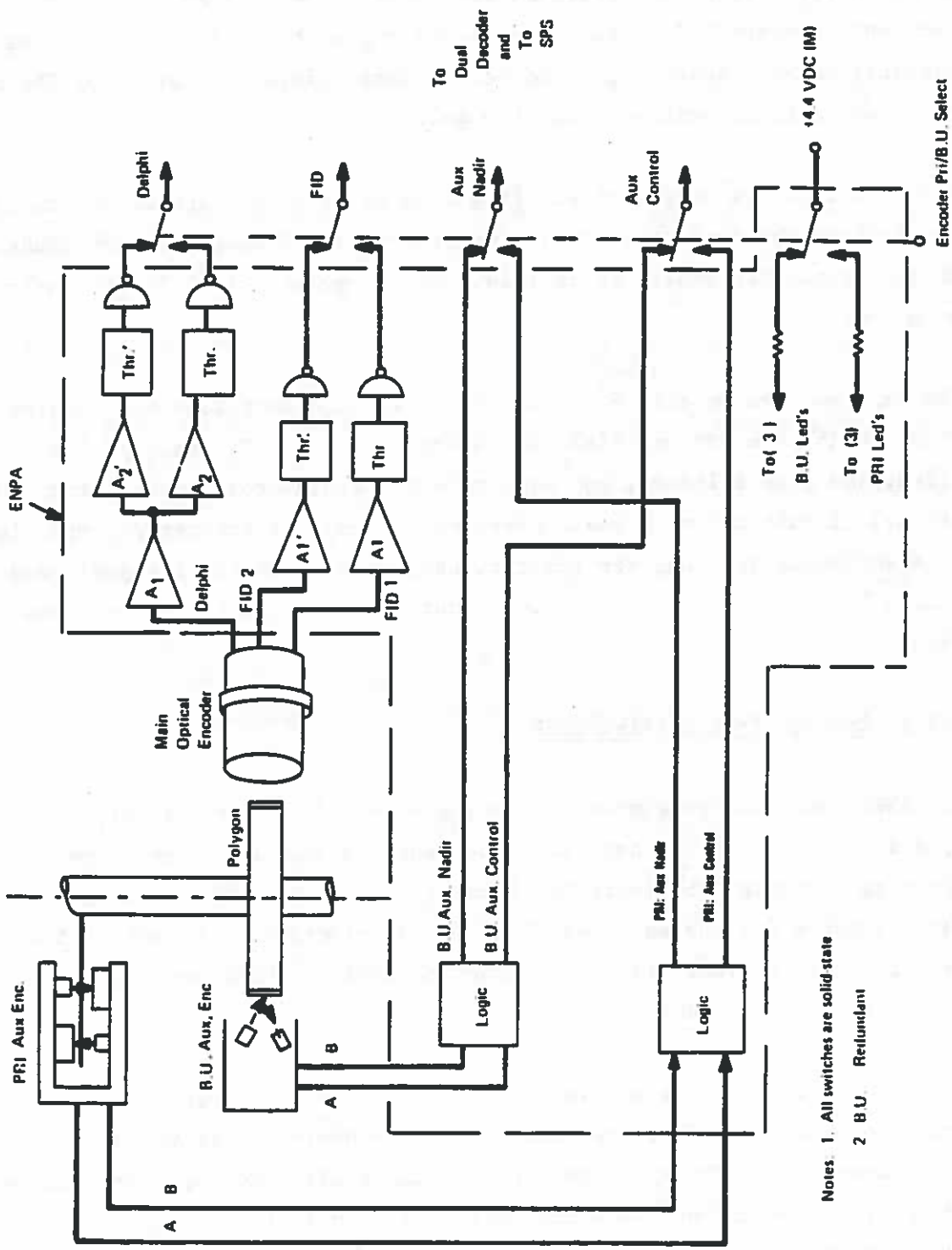


Figure 2.1.5-5. Redundant Encoder System Block Diagram

amplifier stage, threshold, and logic. When encoder primary is selected, LED dc current switching causes FID 2 LED and the primary auxiliary encoder's two LED's to be on. When encoder redundant is selected, these three LED's are shut off and the FID 1 LED and the redundant auxiliary encoder's two LED's are supplied current. The encoder primary or redundant selection is independent of the DME A or B selection.

2.1.5.1.2 Auxiliary Encoders

The ENPA logic is simplified by the use of backside facet mirrors and by the auxiliary encoder angle selection. The AUX nadir signal is AUX channels A and B., the AUX control signal is AUX channels A and B. Primary and redundant sets of this logic are provided in the ENPA.

2.1.5.1.2.1 Primary Auxiliary Encoder

The primary auxiliary encoder assembly also has two channels; A and B. Each channel is a transmission type of optical path, as shown in Figure 2.1.5-6. Each channel has an LED and a combined photodiode detector and operational amplifier. Four vanes attached to the oscillating shaft obscure the light at angles that correspond to polygon Facets 1, 7, 8 and 15. An inverter complements the dark pulse into a positive-going logic pulse for the four key angular positions. Signals A and B yield AUX Nadir. Aux Nadir corresponds to the main encoder polygon facet 8. Signals A and $\bar{B}$ yield the AUX Control signal (corresponding to the angles of the main encoder polygon facets 1, 7, and 15).

2.1.5.1.2.2 Redundant Auxiliary Encoder

The redundant auxiliary encoder has two reflective type optical channels, AUX A and AUX B, to decode which of the 15 FID pulses is +1018 (facet 1), -1018 (facet 15), nadir (facet 8), and hack (facet 7). Figure 2.1.5-7 shows the polygon ring top view with its four auxiliary (backside) facets (facets 1', 7', 8', and 15') in the four key rotational positions illustrating the alignment with the AUX A and AUX B channels for decoding the FID's.

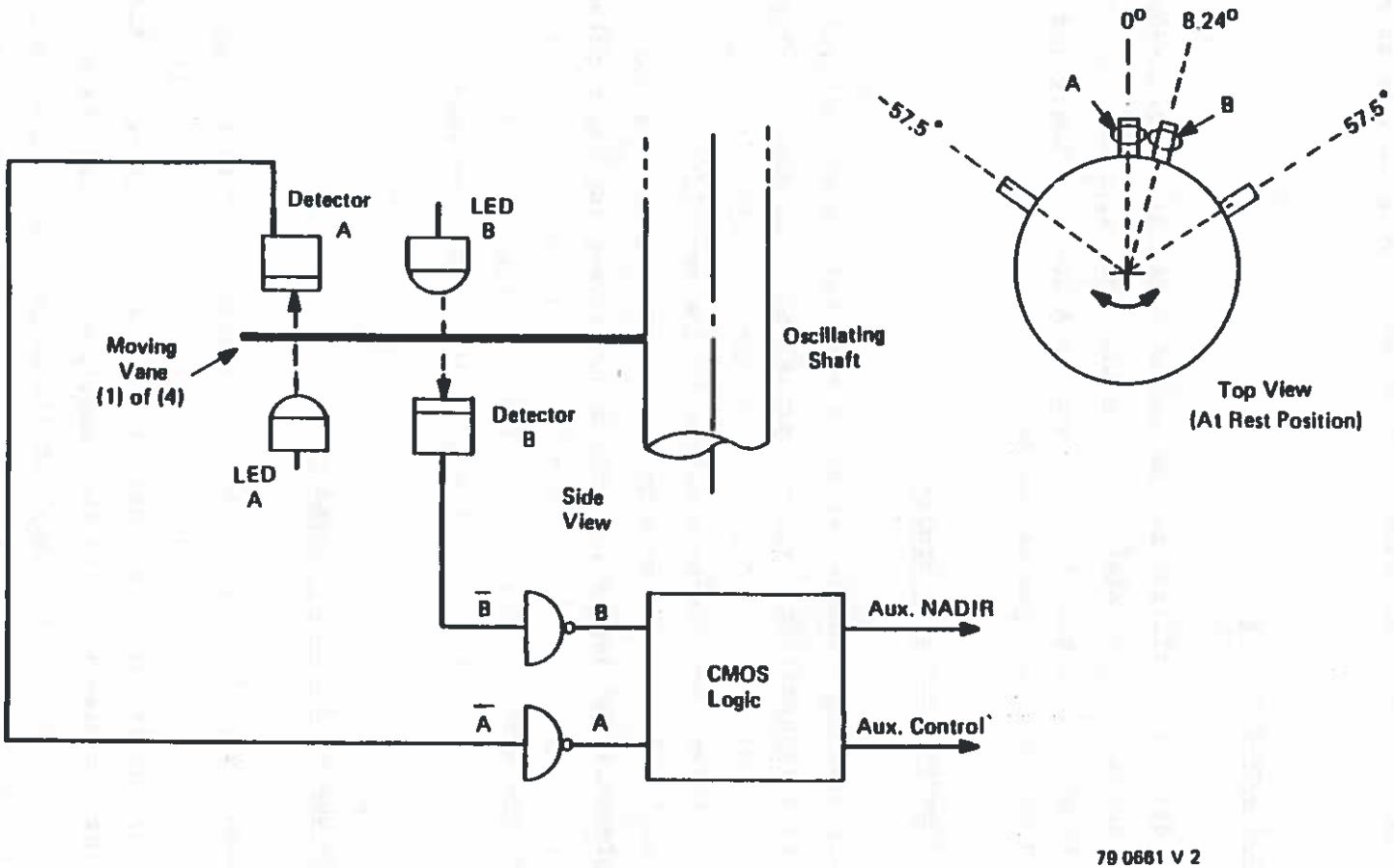


Figure 2.1.5-6. Primary Auxiliary Encoder Block Diagram

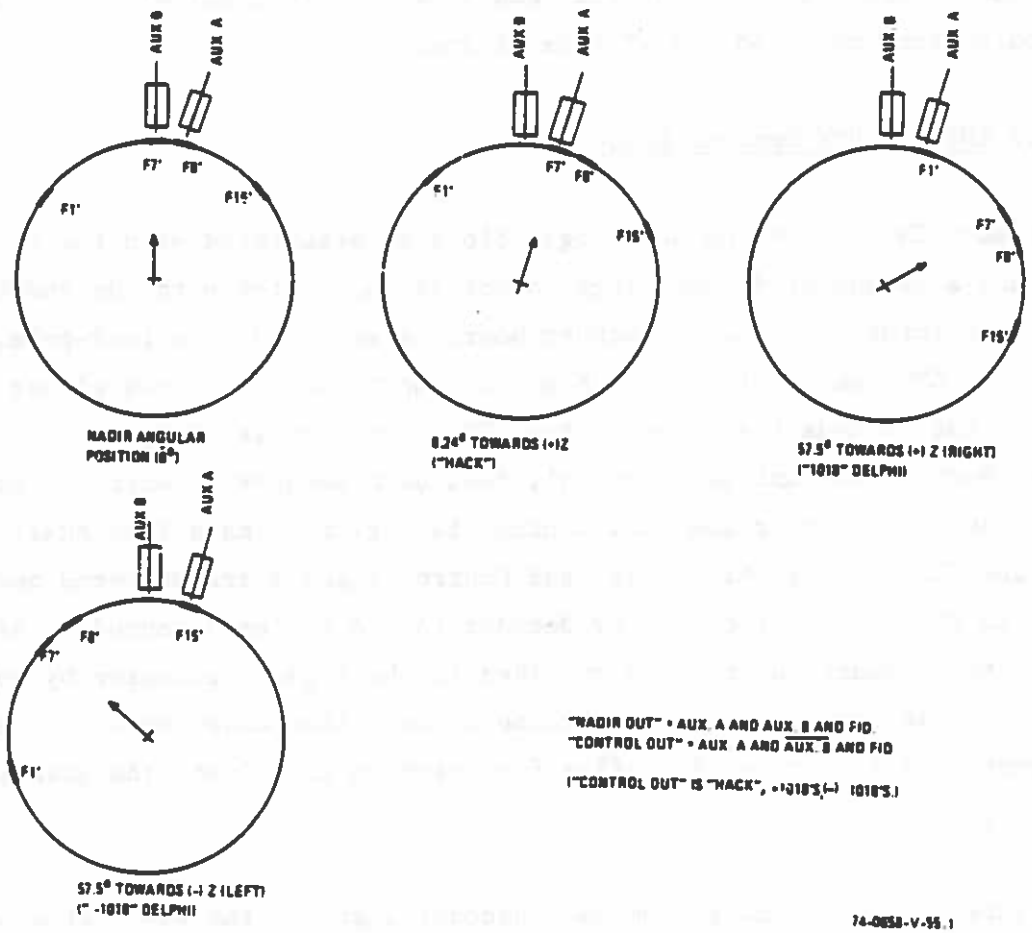


Figure 2.1.5-7. Auxiliary Encoder Key Alignments

2.1.5-8 shows one of the redundant auxiliary channels' side view. An LED with its own lens reflects from the redundant auxiliary facet mirror and energizes a combined (hybrid) photodiode detector and operational amplifier. The AUX A and AUX B pulses are quite broad, (approximately 4° wide) with large amplitudes to gate FID number 8 into the nadir logic and F10 numbers 1, 7, and 15 into the control logic circuitry. The center of the nadir FID pulse is coincident with the center of the zeroth pulse of the Delphi channel on Facet No. 8. The other fiducial pulse centers are also coincident with their corresponding facet normal Delphi pulse zero. The hack mark fiducial from Facet No. 7 is used to detect the right side of scan and is also coincident with the 146th Delphi pulse from nadir on the +Z side of scan.

2.1.5.1.3 ENPA to DME Decoder Logic

A primary ENPA to DME decoder logic block is associated with the primary DME (A) and a redundant decoder logic block is associated with the redundant DME (B). The input to the dual decoder board is selected by a four-pole, double-throw CMOS data select switch so the inputs may come from either the primary or the redundant encoder system. The four signals: Delphi, FID, Auxiliary Nadir, and Auxiliary Control, feed both decoders. Nadir is logically made from Auxiliary Nadir and FID. Control is logically made from Auxiliary Control and FID. The Delphi, Nadir, and Control signals are buffered and supplied to the signal processor by decoder (A). A buffered redundant set of the same three scanner signals is provided to the signal processor by decoder (B). Scan enable from the discrete ground command line also feeds both decoder logic areas. The left/right flip-flop from each DM also feeds the associated decoder logic.

The three output signals from each decoder logic to the associated DME are: hack left-to-right (only), 1018's pairs out, and scan ready. A four-level EST output signal generated by scan ready from both decoders is also provided.

Figure 2.1.5-9 is a detailed logic circuit of one channel of the ENPA to DME decoder. The flip-flop Z1A is set each nadir (polygon facet 8) by the wide auxiliary nadir pulse, thus enabling (high state) the pin 12 input to Z4D. When

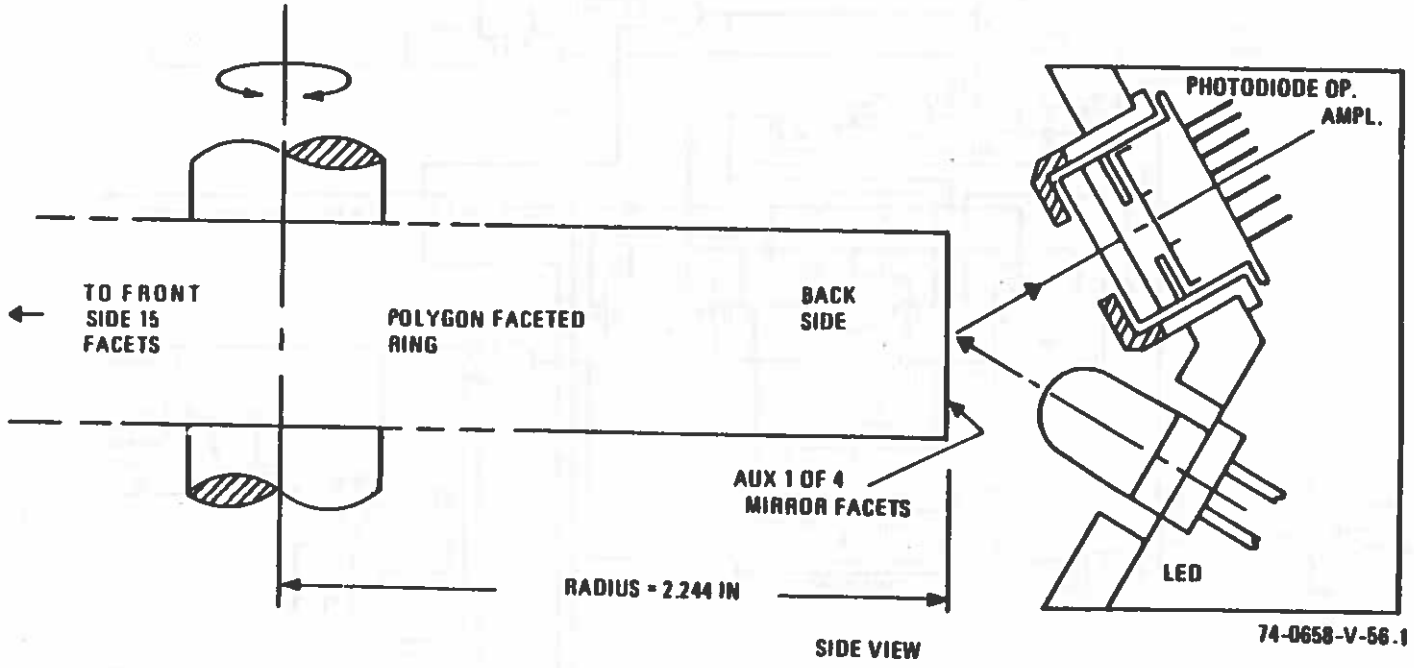


Figure 2.1.5-8. Redundant Auxiliary Encoder (One Channel of Two Redundant Aux Channels)

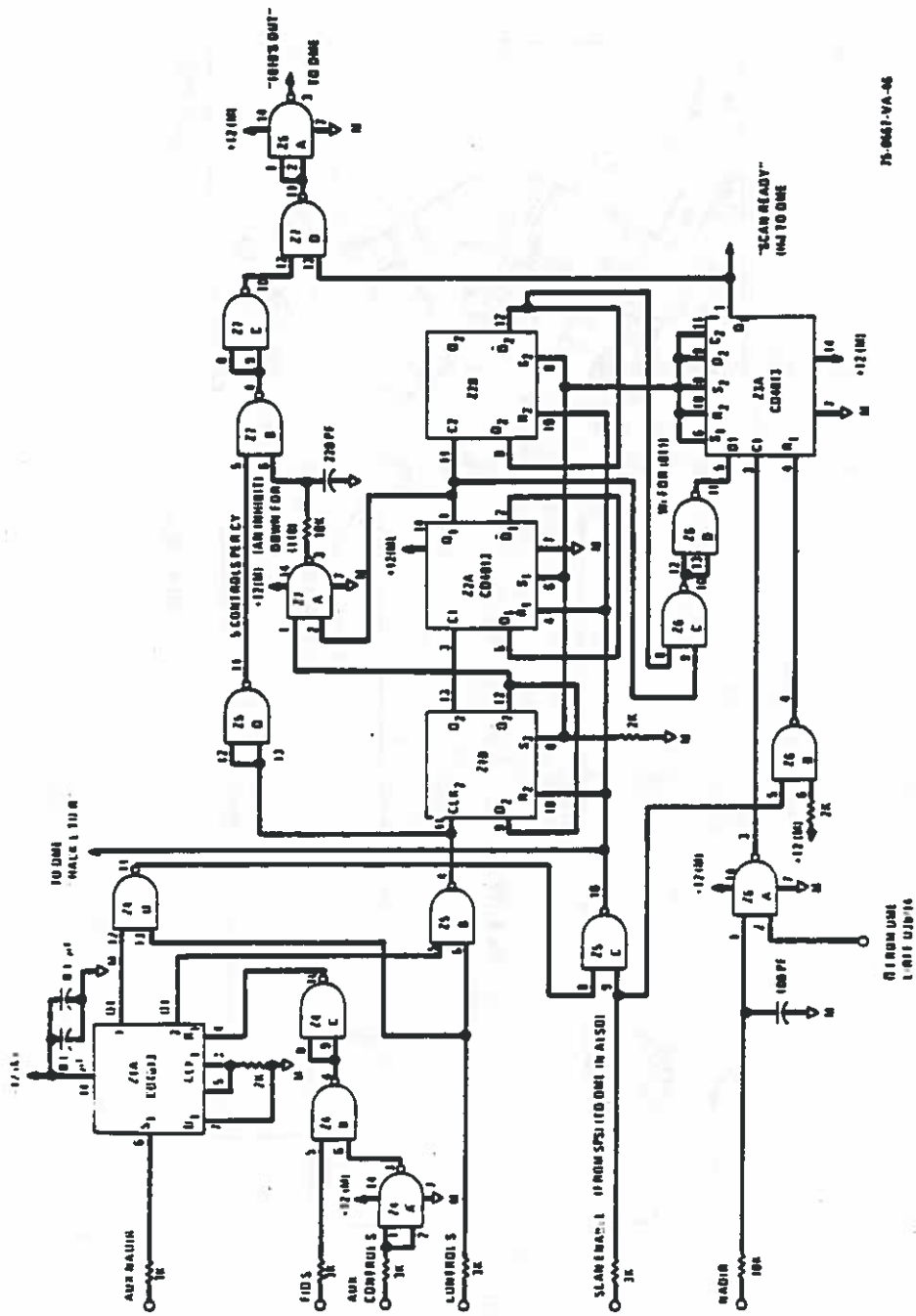


Figure 2.1.5-9. One ENPA to DME Decoder

a control pulse on facet 7 (one FID to the right side of nadir) comes in, it goes through Z4D and Z5C (when scan enable is enabled). This is the hack control pulse from facet 7 on the left-to-right (only) direction. Since there is no control pulse from facet 9, no hack can be given on the first facet to the left side of nadir. Then Z1A is reset by the very next FID pulse that does not have an auxiliary (wide) control pulse with it. Thus Z1A is only enabled from facet 8 to facet 6 in going from left to right (DOS = 1) and is only enabled from facet 8 to facet 9 in going from right to left (DOS = 0). There are no control pulses on facets 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, 13, or 14. There are FID pulses from every Facet. Thus the hack left-to-right pulse is stripped out and sent to the DME for resyncing of its left/right flip-flop if it every gets out of sync.

The Q side of Z1A inhibits the hack left-to-right pulse from passing through Z5B, so that only five of the six Control pulses (for full amplitude) per scan cycle are fed to the three flip-flop counter Z1B, Z2A, and Z2B. This counter is reset to zero at hack left-to-right. Gates Z6C and Z6D decode the counter for a count of five. When the scan amplitude has built up enough to give two control pulses on the right (+Z) side and two control pulses on the left (-Z) side plus the hack right-to-left (the fifth control pulse), the Z3A one bit shift register data input line goes high. The Q from the DME left/right flip-flop is high for the +Z side so the trailing edge (fall) of the nadir pulse going from left to right causes the gate Z6A output pulse to rise and clock the Z3A input data to provide scan ready as its output. If the scan amplitude falls below the 1018 pairs on either the left or right side of scan, then less than five gated Control pulses are counted, the decoding goes false, and scan ready is removed at the next left-to-right Nadir.

Of the five control pulses per cycle at Z5D output, it is necessary to inhibit the third one (the hack right-to-left pulse) in the 1018's OUT data stream to the DME. This is done by decoding the three flip-flop counter state with Z7A, inhibiting the Z7B pin 6 after a count of two, and releasing the inhibit after a count of three. The +Z side 1018's are the first two of the four control pulses per cycle remaining out of Z7C and the -Z side 1018's are

the last two of the four remaining control pulses. The four 1018 pulses out to the DME are also by the Z7D gate inhibited until after scan ready is present.

2.1.5.2 Scan Drive

The scan drive, with minimal power expenditure, produces a sinusoidal scan motion with time whose amplitude and frequency are 57.85° and 5.94 Hz respectively. A spring/mass torsional pendulum system provides torque; sinusoidal scan motion. Four flat, spirally wound springs provide torque; one end of each spring is attached to the fixed structure and the other end is attached to the oscillating shaft. Matching the spring constant and the angular inertia of the oscillating assembly provides the proper, oscillation frequency. The system is mechanically resonant, so the frequency stability and low power are inherent, and the scan drive must only supply energy to overcome damping force losses in just the right amount to maintain amplitude stability.

Energy is imparted to the oscillating scanner by pulsing a dc torque motor twice each cycle of the scanner with a pulse whose width is controlled in a feedback loop based on scan amplitude.

The motor is a brushless, limited angle, dc torque unit modified to function within the constraints of the OLS oscillating scanner assembly. The permanent magnet rotor of the motor has been made slightly smaller to provide a 0.050 inch gap between the rotor and stator to allow shaft clearance during caging and vibration. The motor input power is a pulsewidth-modulated 28 volt dc peak amplitude pulse, symmetrical around the Nadir position of the scanner for most efficient use of power.

The Drive Motor Electronics (DME) is a control system designed for an electro-mechanical torsion oscillator device with high Q. The frequency of oscillation is tuned to the nominal 5.94 Hz by adjusting the torsional inertia. A block diagram of the DME is shown in figure 2.1.5-10.

Representative waveforms during full-amplitude operation are shown in the timing diagram, figure 2.1.5-11.

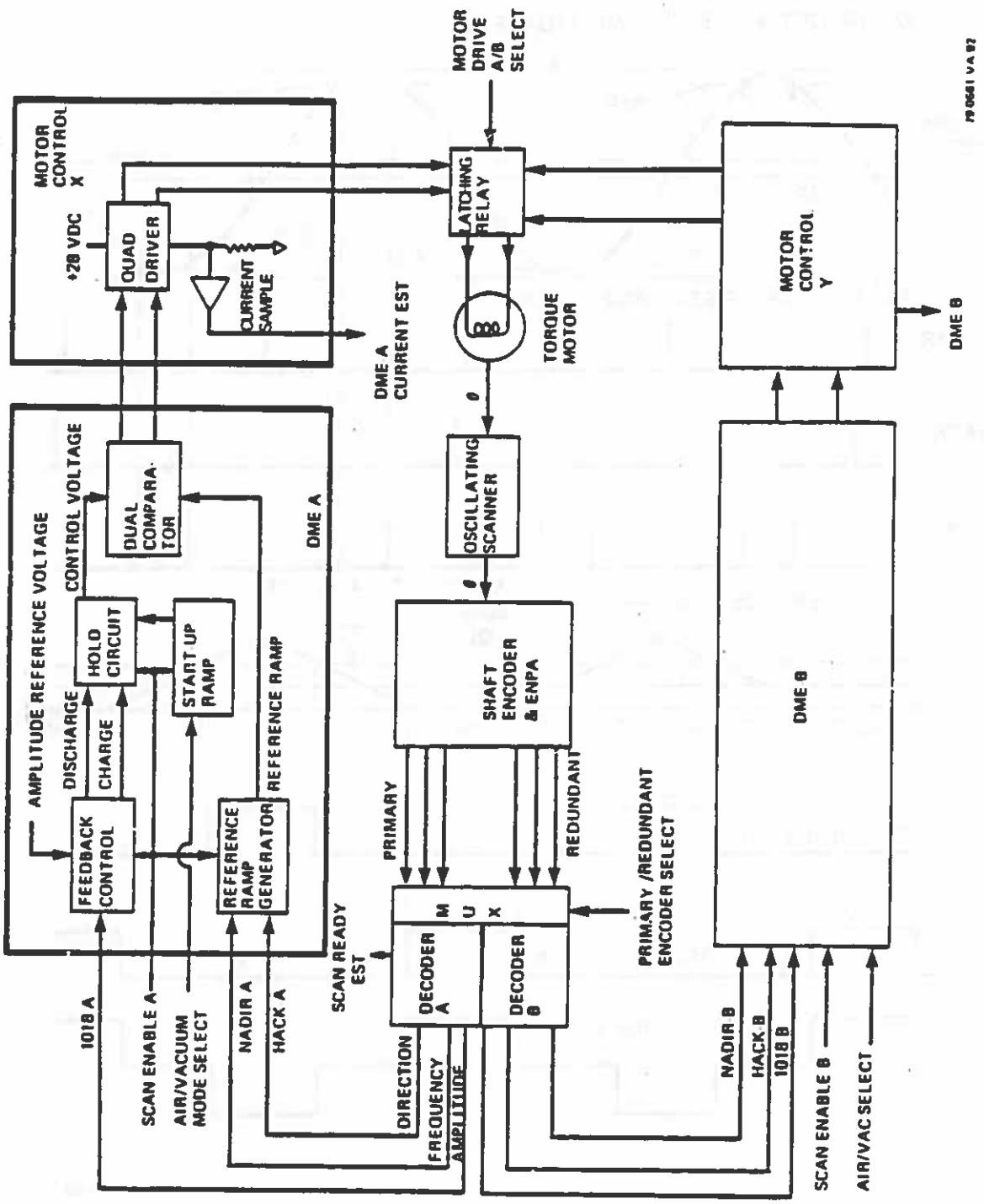


Figure 2.1.5-10. Scan Drive Block Diagram

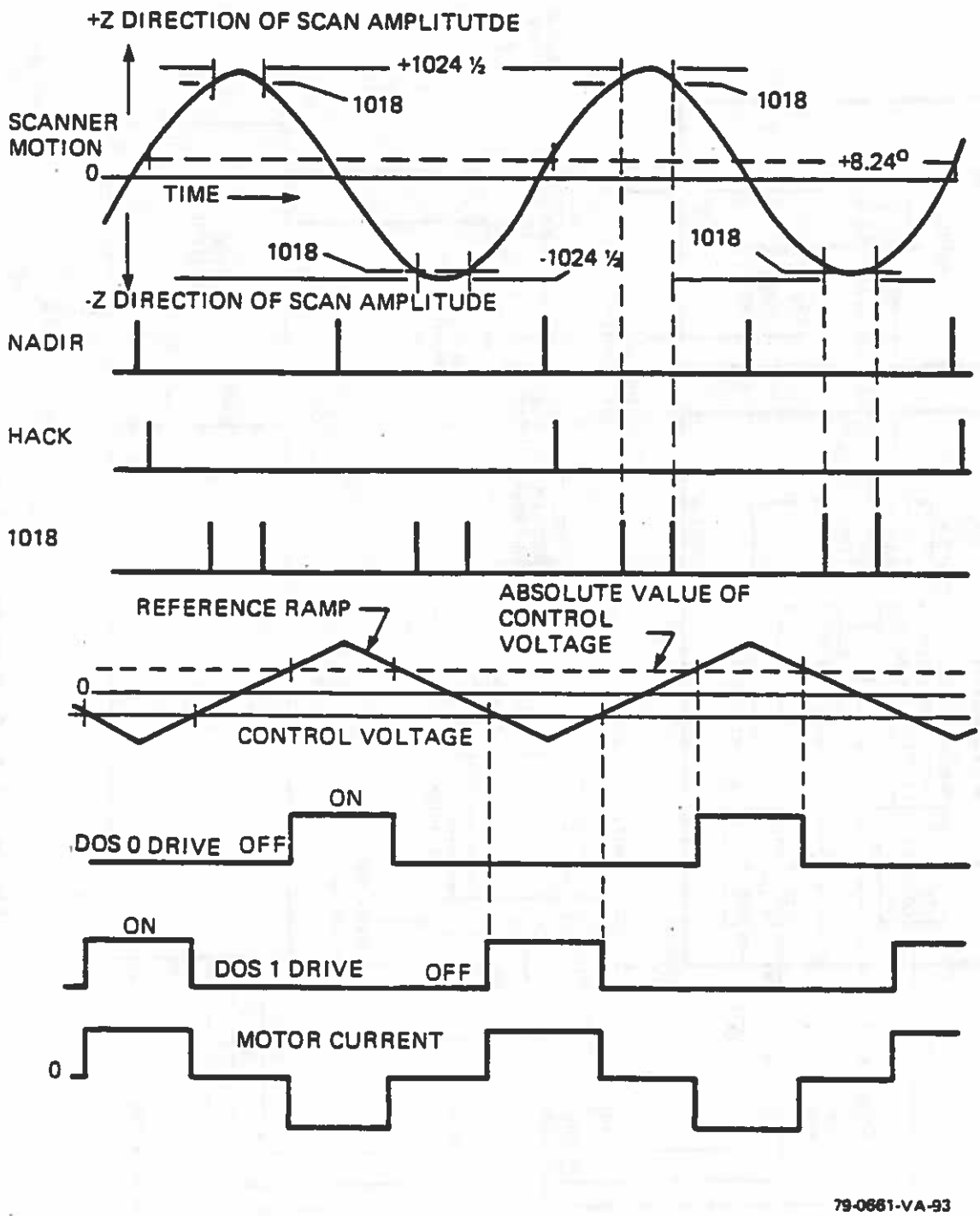


Figure 2.1.5-11. DME Timing Diagram

The "Reference Ramp generator" and "Dual Comparator" together make up a pulsewidth modulator capable of generating a drive pulse symmetrical about scanner nadir. The width of the drive pulses is controlled by a dc voltage applied to the Dual Comparator. Two lines are used to supply the torquer with pulses of alternate polarity current so that the scanner is always driven in its direction of motion. An "H" configuration drive circuit located in the Power Supply convert the DME output to the 28 volt, high current pulses of alternating direction required by the torque motor.

The output voltage of the Start-Up Ramp circuit sets the maximum available pulsewidth availabe to drive the motor. At scanner turn-on, the Start-Up Ramp output voltage changes linearly from a voltage representing approximately zero pulsewidth, to a final value over a period of approximately 90 seconds. The final value is switchable by the AIR/VACUUM Mode ground command to correspond to 29 $\pm$3 msec. maximum available pulsewidth in vacuum, or 49 $\pm$3 msec. maximum available pulsewidth in air. When full amplitude is reached, scanner feedback pulses from the decoder are processed in the "Feedback Control" and "Hold Circuits" in the DME to vary the control voltage as required to maintain proper scanner amplitude. Feedback from the scanner is by means of the optical shaft encoder. Three lines from the encoder output are routed through the ENPA to DME decoder logic to the DME.

Nadir - A pulse produced each time the scanner crosses its zero reference (Nadir) position, used to clock the Reference Ramp Generator.

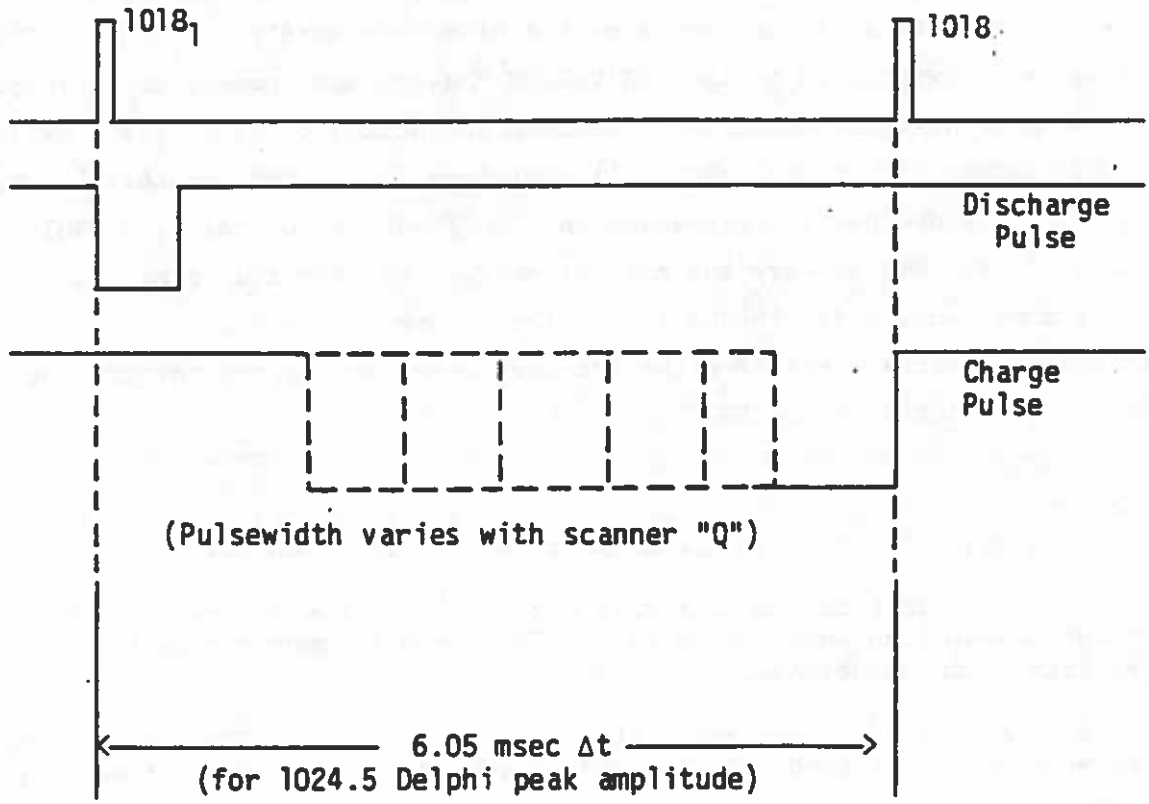
Hack - A pulse produced only once each cycle of the scanner, providing direction-of-scan information to the DME. Used to synchronize the Reference Ramp Generator.

1018 - A pair of pulses generated a each end of scan. The time interval between pulses of each pair is used by the DME as a measure of scanner amplitude.

Scanner amplitude control as accomplished in the DME is described below. At each end of scan, the time interval between 1018 pulses is detected and converted to a dc voltage in the Feedback Control Circuit. This is compared with an Amplitude Reference Voltage corresponding to the desired scanner amplitude. Any difference between these two voltages is integrated to produce an error signal which then generates the Charge Pulse for the Hold Circuit.

The Discharge Pulse is a 0.5 ms wide pulse beginning at the 1018 entering overscan. The Discharge Pulse initializes the Hold Circuit to a voltage determined by the Start-Up Ramp readying it for the new information to follow. The Charge Pulse changes the control voltage to a new value as determined from the amplitude feedback information. This control voltage is held by the Hold Circuit for use until the scanner swings back toward Nadir at which time the appropriate width drive pulse is generated. The relationship of the Charge Pulse, Discharge Pulse and the 1018's are shown on the following figure.

End-of-scan timing detail:



The motor drive is controlled to keep the 1018 to 1018 time interval equal to that required to balance the Amplitude Reference Voltage. The integrator in the loop provides very high dc gain which yields operation with zero amplitude error.

Selection of DME A or back-up DME B is made by ground command. A pulse placed on a discrete Motor Control command line switches magnetic self-latching relay K1 between DME A and DME B.

Driver motor average current telemetry is provided by an EST signal from each DME. A 1.82 ohm current shunt resistor measures the quad driver return line current and is amplified by a differential amplifier stage having 4.016 gain. The EST scale factor is 137 mA per EST volt. The EST circuit also provides approximately 0.34 second time constant for smoothing the drive motor current pulses.

2.1.5.3 Image Motion Compensation

Because of the sinusoidal scanning motion of the OLS, received data without image motion compensation would be distorted by standard raster scan receiving equipment in that regions near the end of scan would be alternately compressed and expanded along track. Image motion compensation (IMC) has therefore been mechanically incorporated into the scanner optics.

IMC is accomplished by swinging mirror M3 plus and minus 0.4 milliradian in the along track direction at a rate of 1 cycle for each scan of the telescope, or twice the telescope scanner frequency. The locus of the line of sight with IMC is shown as the heavy line in Figure 2.1.5-12. The light line represents the line of sight locus without IMC. For proper operation, M3 must be pulled to the end of its travel while the telescope is at one end of scan, then pulled through its sweep as the telescope performs one scan line. When the telescope reaches the opposite end of its scan, and while it is reversing direction, M3 must be returned rapidly to its original position in preparation for the next scan of the telescope. Correct movement of M3 is accomplished with the electromagnets acting on the steel M3 control arm.

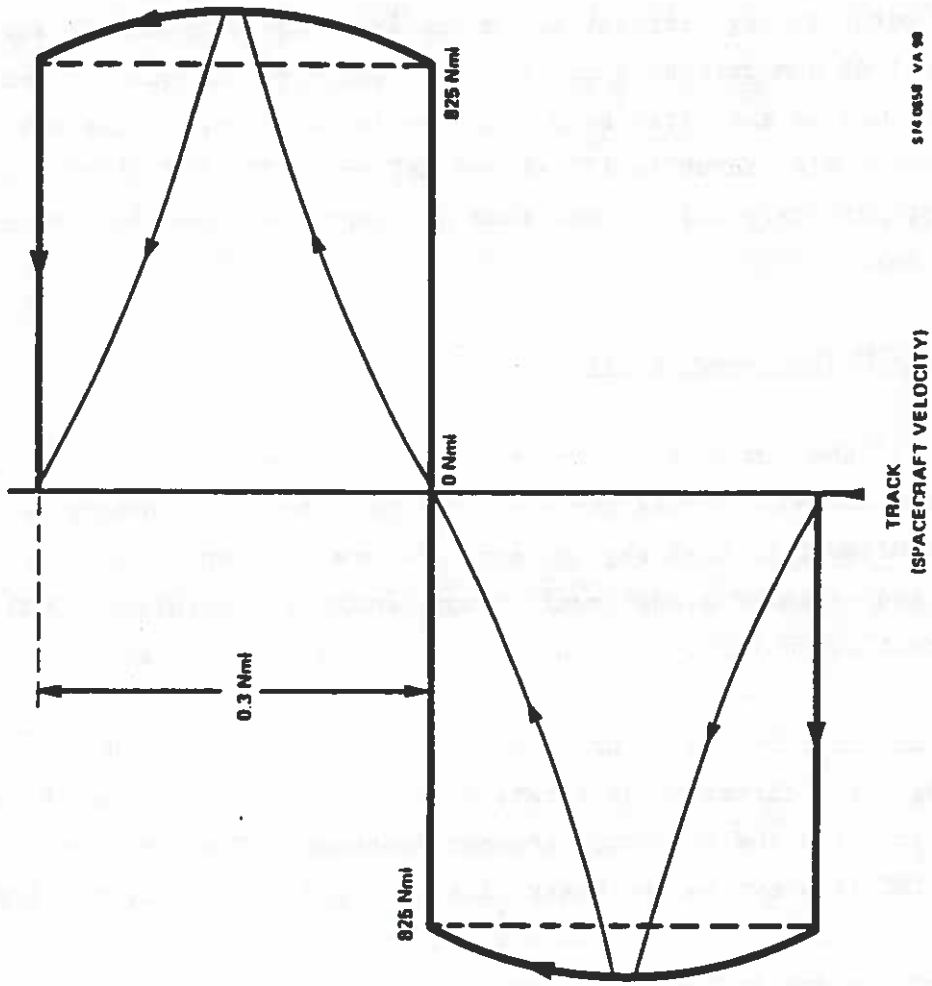


Figure 2.1.5-12 Image Motion Compensation

The drive circuitry for the electromagnets, shown in Figure 2.1.5-13, is described below. The telescope scanner's optical shaft encoder via the digital processor supplies two logic signals to the IMC electronics to synchronize the M3 motion with the oscillating telescope.

Nadir: a positive pulse generated each time the scanner crosses its center position. The time between nadir pulses is approximately 84 msec.

996 pulses: also known as SOAD/EOAD (start of active data/end of active data), occur in pairs at each end of telescope scan. They indicate to the IMC that the telescope has completed a swing and is turning around. It is during this time that M3 must be quickly returned to its starting position.

Nadir is used to reset flip-flop U1, ensuring that the TP4 waveform is at a logic 1 during the time M3 should be scanning. The first 996 pulse at the end of telescope scan sets flip-flop U1; the 2nd 996 pulse resets it again. This produces a logic zero at TP4 during telescope turn-around time, when M3 must be returned to its starting position.

The rectangular waveform at TP4 drives an integrator to produce a ramp suitable for driving the IMC coils. The output of the integrator is split into positive and negative components by two diode clipping networks that provide opposite polarity drive signals for the two IMC coils. DC feedback is used with the integrator to modify the positive and negative slopes of the output ramp and maintain symmetry about zero volts. An emitter-follower output stage is used to drive each IMC coil.

A switching network is used to select the direction of M3 scan by driving one pair of two pairs of output driver transistors. This is necessary to permit proper image motion compensation for a S/C moving in either the +Y or -Y direction forward. For a "0" command Q3 and Q4 are used; for a "1" command Q2 and Q5 are used.

The switching is ground commandable by a CMOS-compatible logic control input signal at pins 24 and 64 of the IMC board. The switches are able to

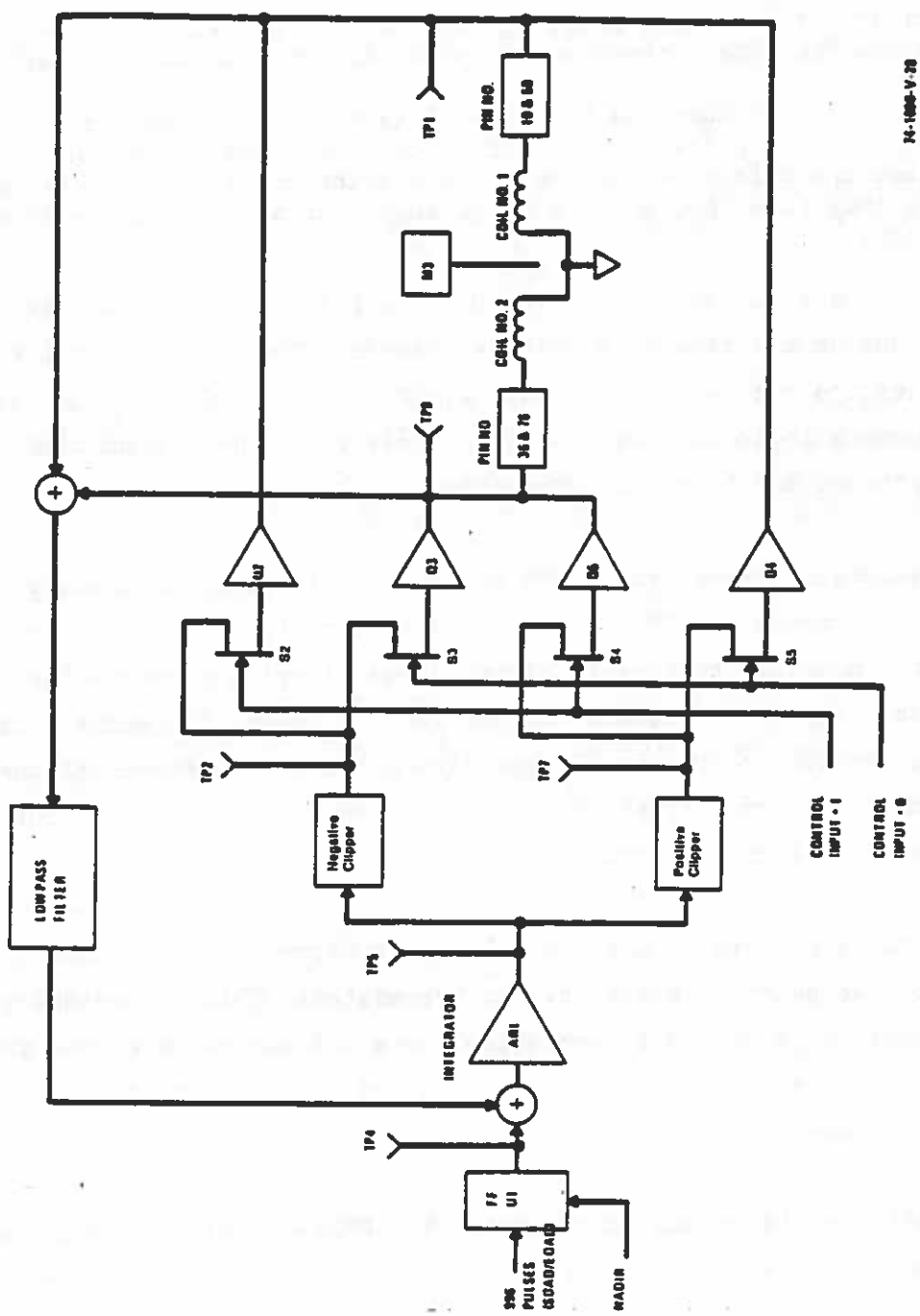


Figure 2.1.5-13 IMC Block Diagram

interchange the drive signals to the two coils, thus scanning M3 in its opposite direction. The system is set for +Y or -Y forward direction by loading the proper IMC command word into the OLS constants memory.

2.1.6 System Control

The operational program, OLSP, provides data management and control for the following resources:

4 primary tape recorders for stored data
4 output channels for real time data or stored data playback
4 data transmitters
2 stored data formatters
1 real time data formatter
primary sensor
12 mission sensors

The OLSP routes data through the system via commands (real time or stored) and provides interlocking logic to prevent accessing busy resources or mixing data (such as trying to record simultaneously 2 different data types on the same tape recorder).

In addition there are commandable functional redundant resources for many of the above (formatters, output channels) which can be used in case of primary resource failure.

2.1.6.1 Configuration

The flight software program (OLSP) resides in a 16K memory which is controlled by a space qualified 16-bit on-board processor. The system also contains a redundant on-board processor and 16K memory whose main purpose is to serve as a backup but which can also operate at the same time as the main computer system, accessing the same I/O, in order to share the processing load or to run general system health diagnostics while the primary system is performing its mission.

The software was developed on a Univac 1100/82 host computer using a cross-assembler, loader, and on-board processor simulator. A special simulator of the OLS was written and used to check out the flight software before system integration.

A loader program resides in ROM memory which can load any uplinked program into any or all of RAM memory. A loadable program memory has several advantages: 1) software errors which may be discovered on-orbit can be easily corrected, 2) refinements to existing algorithms or new algorithms can be tried, 3) program can be reassembled and reloaded to bypass failed portions of memory. Also existing in ROM memory is a checksum program which computes and downlinks checksums on all memory blocks so that program loads can be rapidly verified.

Other programs in ROM are a simplified processor diagnostic used to determine the health of the processor, a telemetry gathering program which receives and stores S/C serialized 2K-bit telemetry during any orbit when the main program is not executing, and a data base of tables such as sine and arc sine tables.

The operational flight software program (OLSP) which is loaded into RAM by the program loader receives real time commands from the ground. These commands are decoded and executed if they meet the correct criteria. The command execution, in general, invokes certain processing, selects operational modes and equipment configuration, and sends control information to up to 40 devices within the signal processing subsystem (SPS).

When the OLS is out of the station circle, real time commands are not possible. A stored command table is provided in order to execute commands during these orbits. Each command has a time tag which the OLSP uses to determine when to execute the command. The commands are the same ones used in real time commanding and the same software executes the commands.

Two stored command tables are provided. One references its time tags to the spacecraft's (S/C) elapsed time clock, the other stored command table is cyclic on an orbital basis and is referenced to a derived orbit clock.

These tables along with special constants and data tables which may require changes from time to time are changeable via real time memory load commanding.

2.1.6.2 Processor

The OLSP provides timing pulses for formatting the data. These pulses occur at set scan angles and include wow/flutter enable, start and end of active data, and line sync pulses.

Gain prediction and selection is made using location data from the S/C and stored gain tables. The selection is made by connecting a sensor (one of four) to a variable digital gain amplifier (VDGA), setting the gain in the amplifier, and selecting a ramp at which the VDGA should increment. Using this method a large dynamic range is achieved.

Timing pulses and controls to the mission sensors via the special sensor formatter provide the means for mission sensor sampling and data collection which is placed in the primary data.

The OLSP receives and buffers S/C serialized 2K-bit telemetry which is placed in the stored data by the stored data-smooth formatter. Any value in the OLSP memory can be placed in the CPU telemetry section of the stored telemetry. These CPU telemetry channels are reassignable via commands. A basic CPU telemetry table is provided which provides such information as:

scanner amplitude, period, and offset
primary recorder location counters
main and orbit stored program status
transmitter status
location data
gain mode

program version and revision
initialization count
error indications

The program decodes and executes both real time and stored commands. The types of commands are:

gain control, segment selection, gain mode
real time data collection, data type
stored data control (record and playback), data type
transmitter to channel select, transmitter power
primary sensor control, encoder simulator control
mission sensor commands, loads, and control
redundant function control
orbit clock set
stored program control
memory loads and dumps, CPU telemetry changes
dynamic programming commands
status dumps

The OLSP makes various syntax checking and parity checking on commands. In additon some hardware checking is done including a processor diagnostic and program memory checksums. Any errors encountered are coded along with time of occurrence and stored in an error table which can be dumped. A telemetry bit is set to provide notification of error table entry.

The program can be commanded to load any portion of its RAM memory without interrupting the primary data. The primary purpose is to change the stored constants or stored command tables; however, the program itself can be changed or patched with a memory load command. Any part of the program RAM or ROM can be dumped on command. Various status dumps can be commanded without having to know the absolute addresses of the status information stored in memory. This includes such information as main program, orbit program, stored constants, stored tables, checksum error table, system error table, processor status, etc.

The OLSP also provides timing pulses and controls for multiplexing data into different data streams called primary data. The primary data can be either real time or stored. The program selects the data type according to

command where the stored data smooth is LS and TS data. The stored data fine can be LF, TF, or interleaved LF and TF data. Real time data is multiplexed LS/TF or LF/TS data. Other types of data which are multiplexed into the primary data are S/C 2K-bit telemetry, mission sensor data, direct mode data, and ancillary data consisting of calibrations, elapsed time count, offset, and location data.

2.1.7 Survivability Features See BVS 2526, this BVS forms a classified appendix to the Technical Operating Report.

2.2 OLS Physical Description

The 5D-3 OLS is described physically in the subparagraphs which follow. The OLS physically consists of the fourteen equipment units listed below and shown interconnected (except for the GSSA/DOC) in Figure 2.2.0-1, 5D-3 OLS System Equipments.

SSS - Sensor Subsystem
GSSA/DOC - Glare Suppression System A/Deployable Optics Cover
SPS - Signal Processing Subsystem
SPU - Special Processing Unit
PSU - Power Supply Unit
OSU - Output Switching Unit
BBs - Encrypters (3)
DTRs - Digital Tape Recorders (4)
CHA - Cable Harness Assembly

Figure 2.2.0-2 is a photograph of most of these equipment units. The DOC, BB's and CHA are not shown.

The location of each of the OLS assemblies on the spacecraft is shown in Figure 2.2.0-3, Spacecraft Placement of OLS Assemblies. The GSSA/DOC mounts on the SSS which mounts on the spacecraft Precision Mounting Platform (PMP). The rest of the OLS units mount on the internal panels of the spacecraft Equipment Support Module (ESM).

There is no direct correspondance between the funtional blocks and physical units but there is correlation as given in table 2.2.0-1. A more detailed description of the physical location of functions is given in the family tree figures in the subparagraphs of this section.

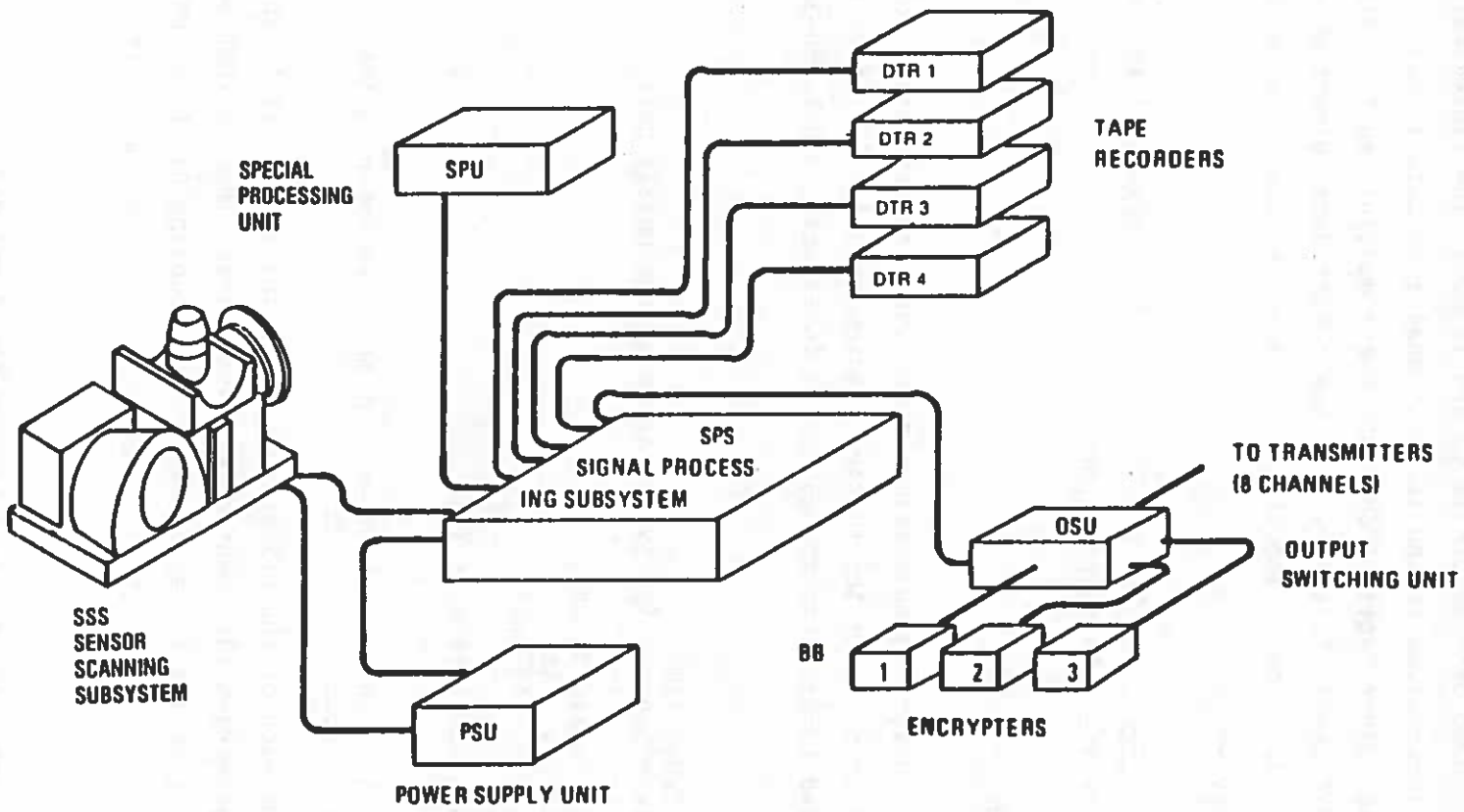


Figure 2.2.0-1. 5D3 OLS System Equipments

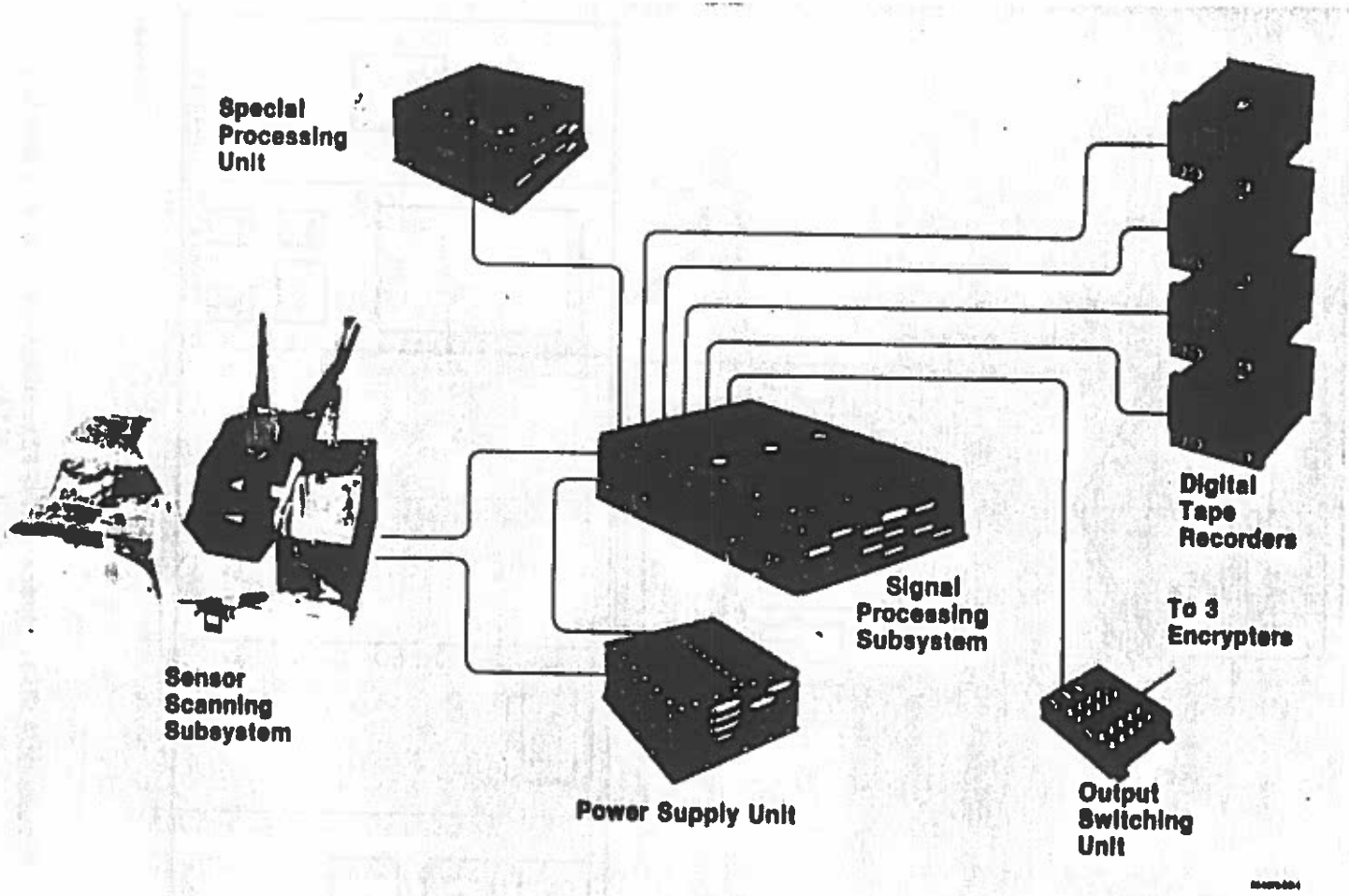


Figure 2.2.0-2. 5D3 OLS System

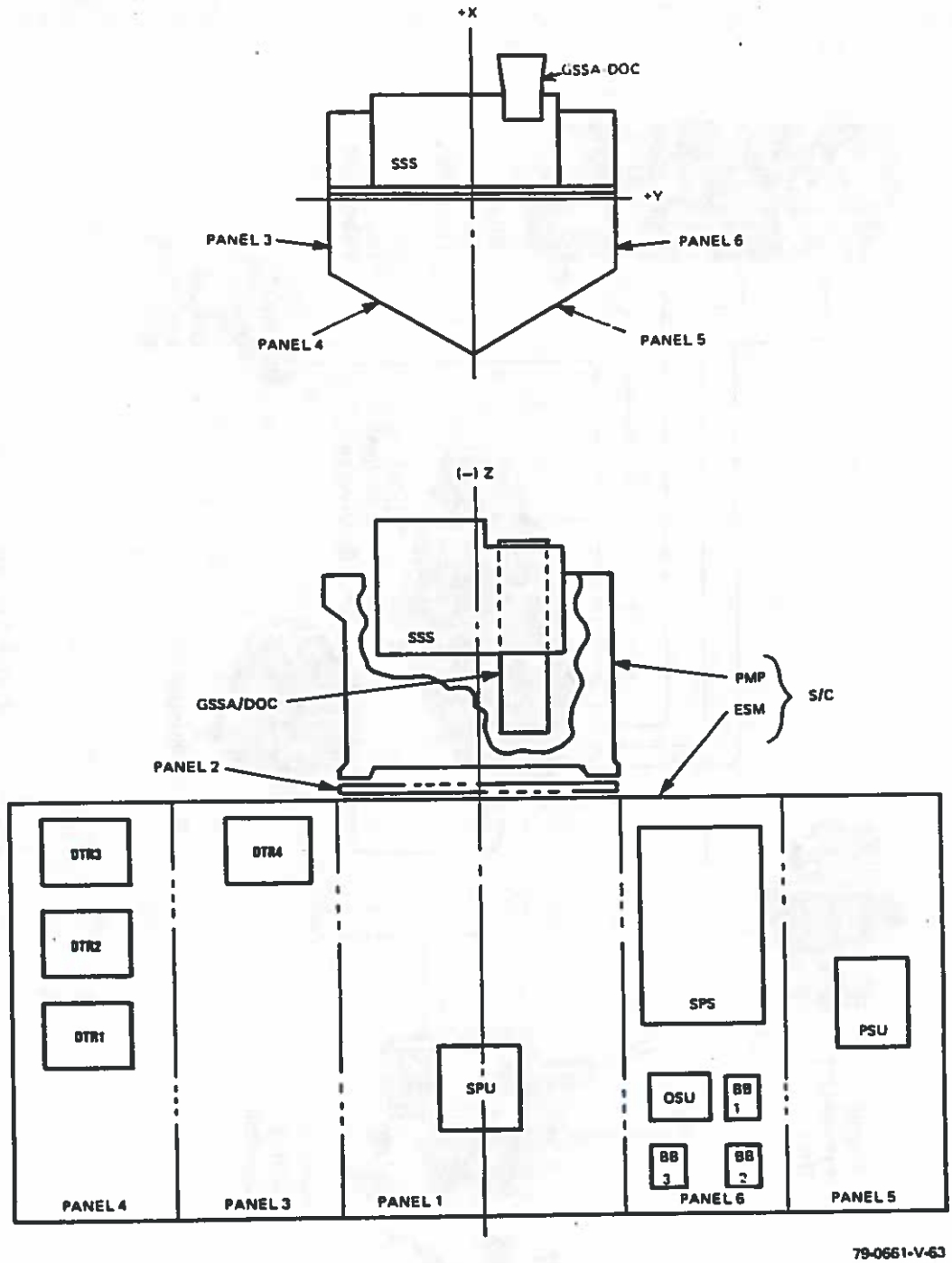


Figure 2.2.0-3. Spacecraft Placement of OLS Assemblies (S11 - S14)

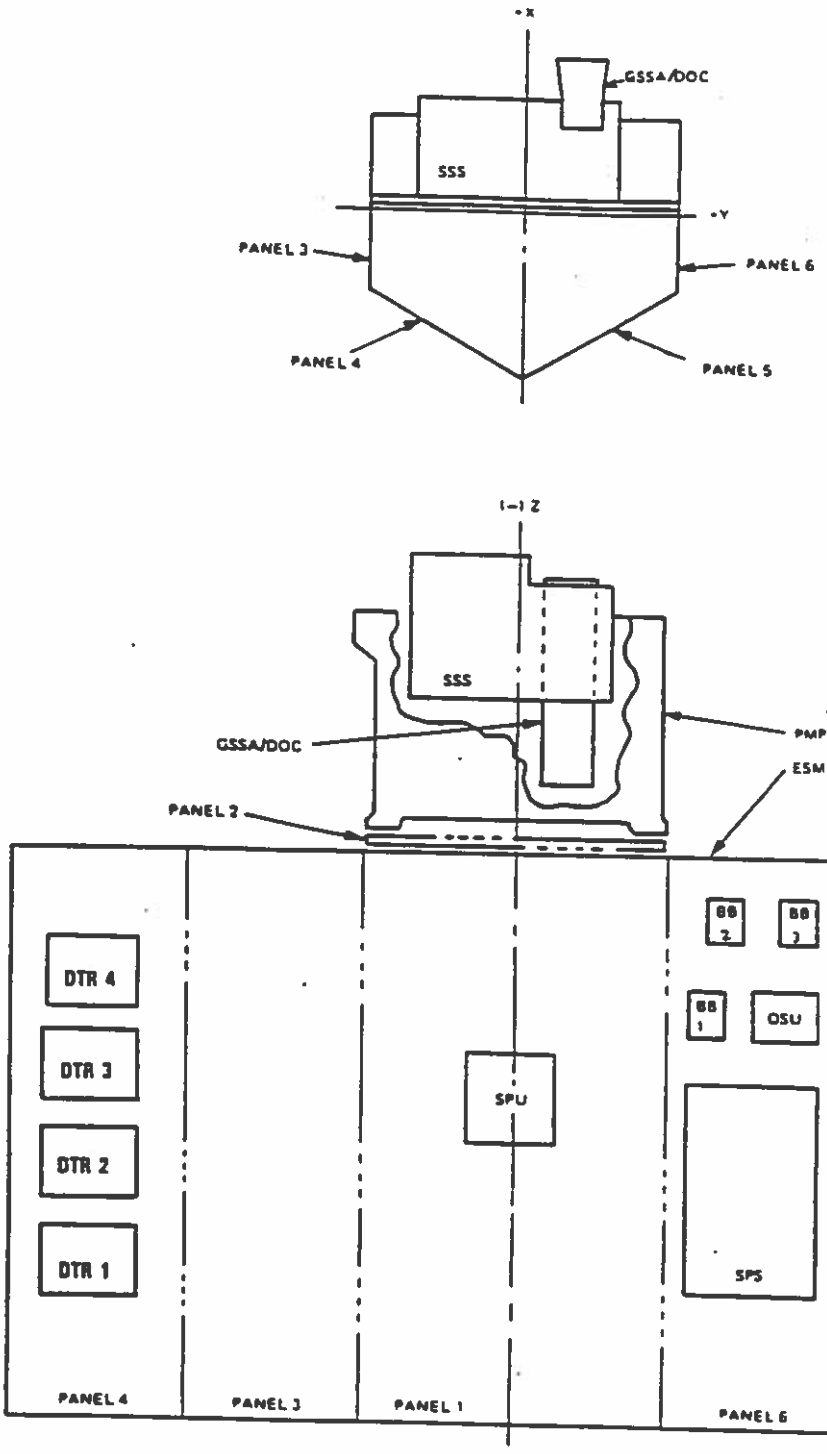


Figure 2.2.0-3a Spacecraft Placement of OLS Assemblies
(OLS 16 & up)

Table 2.2.0-1. Location of Functional Blocks

Physical Unit	Functional Block
SSS	Optics Glare Suppression (Portion) Detectors Analog Signal Processing (T Preamp; L Channel excluding Filters) Power Supplies (HVPS) Scanner Monitor & Control (Encoder, ENPA, Motor)
GSSA/DOC	Glare Suppression (Portion)
SPS	Processor Operational Program Memory Input/Output Control Spacecraft Interface Sensor & Gain Control Output Data Multiplexer (Portion) Encoder & Wow/Flutter Processing Special Sensor Control Formatters (SDF & SDS portion)
SPU	Formatters (RTD & SSP portion)
PSU	Power Supplies (Main) Analog Signal Processing (L Filters; T Postamp through T Filters) Scanner Monitor & Control (Decoder, DME, Power Switch, & IMC Drive)
OSU	Output Data Multiplexer (Portion)
BB's	Data Security
DTR's	Data Storage

2.2.1 Sensor Scanning Subsystem (SSS)

The Sensor Scanning Subsystem (SSS) integrates the optical system elements, the scanning and drive system elements, the detectors (with major portions of the associated electronics), the calibration sources, and thermal control elements on a single stable main structure. The telescope of this unit scans the earth scene and provides three channels of information for the OLS system. Figure 2.2.1-1 shows a family tree of those basic elements which are integrated to form the SSS assembly. Figure 2.2.1-2 shows the physical arrangement of the elements on the main structure. The thermal blanket is not shown in figure 2.2.1-2 but is in figure 2.2.0-2. It surrounds the entire unit except for the oscillating assembly aperture and the mounting surface. Figure 2.2.1-3 is a photograph of the SSS and annotates several of the principle elements. The SSS mounts on the spacecraft precision mounting platform (PMP) as shown in Figure 2.2.0-3.

The SSS is 30.3" long by 14.4" wide x 13.6" high and weighs 55.3 pounds.

A description of the SSS elements is provided in the following paragraphs.

2.2.1.1 Main Structure

The main structure is a lightweight magnesium weldment which is designed to be a rigid "optical bench". This structure provides for accurate support for all functional elements and incorporates a three point spacecraft mounting interface that provides accurate alignment with minimum distortion due to mechanical and thermal expansion differences.

2.2.1.2 Oscillating Assembly

Figure 2.2.1-4 shows the physical arrangement of this statically and dynamically balanced assembly which contains the telescope and all other oscillating optical elements which constitute the integrated reflector assembly. Major elements of the oscillating assembly are fabricated from beryllium which provides high strength, low weight, and excellent thermal conductivity. Stainless steel shafts at each end of the assembly provide for

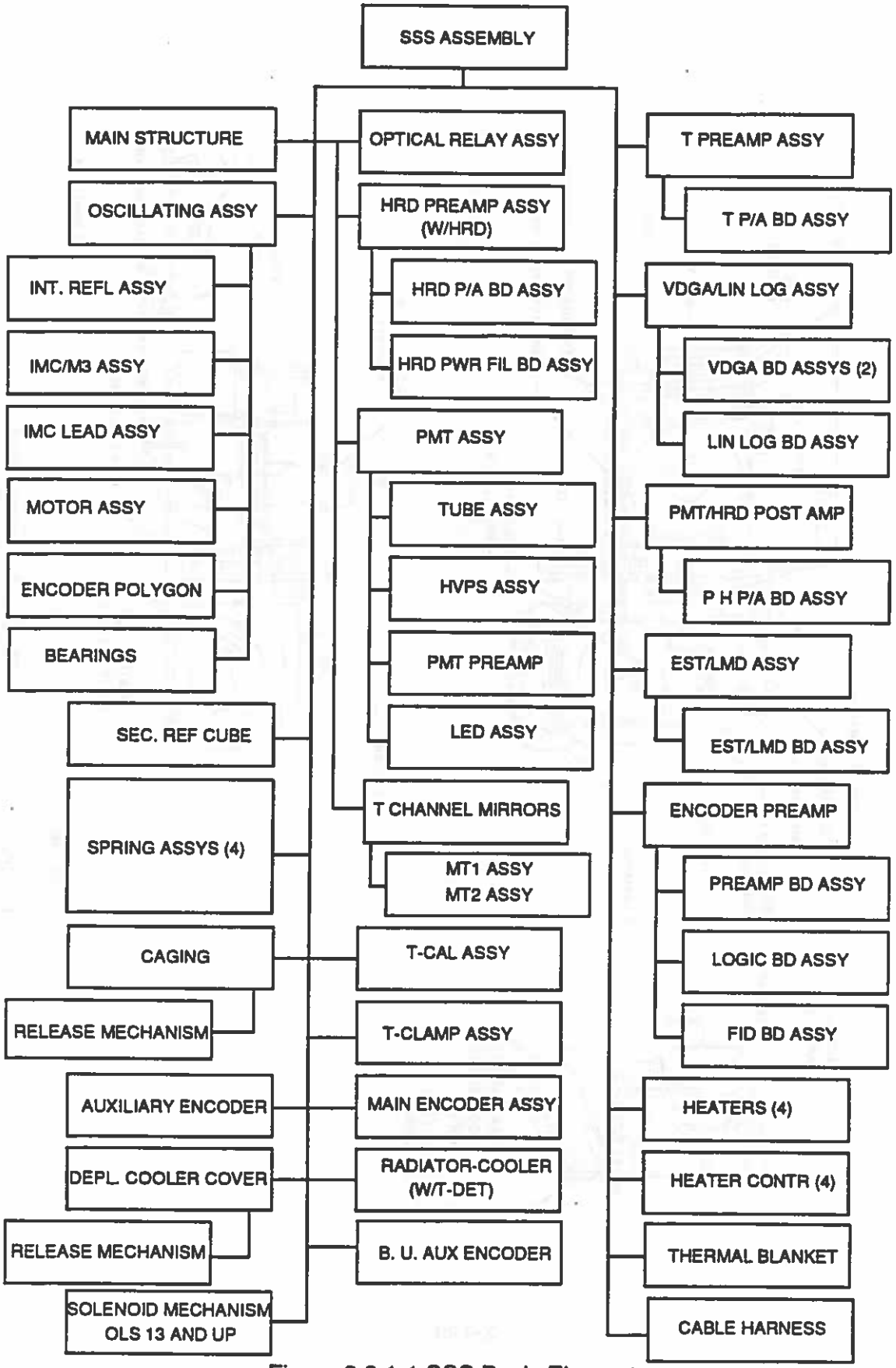


Figure 2.2.1-1 SSS Basic Elements

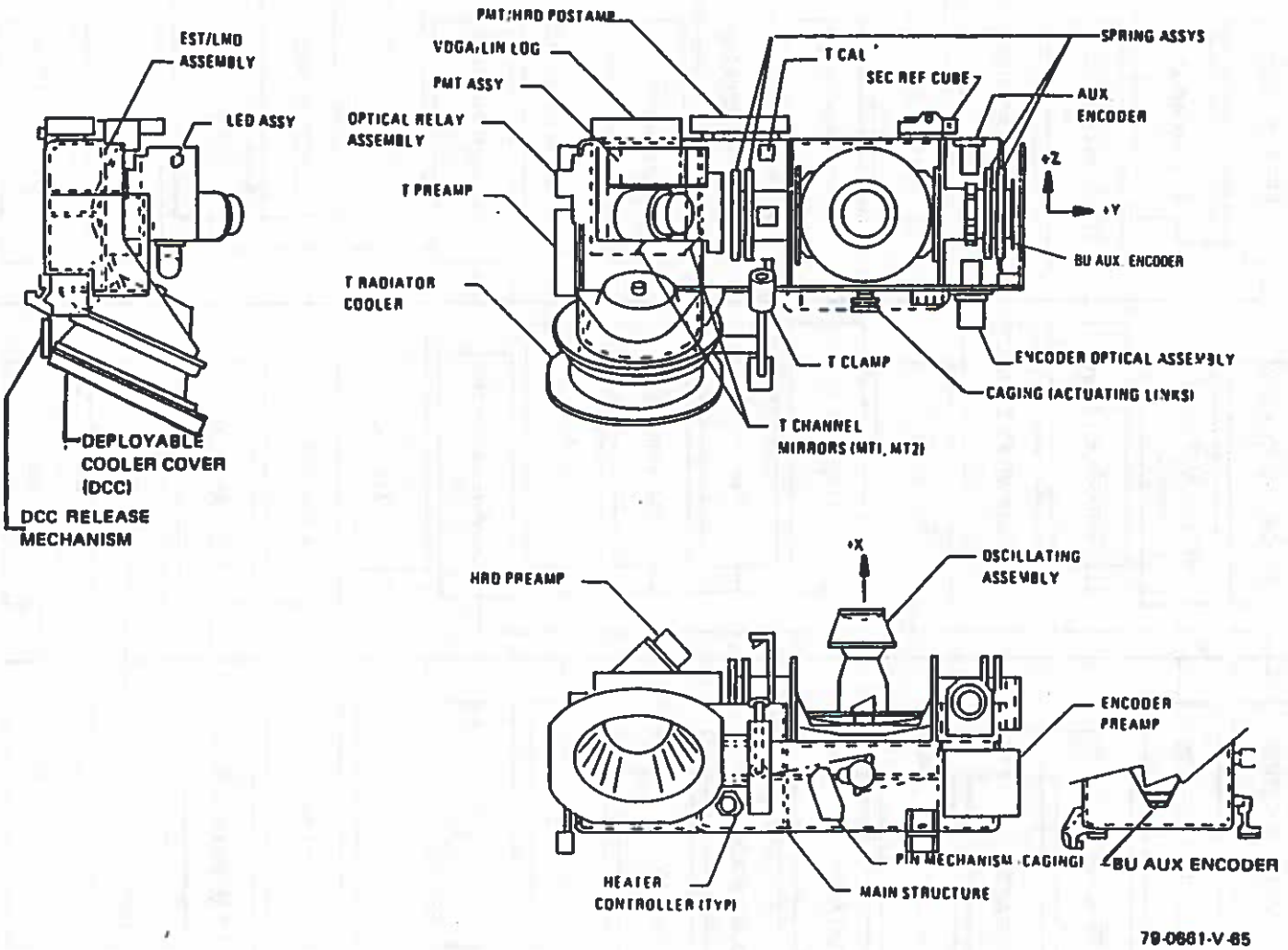


Figure 2.2.1-2 SSS Physical Arrangement

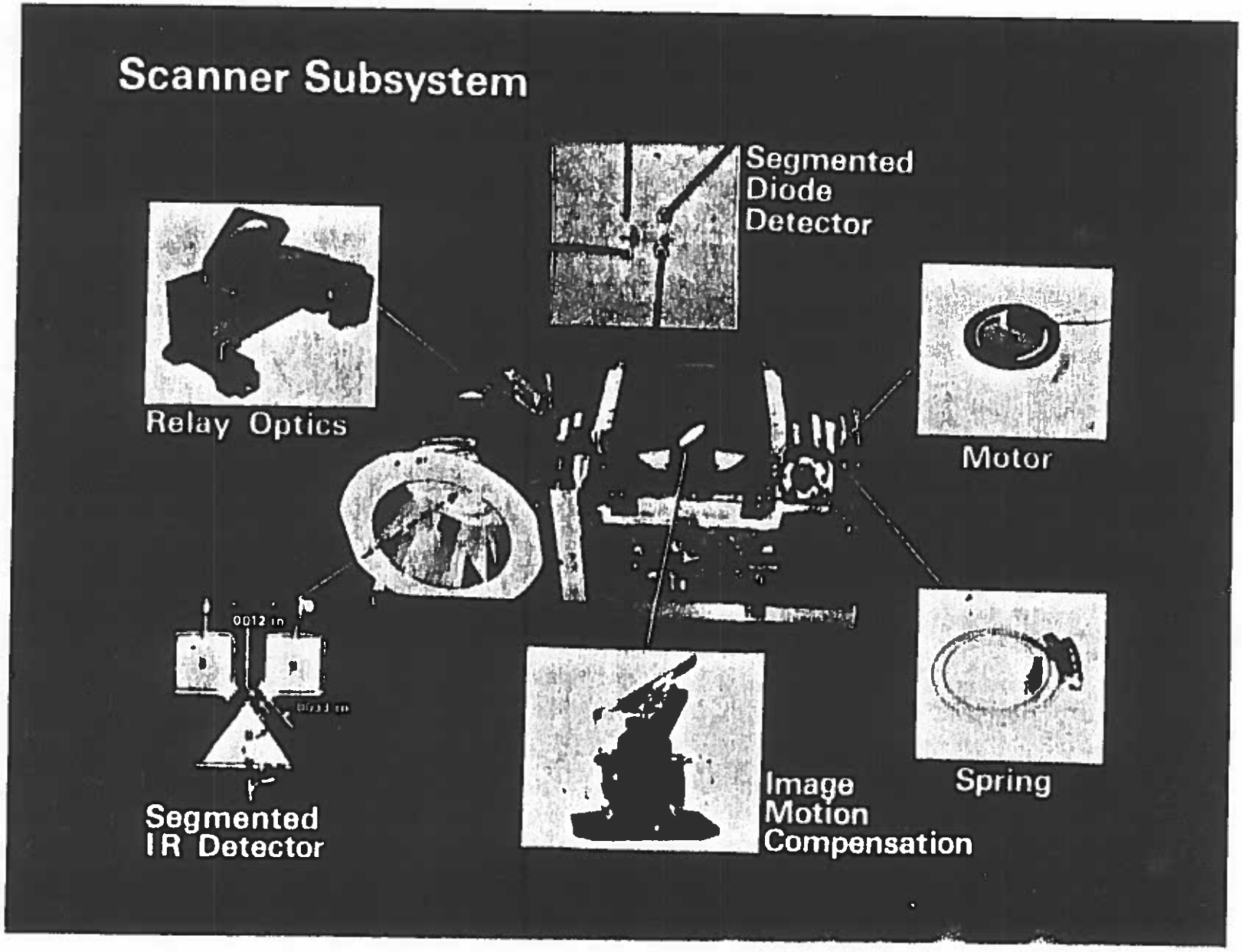


Figure 2.2.1-3. SSS Assembly

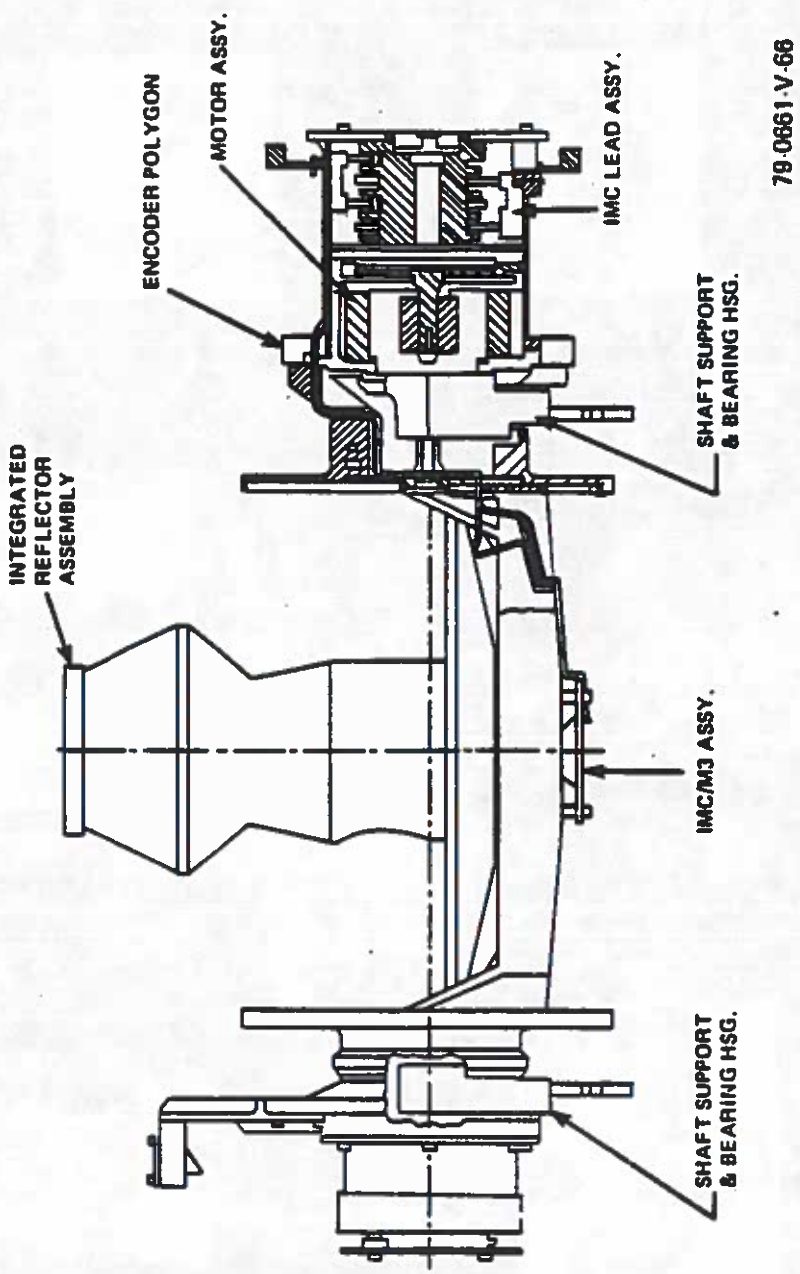


Figure 2.2.1-4. Oscillating Assembly

mounting a pair of small preloaded bearings. Each bearing is housed in an assembly which provides a lubricant reservoir and labyrinth seals. The housings are attached to the main structure at precision machined locations. One housing has a slip joint to prevent distortion due to thermal expansion differences between the oscillating assembly the the main structure.

Figure 2.1.1-1 shows the schematic arrangement of optical elements, M1 through M5, which are contained in the integrated reflector assembly. M3 is supported on a spring pivot and is driven to provide image motion compensation (IMC) during the scan. Drive signals for the IMC are brought out from the oscillating assembly to the fixed structure through four small beryllium-copper spiral springs in the IMC Lead Assembly.

The oscillating portion of the optical encoder (encoder polygon) is mounted to the oscillating assembly and works in consort with other parts of the encoder which are described in paragraph 2.2.1.5.

A torquer type motor mounted near one end of the oscillating assembly provides power for starting and sustaining the oscillating rotation. The rotor is a permanent magnet attached to the oscillating shaft and the stator with windings is attached to fixed structure.

2.2.1.3 Springs

Four spiral wound springs in combination with the inertia of the oscillating assembly form a mechanically resonant system which provides the oscillating scan motion. Each spring consists of two turns of heat treated stainless steel strip having cross sectional dimensions of approximately .50 inch wide and .08 inch thick. Losses in the resonant system are very low and result in a "Q" of approximately 450 so that very little drive motor power is required.

Frequency of oscillation is fixed by adjusting the mass of tuning weights on a flywheel assembly at the extreme +Y end of the oscillating assembly.

2.2.1.4 Caging

A caging system with release mechanism is provided to support the oscillating assembly during ground transportation and launch. This caging system when engaged simultaneously provides good mechanical support to the oscillating assembly and relieves all mechanical loads from the small bearings. A manual system for caging and release is provided for ground use and is accessible at the -Z surface of the structure. Once in orbit, however, the release mechanism is released by command which fires two fuse link type actuators and the unit cannot be recaged.

2.2.1.5 Optical Encoder

The function of defining scan position for use in timing and control of oscillation amplitude is performed by the three segments of the optical encoder: the polygon, the encoder optics and either the primary or backup auxiliary encoder.

A multifaceted polygon ring having fifteen mirror surfaces is mounted to the oscillating assembly, (Figure 2.2.1-4). This polygon is "viewed" by the main encoder optics which contains light sources, slits and detectors to produce the clock, nadir and control pulses necessary for system use. A backup mode for providing nadir and control pulses is supplied by a separate channel of light source/detector combination in the main encoder optics.

The backup auxiliary encoder also has sources and detectors, but of much lower angular resolution. It is used to gate the main encoder nadir and control pulses. The main encoder optics and backup auxiliary encoder mount to the main structure and are accurately aligned to the polygon ring.

A backup mode for providing nadir and control pulses is supplied by a separate channel of light source/detector combination in the main encoder optics.

The primary auxiliary encoder is mounted on the structure near the motor end of the oscillating assembly shaft. Four vanes on the inertia wheel (part of the oscillating assembly) interrupt paths from light sources to detectors and provide primary auxiliary encoder nadir and control pulse gating signals.

Main encoder and auxiliary encoders electrical outputs are carried to the encoder preamplifier assembly (ENPA) via the SSS cable harness. The ENPA is a shielded assembly containing components on three printed wiring boards and is mounted immediately adjacent to the main encoder optics to minimize EMI susceptibility problems.

2.2.1.6 Optical Relay Assembly

A machined beryllium housing contains the optical lenses, mirrors and splitters necessary for the three channels: T Channel, LRD Channel and HRD Channel.

The optical relay housing provides precision mounting interfaces at proper location for the HRD assembly and the PMT assembly (LRD Channel) so that these assemblies can be removed and replaced without disturbing optical alignment. It also provides mounting for two adjustable folding mirrors for the T Channel (MT1 and MT2).

The optical relay assembly is mounted to the main structure by means of adjustable support points which allow it to be aligned and focused to the optical output from the oscillating assembly at M5.

2.2.1.7 Secondary Reference Cube

An optical cube mounted on the main structure provides three optical reference axes with known relationships to the axes best representing the scan of the detectors and to the axes of the mounting interface. The cube is used to transfer alignment information to the spacecraft during integration and test.

2.2.1.8 HRD Channel

The detector for this channel is assembled and accurately aligned to a precision machined magnesium housing which when mounted to the optical relay assembly positions the detector at the optical focal point for the channel.

Removal and replacement is allowed without need for system realignment. A preamplifier consisting of two small printed wiring boards with the circuit components and a connector are contained within the housing. Input/output signals and voltages are carried between this assembly and the PMT/HRD postamplifier assembly through the SSS cable harness. The postamplifier assembly contains the postamplifier circuits for both the PMT and HRD channels on a single multilayer printed wiring board.

2.2.1.9 PMT Channel

A photomultiplier tube and its magnetic deflection yoke are potted in a metal housing with elastic potting material for support and high voltage protection. The aperture for the detector is accurately aligned to the precision machined front end of the housing. Leads from the potted tube assembly for cathode, anode and dynode connections go directly to a metal encased high voltage power supply (HVPS) with internally mounted printed wiring boards containing the circuit components. The HVPS in integrally mounted to the PMT tube and potted in place. A PMT preamplifier circuit is contained on a small printed wiring board mounted in a magnesium housing attached to the rear of the PMT assembly. Deflection yoke leads are pigtailed out of the assembly and connected to a yoke deflection circuit contained in the EST/LMD Assembly.

The PMT assembly is mounted to the optical relay assembly of the SSS and can be removed and replaced withut need for system realignment.

The PMT postamplifier circuit is contained in an assembly with the HRD post amplifier as descrbied in paragraph 2.2.1.8.

2.2.1.10 VDGA/LIN LOG

This electronics assembly consists of three multilayer printed wiring boards mounted on a magnesium chassis with a cover to enclose the assembly. It is interconnected with the HRD and PMT channels via the SSS harness to provide gain controls.

2.2.1.11 T Channel

The detector and final optical elements for this channel are housed in the T Detector Cooler. The cooler, along with a small heating element, provides a selected temperature for the detector of approximately 110°K controlled to 0.1°K and is further described in paragraph 2.2.1.12. Prior to cooler installation, folding mirrors MT1 and MT2 are aligned relative to an accurately machined mounting interface of the SSS main structure in accordance with predetermined optical characteristics of each cooler. This makes it possible to remove and replace the cooler without need for system realignment.

Signal leads from the detector are routed to the T Preamplifier Assembly which consists of circuit components mounted on a printed wiring board contained in a machined magnesium housing and mounted to the SSS structure.

The channel requires thermal references which are provided by subassemblies on the SSS as described in paragraph 2.2.1.13.

2.2.1.12 T Detector Cooler

As explained in the previous paragraph, the purpose of this assembly is to cool the T detector to a suitable operating temperature near 110°K. This is accomplished by an assembly configured as shown in Figure 2.2.1-5. Cooling is accomplished by passive radiation to deep space and requires no moving parts.

The cooler consists of three major sections: mounting ring, outer stage, and inner stage. When functioning in orbit, they are connected to each other by very low conductance supports which maintain accurate mechanical and optical alignment between the sections so that the detector remains accurately positioned with repsect to the lens system and the mounting interface. The inner stage, on which the detector is mounted, has a high emissivity coating so that it has the highest possible radiant coupling to cold space. The outer stage consists of a highly polished cone which reflects almost all incoming radiation within an included angle of 101°. By mounting the cooler in a

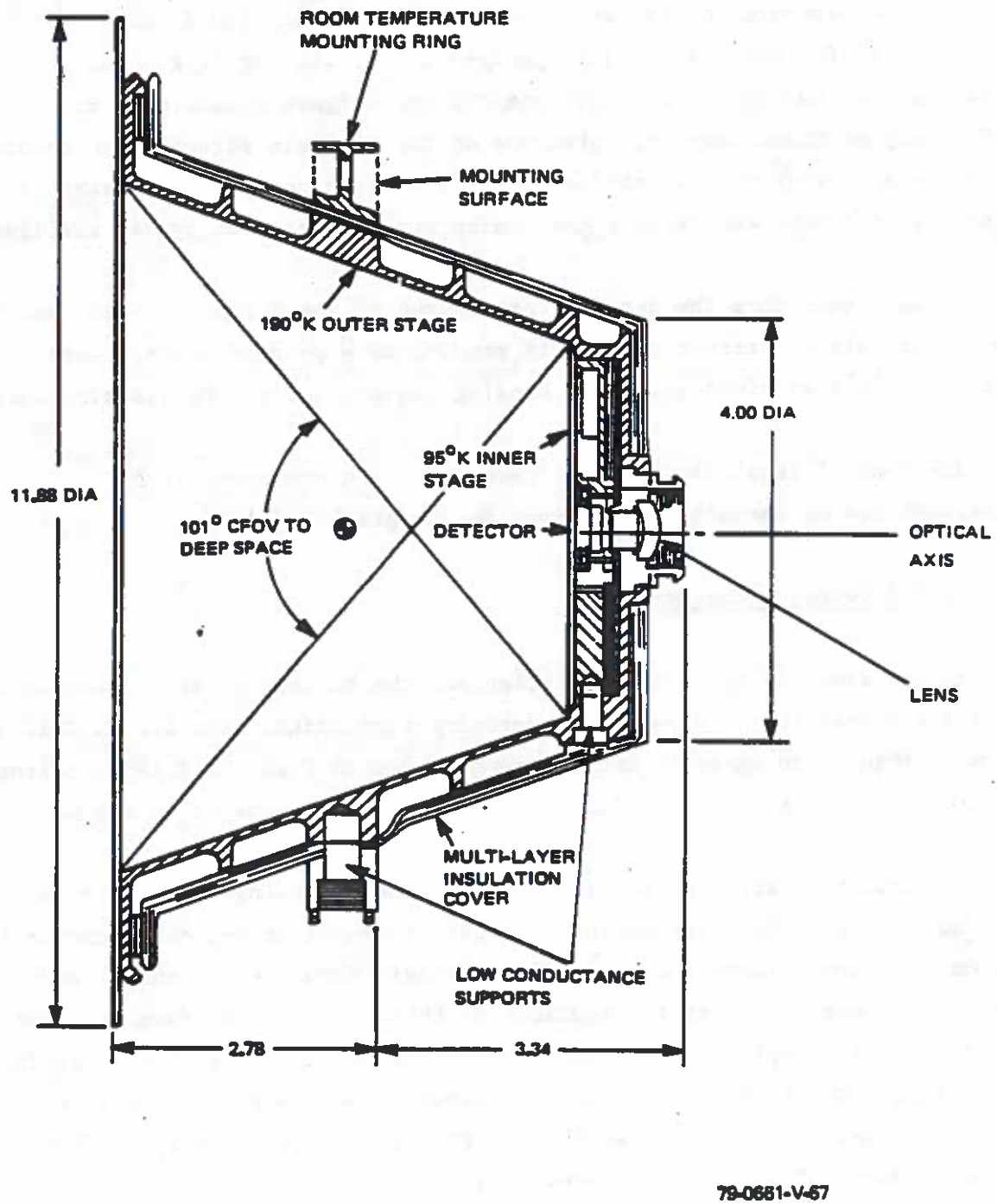


Figure 2.2.1-5. Radiator Cooler

slightly tilted position on the spacecraft, all earth source energy is prevented from reaching the innter stage as is indicated by Figure 2.2.1-6.

The temperature of the outer stage is maintained at approximately 190°K by an annular radiation plate attached to its large open end. The entire surface at this end is protected from direct solar inputs by a sunshade, GSSB, supplied by and mounted on the spacecraft.

2.2.1.13 T Clamp and T Cal

These two assemblies are required for T Channel temperature references as mentioned in paragraph 2.2.1.11. T Clamp is active at the minus (-) end of scan and T Cal is active at the plus (+) end of scan. Each one consists of a black cavity with a known temperature by measurement. T Cal is attached directly to the SSS main structure and maintained at structure temperature which is about +5°C. T Clamp is thermally insulated from the structure and conductively coupled to a radiating plate aimed at deep space and sized to maintain the cavity temperature between -40°C and -21°C. The plate is adjacent to the T-Detector Cooler cone opening.

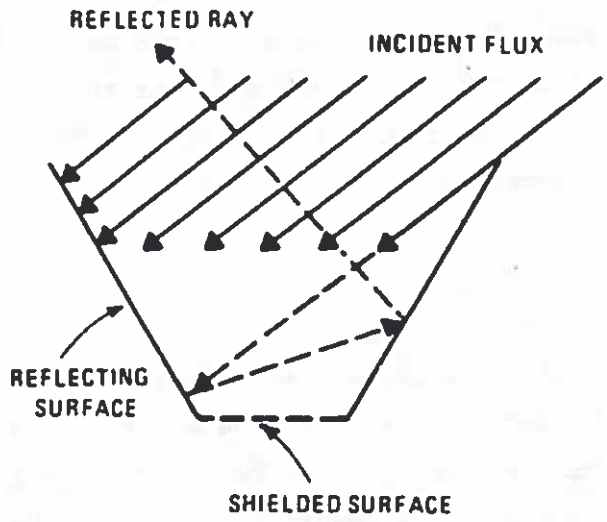
2.2.1.14 EST/LMD

This unit consists of a single printed wiring board with components to provide EST outputs from all temperature monitoring locations within the SSS and to control the magnetic deflection coils of the PMT. The board is housed in a cavity at the (-) Y end of the SSS structure.

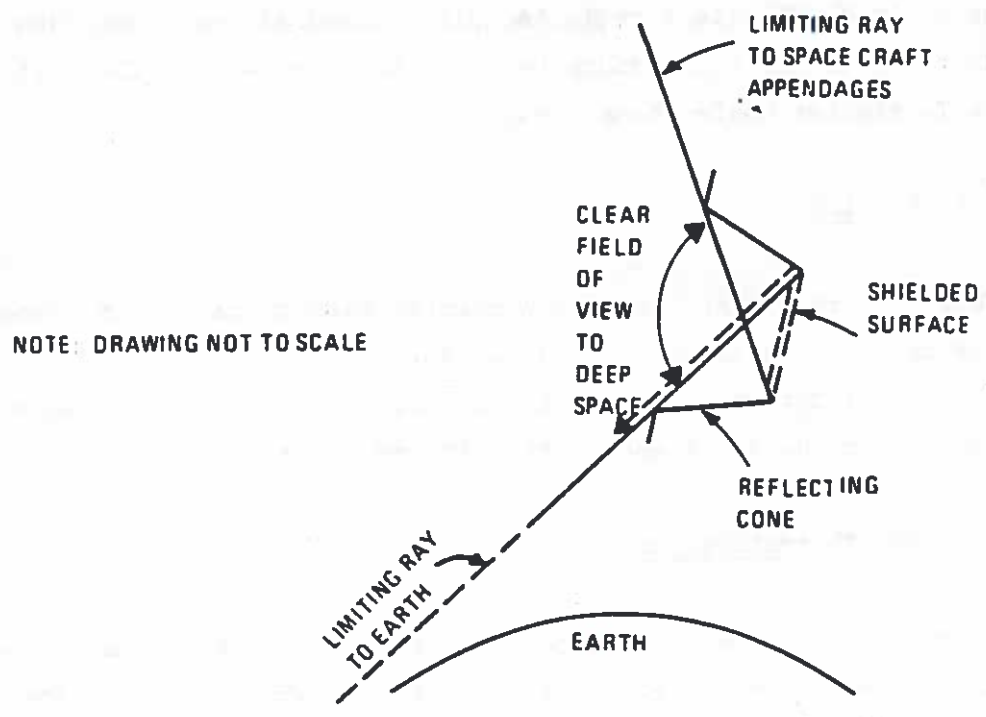
2.2.1.15 SSS Thermal Control

Overall thermal control of the SSS is provided by thermal blanketing in combination with strip heaters attached to the SSS structure. Specific items requiring special thermal control have been described in previous paragraphs.

The SSS is thermally insulated from the spacecraft. It is completely encased in multilayer thermal blankets attached to fabricated epoxy-glass



SHIELDING OF INCIDENT RADIATION BY REFLECTING SURFACES



NOTE: DRAWING NOT TO SCALE

RADIATIVE COOLER GEOMETRY IN RELATION TO LIMITING RAYS FROM EXTERNAL RADIATION SOURCES

74-1090-V-33

Figure 2.2.1-6. Outer Stage Function

support frames. Only the telescope portion of the oscillating assembly is external to the blanketing. Except in the immediate vacinity of the telescope, the external layer of the blanket is a second surface mirror of aluminized Teflon with the Teflon thickness chosen for good emissivity in combination with low solar absorbtivity. The remaining nine layers of the blanket are double sided aluminized Mylar separated by Nylon netting.

Four strip heaters on the SSS structure are distributed along the four edges of the basic box structure. Each heater is sized in consort with the expected local heating of the various electronics packages on the structure. Each heater is temperature controlled by an individual Heater Controller which averages the input from three thermistors located on a structure adjacent to the heater. The four controllers are set within 0.5°C of each other to maintain the SSS structure at a preselected set point temperature of +5°C. The total power available from the four heaters is 22 watts maximum.

Thermal analyses have been performed for two separate SSS configurations. The first configuration is the SSS without the GSSA. This configuration was analyzed in a twilight orbit ($\beta = 0°$). Since in this orbit there is little or no sunlight on the telescope, the heater power requirements and mirror temperatures are similar to those expected with the spacecraft glare obstructor (GLOB). Figure 2.2.1-7 gives the mirror temperatures and heater powers as a function of structure temperature for the $\beta = 0°$ orbit.

The second SSS configuration analyzed combines the SSS with the GSSA (specular shade). This shade is used on the SSS for noon orbits ($\beta = 90°$) and near noon orbits ($\beta = 75°$). Figures 2.2.1-8 and 2.2.1-9 give the calculated mirror temperature and heater powers as a function of structure temperature for $\beta = 90°$ and $\beta = 75°$ orbits

The M1 mirror temperature changes ahout 2.5° to 3°C for a 5°C temperature change of the structure. Other mirror temperatures curves have the same slope. The power that is given is an orbit average. At some times it is possible that none or all of the heaters will be on, depending upon the set point, orbit, and position in orbit.

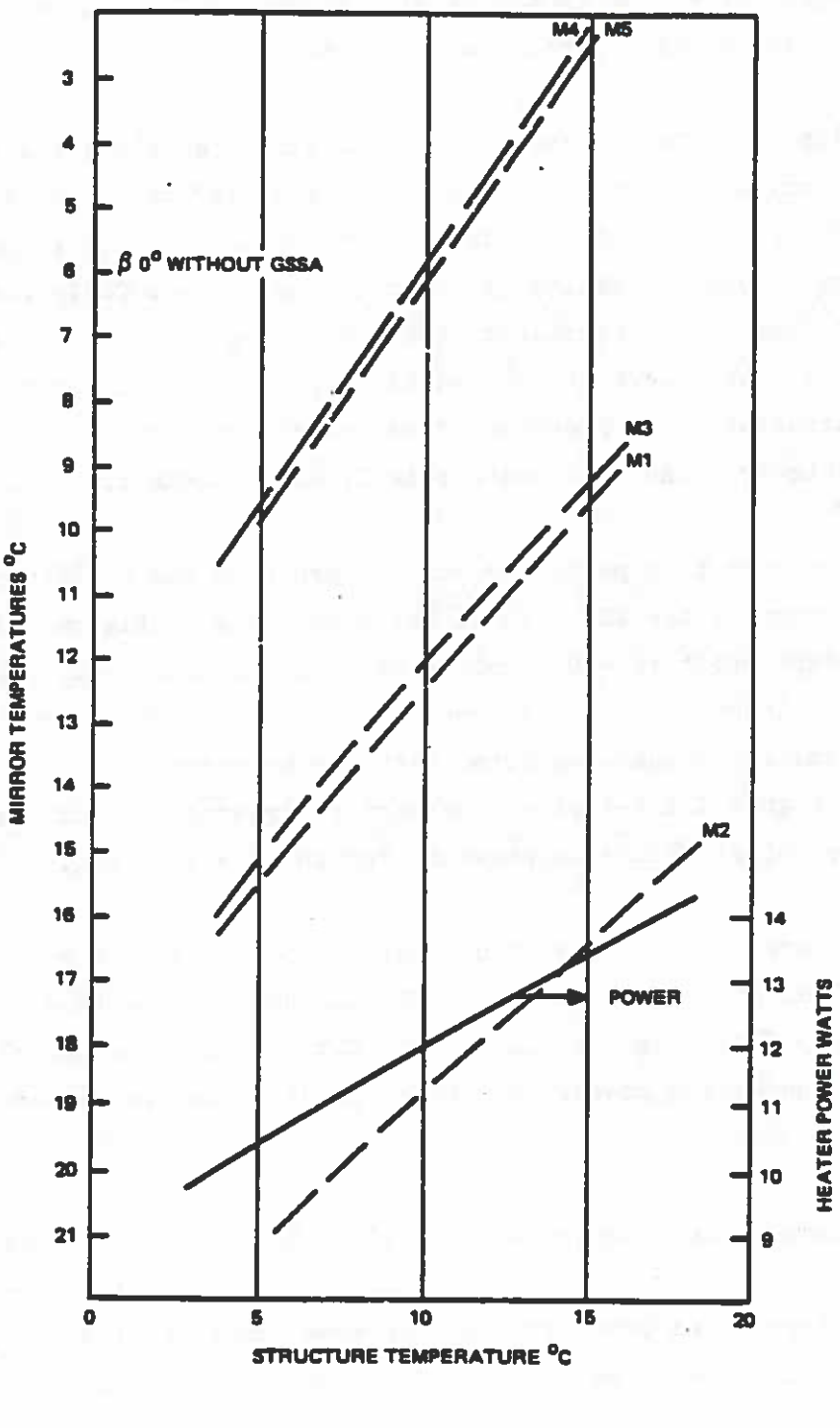


Figure 2.2.1-7. SSS Structure Temperature (ß = 0°)

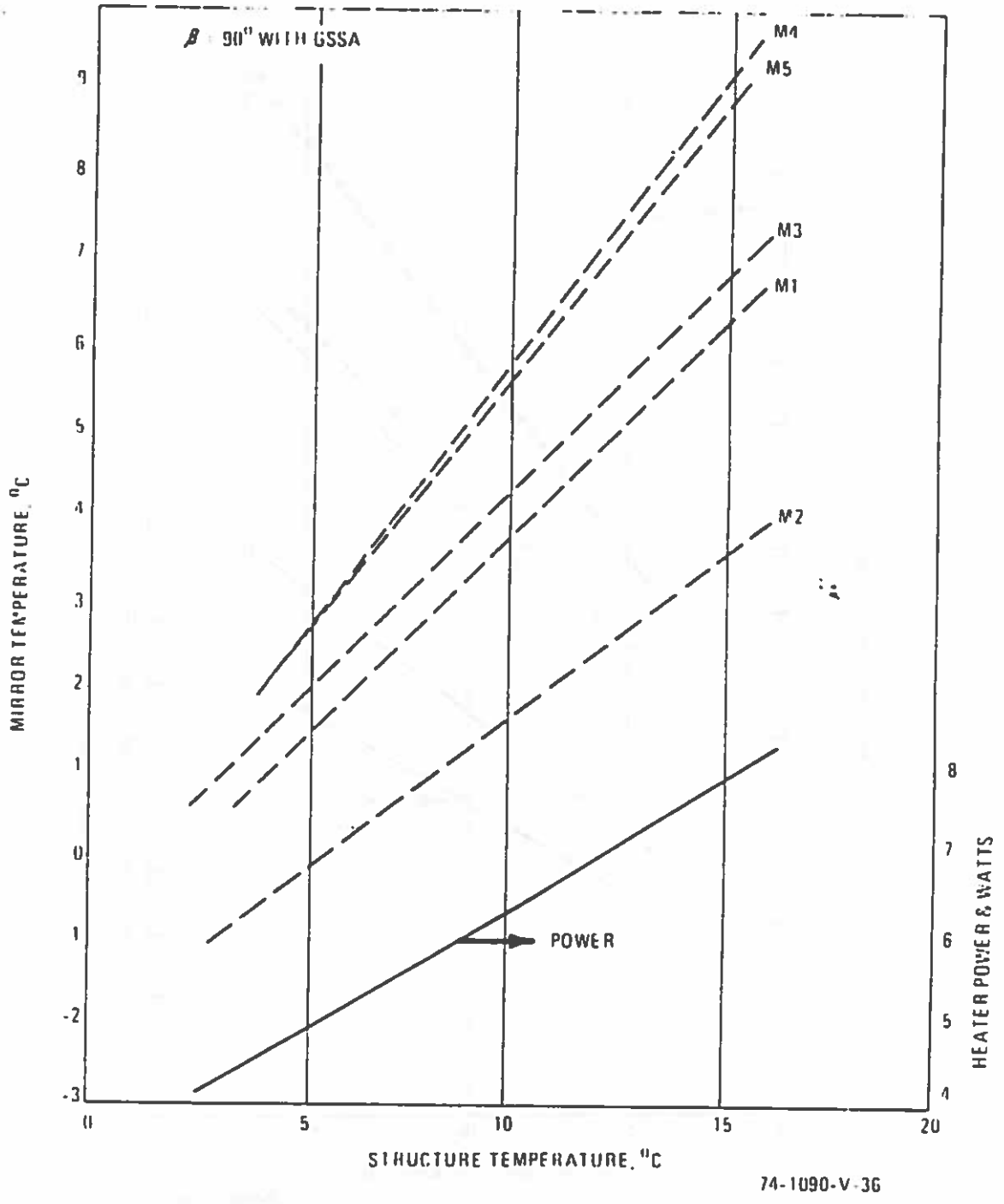


Figure 2.2.1-8. SSS Structure Temperature (β = 90°)

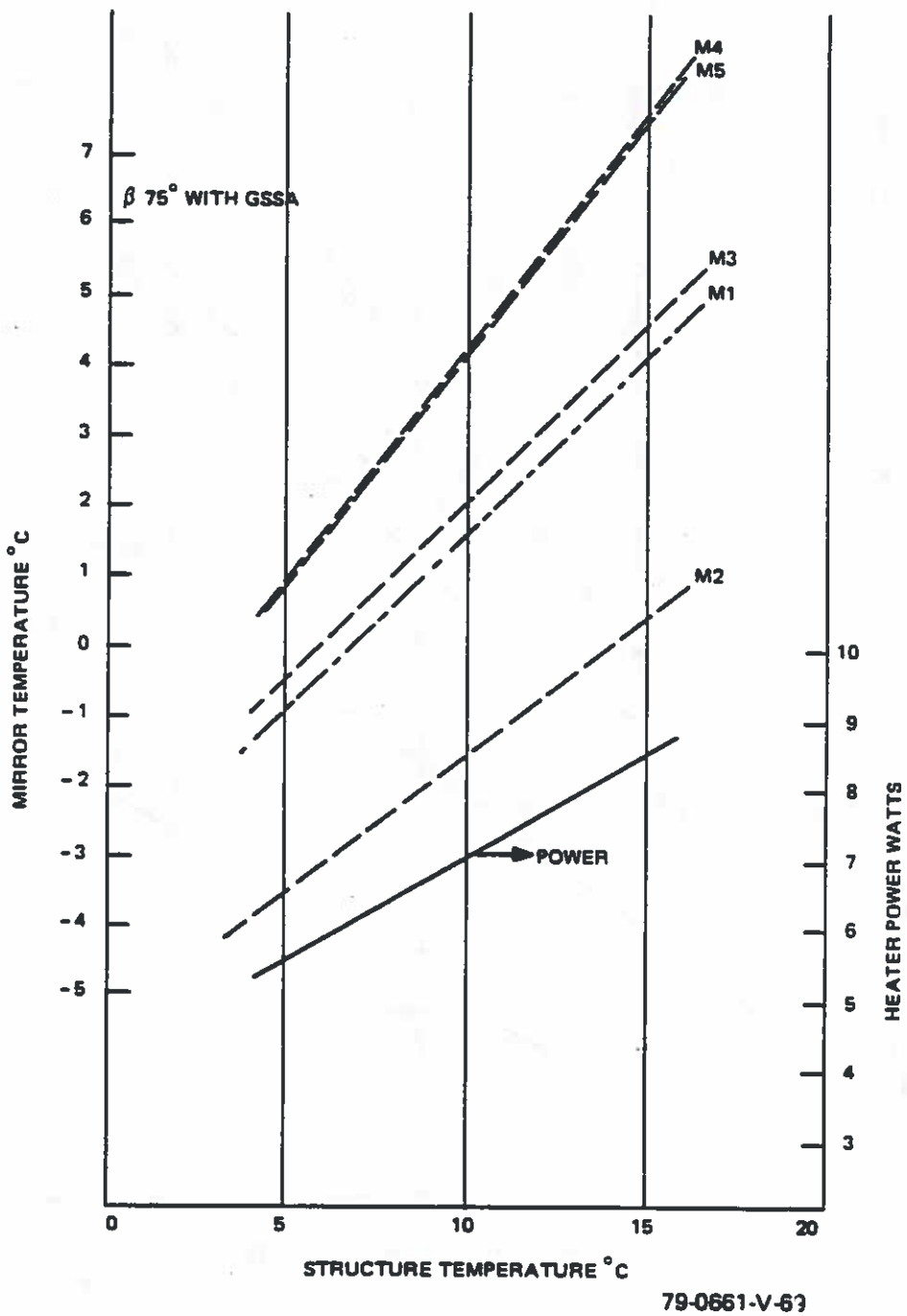


Figure 2.2.1-9. SSS Structure Temperature (β = 75°)

2.2.1.16 Contamination Control

The exposed optics (i.e., the telescope) and the T cooler are particularly susceptible to functional degradation due to contamination. Telescope contamination causes degradation because light incident on the mirror surfaces can be scattered by the contamination and be partially directed on-axis through the optics train and appear to be a scene signal. Therefore, it is essential to minimize contamination through the life of the telescope. To minimize contamination, the whole OLS is fabricated from low outgassing substances. To protect against particle and environmental contamination, the telescope is fabricated and tested in a clean room environment. When a cleanroom is not available like at the launch facilities, the telescope is purged with clean, dry nitrogen. A deployable cover (DOC) protects the telescope from contamination during test, launch and early orbits. This cover actually mounts on the glare suppression subsystem (GSSA) but it covers the entire scanning aperture of the SSS. It is fabricated from an extremely thin section of metal shaped to cover but not tightly seal the aperture opening.

Contamination of the T cooler can cause degradation of two types. The first type is associated with either particulate or film type contamination of the cool specular surfaces of the outer stage cone. This would result in scatter energy that can impinge on the inner stage and warm it above the desired temperature. A deployable protective cover (DCC) is provided for the cooler aperture during ground test, launch and early orbits. The cover is fabricated from kapton coated urethane foam attached to a metal framework. It makes intimate contact with the cooler cone aperture and is retained by a spring loaded hinge on one side and a release mechanism on the other. When the release mechanism is actuated by ground command, the cover swings off and is ejected from the spacecraft.

The second type of T cooler degradation is associated with surface film contamination of the germanium lens which results in transmission degradation and consequent signal deterioration. Film accumulation is generally caused by outgassing products accumulating on low temperature surfaces. To prevent this, a "warm window" assembly is provided over the cold T channel lens. It is

radiatively coupled to the SSS structure and thermally isolated from the cone cooler structure, so that the window remains nearly at structure temperature and thus does not tend to accumulate a film deposit. A bellows system is provided between the warm window and the cooler to allow for gas escapement during launch and to provide a sealed enclosure after attaining orbit.

2.2.2 Glare Suppression Subsystem (GSSA)

For noon orbit glare suppression, first surface specular mirror sunshades (GSSA) are mounted immediately adjacent to the aperture area of the telescope. These mirrors prevent sunlight from impinging directly on any part of the telescope or surrounding diffuse scattering surfaces. The GSSA assembly consists of the flat mirror panels which are supported from the SSS structure and configured to surround the scan aperture as shown in Figure 2.2.2-1. It also provides support and mounting for the deployable optics cover (DOC) and its release mechanism described in paragraph 2.2.1.16.

The GSSA/DOC assembly measures approximately 39.4 inches long, 17.0 inches high and 14.4 inches wide at its extremes and weights 8.7 pounds. It is fabricated from copper clad epoxy-glass panels which have the copper side nickel plated and superpolished to a low scatter optical surface quality. The panels are bonded to molded fiberglass layup support structures which orient the panels so that, in orbits having sun angles between 75° and 95°, sunlight which impinges on the polished inside surfaces is specularly reflected out rather than onto the SSS telescope. The external surfaces of the support structures are painted blank and the entire assembly has been vaccum outgassed prior to installation on the SSS.

2.2.3 Signal Processing Subsystem (SPS)

The signal processing subsystem (SPS) is about 18 x 28 x 6 inches in size, weighs about 70 pounds and can dissipate up to 70 watts of electrical power depending on the operating mode selected. A picture of the SPS is shown in Figure 2.2.3-1. The SPS mounts on panel 6 of the spacecraft equipment support module (ESM) as shown in Figure 2.2.0-3.

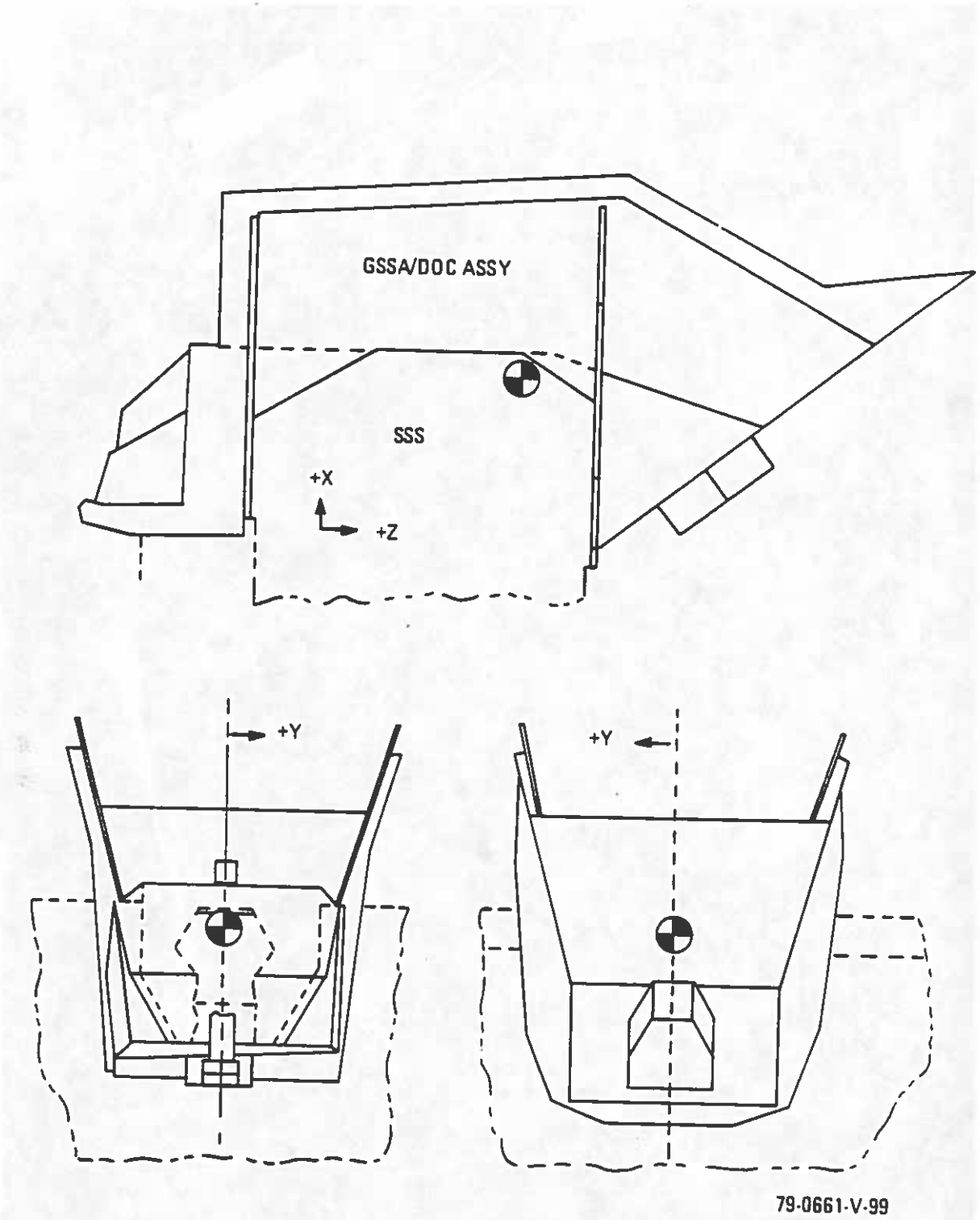


Figure 2.2.2-1. GSSA Outline Drawing

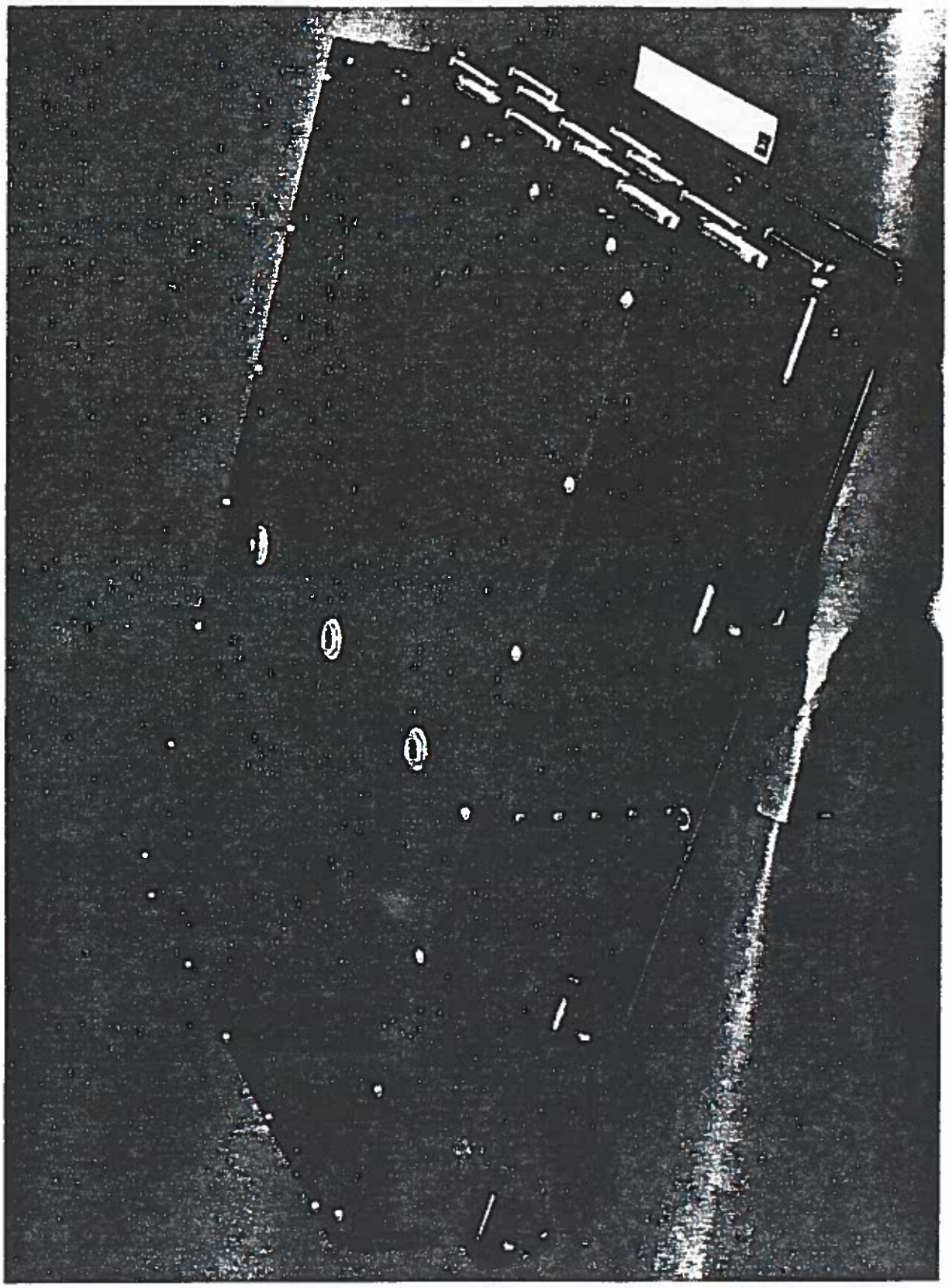


Figure 2.2.3-1. SPS Assembly

The SPS, which contains the dual processors and memories, is described by subassemblies in the subsections which follow. The many branches of the SPS family tree are shown in Figure 2.2.3-2.

2.2.3.1 Board Assemblies

Most of the electronics in the SPS is packaged on 90 plug-in boards for ease of test and replacement in instances of design revisions. These boards are 4.9 inches wide by 4.5 inches high with 80 pin input/output connectors on the bottom edge and test points at the top edge. Thermal "ears" are provided to conduct generated heat from the board surface to the SPS structure.

All SPS boards are point-to-point; stitch bonded, welded wire assemblies. The basic board is a multilayer, plated through hole, printed wire board containing stainless steel pads for stitch bonding the interconnections. A thermal plane is bonded to the component side of many of the boards, when required by board thermal loading, to maintain component temperature with design limits. Figure 2.2.3-3 shows a sample SPS board before component installation.

Circuit interconnections are made using insulated nickel wire welded to the stainless steel weld pads on the circuit side. Three standard boards are used to handle the mix of components: 14 lead dual in-line package integrated circuits (DIP's); 16 lead DIP's; 24 lead DIP's, TO-5 and TO-18 transistor cans and discrete components. A total of 6398 components are distributed over the 90 digital boards. Figure 2.2.3-4 shows a sample digital board with DIP's and discrete components.

2.2.3.2 Red/Black Assembly

Two Red/Black assemblies are contained within the SPS. Each Red/Black assembly contains the electronics which interface between the spacecraft and the SPS electronics. This unit is an EMI tight assembly consisting of an aluminum sheet metal chassis, three plug-in stitch bonded board assemblies (each 3.40 inches wide by 3.76 inches high with a 60 pin input/output

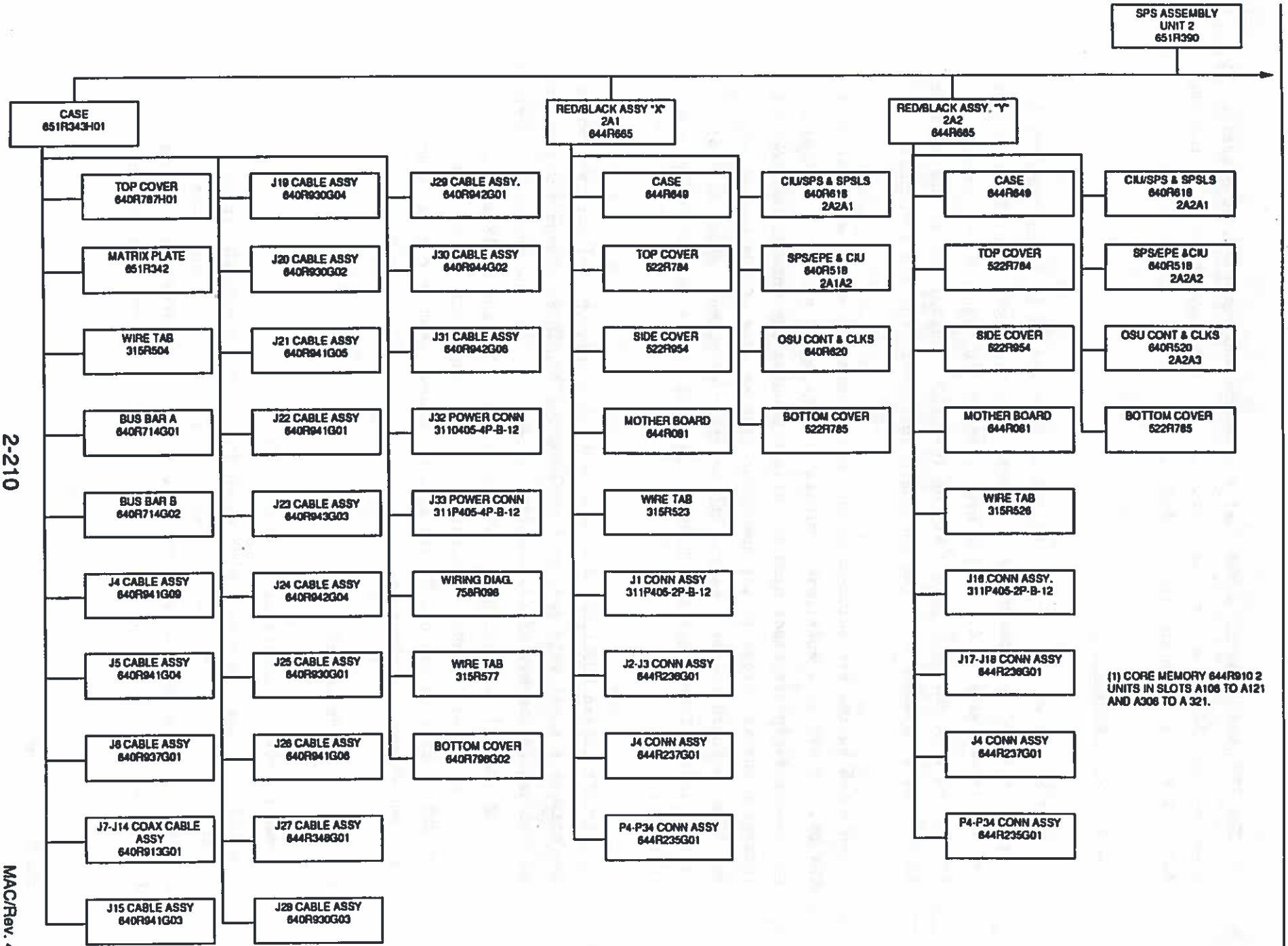


Figure 2.2.3-2A SPS Family Tree (OLS 12)

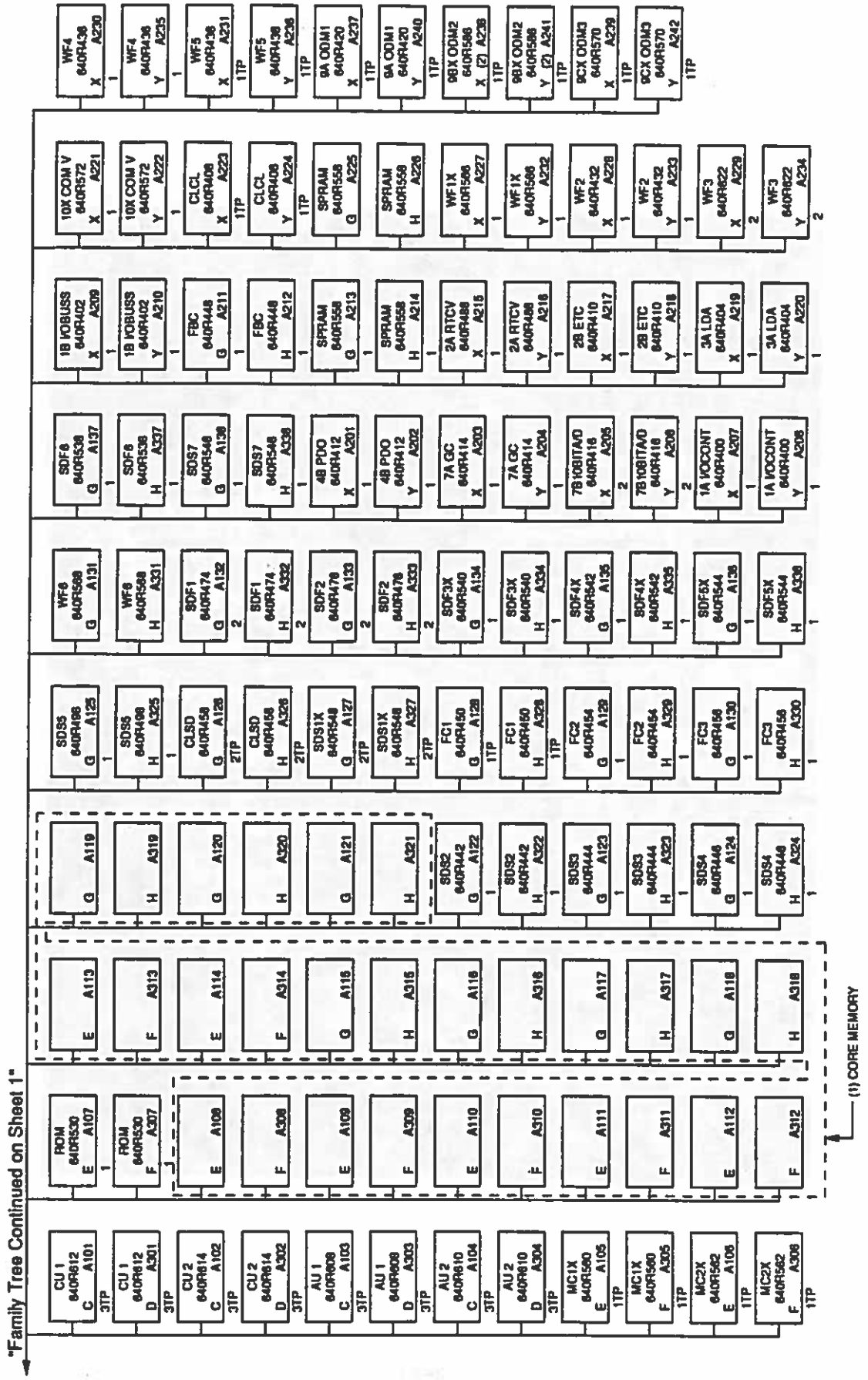


Figure 2.2.3-2B SPS Family Tree (OLS 12)

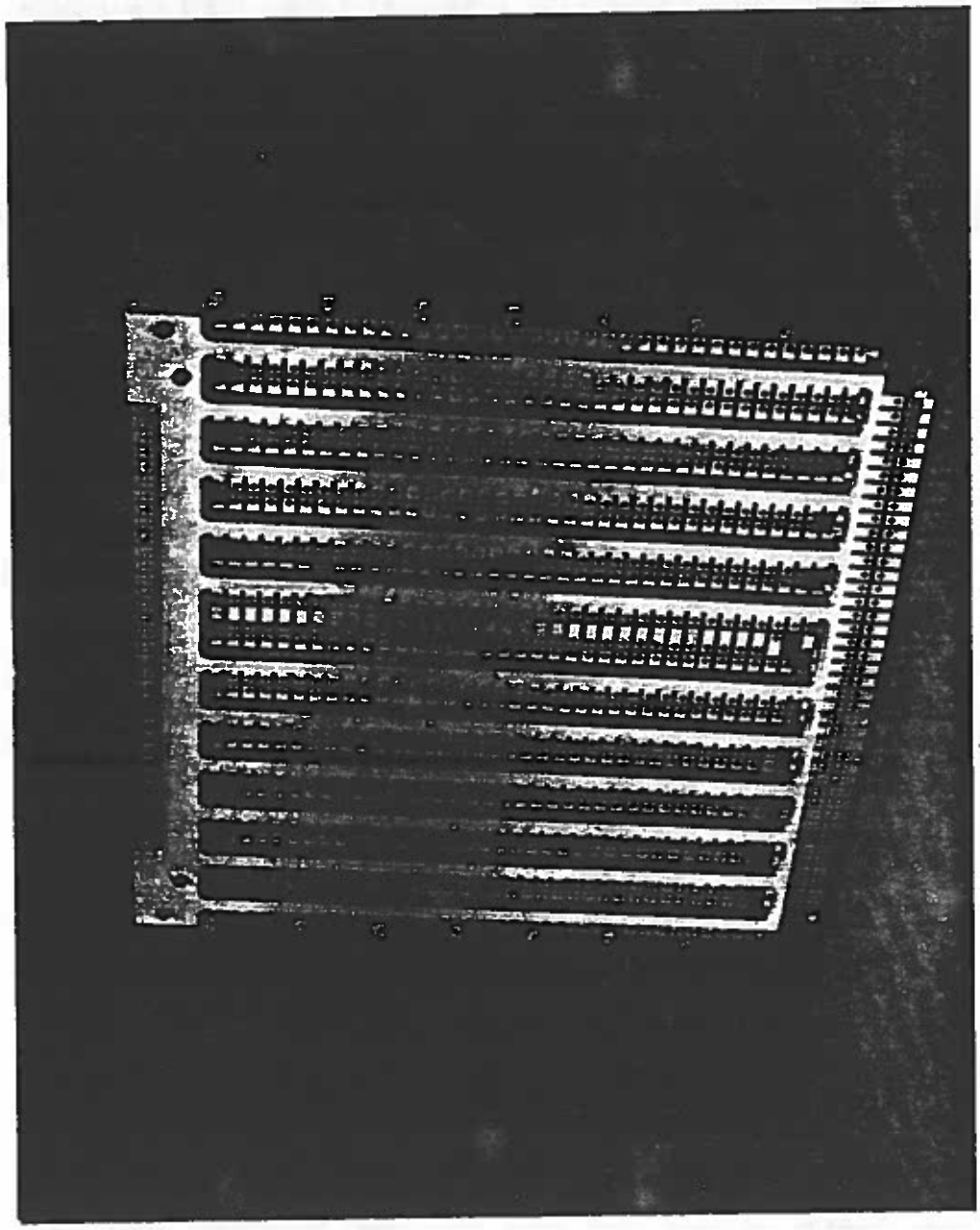


Figure 2.2.3-3. Bare Board with Thermal Plane

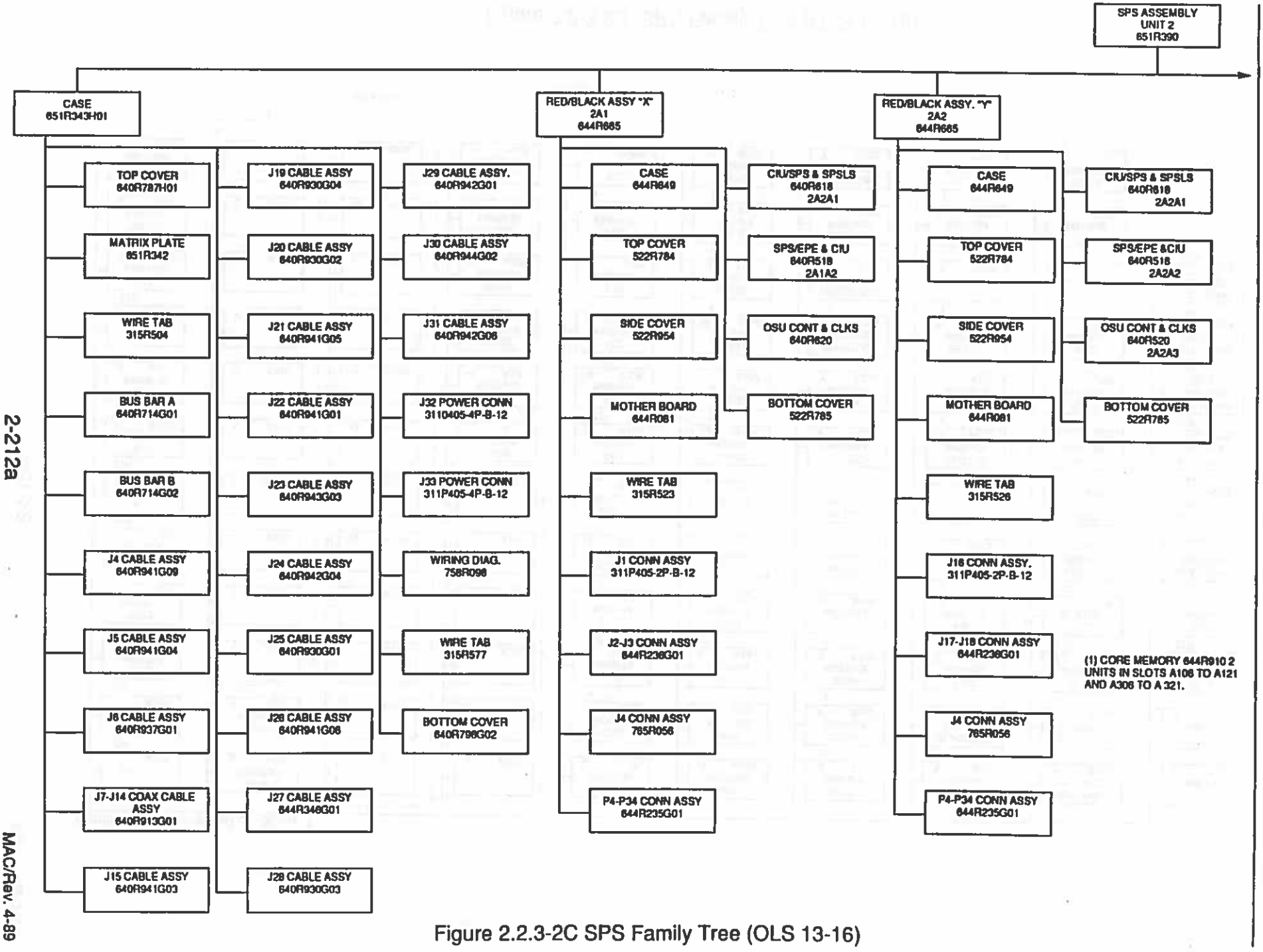


Figure 2.2.3-2C SPS Family Tree (OLS 13-16)

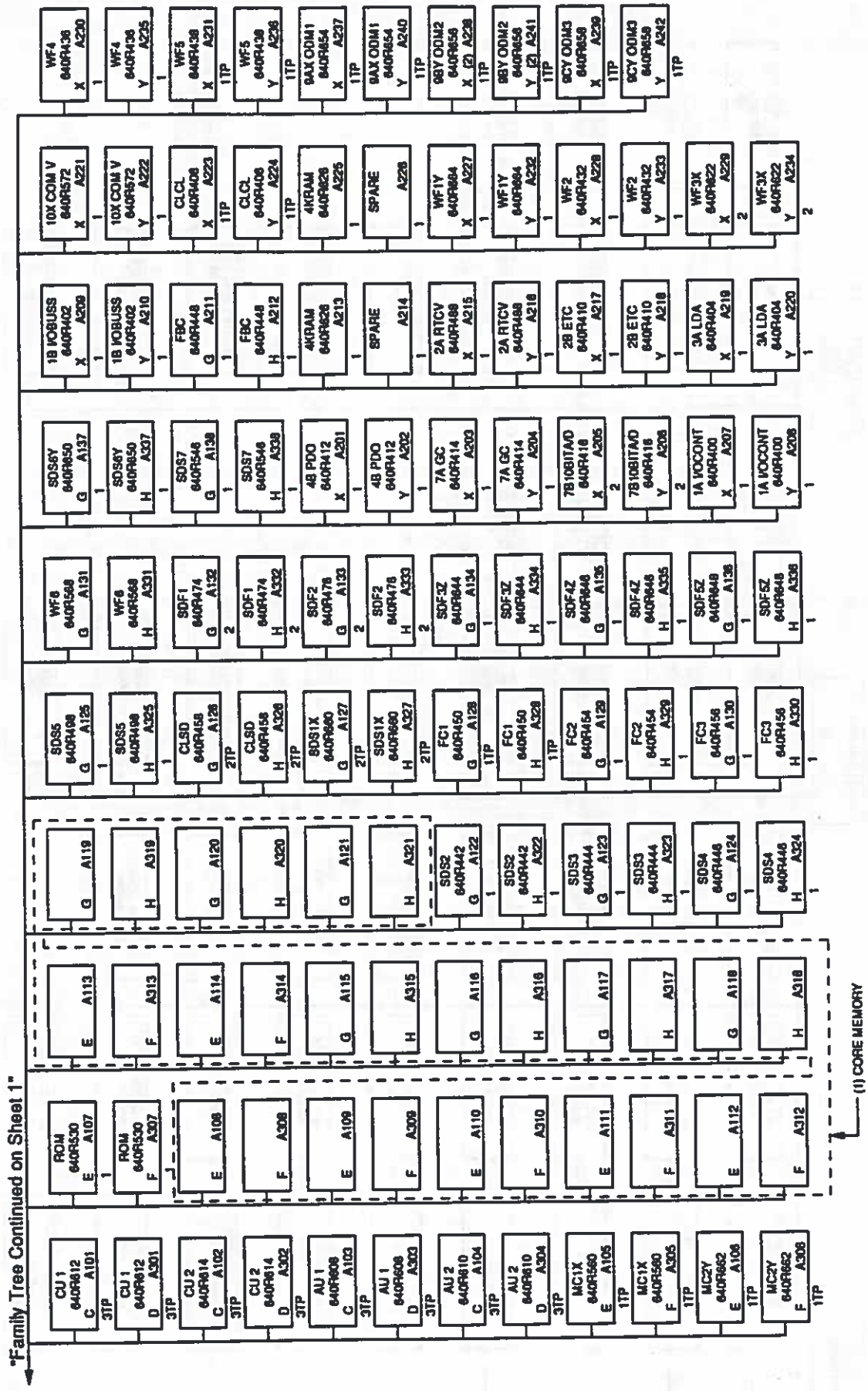


Figure 2.2.3-2D SPS Family Tree (OLS 13-16)

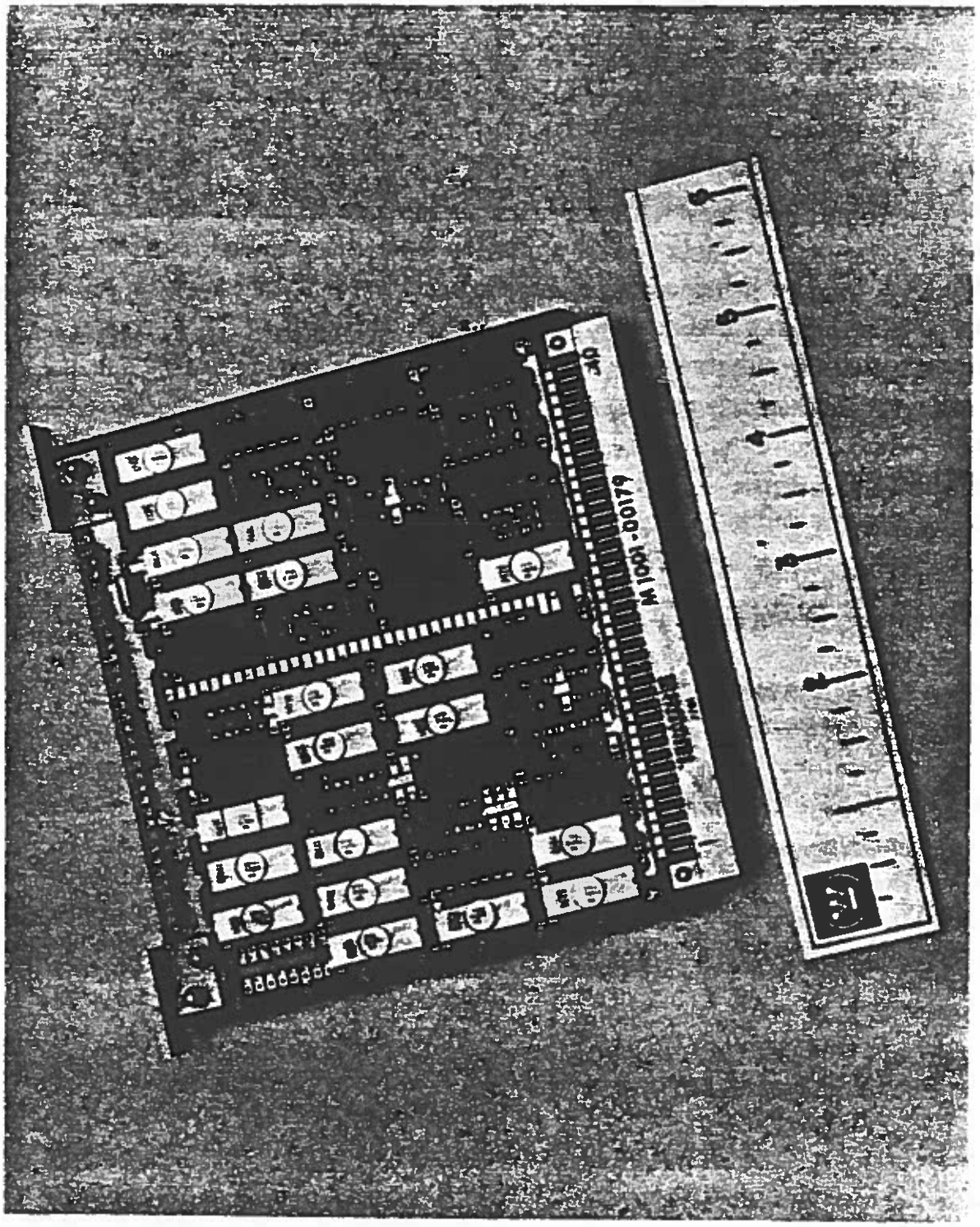


Figure 2.2.3-4. Sample Digital Board

connector), two point-to-point I/O connector assemblies, one point-to-point back-to-back chassis connector/filter connector assembly and one matrix plate assembly. A total of 418 components are distributed over the six boards contained in the two Red/Black assemblies. The Red/Black plugs directly into the matrix plate of the SPS. Figure 2.2.3-5 shows the Red/Black assembly.

2.2.3.3 Core Memory Assembly

Two core memory assemblies are contained within the SPS. Each core memory assembly contains the electronics and memory core array for two separate nonvolatile, nondestructive readout, random access memories one a 12,288 word, 16 bit memory and the other a 4096 word, 18 bit memory. Each assembly consists of an aluminum chassis, a multilayer mother board, two core memory stacks, twelve multilayer, plated through hole, printed wiring boards and two 80 pin I/O connectors assembled to the mother board. A total of 1800 components are distributed over the 24 boards contained in the two core memories. The core memories plug directly into SPS matrix plate. Figure 2.2.3-6 shows the core memory assembly.

2.2.3.4 Interconnection

2.2.3.4.1 Matrix Plate

The matrix plate (or mother plate) is used to interconnect all digital boards, bus bars, I/O connector headers, red/black boxes, coax I/O connectors and core memory assemblies into an operating system. The matrix plate is an aluminum plate with female insulated connector pins inserted into it. These female connector pins receive the connector pins of the above assemblies. The rear ends of the pins are automatically point-to-point wire wrapped to make system interconnections.

2.2.3.4.2 Power Distribution

Molded, plugable power distribution bus bars are used to distribute four voltages and two grounds to the various boards and assemblies. Each bus bar

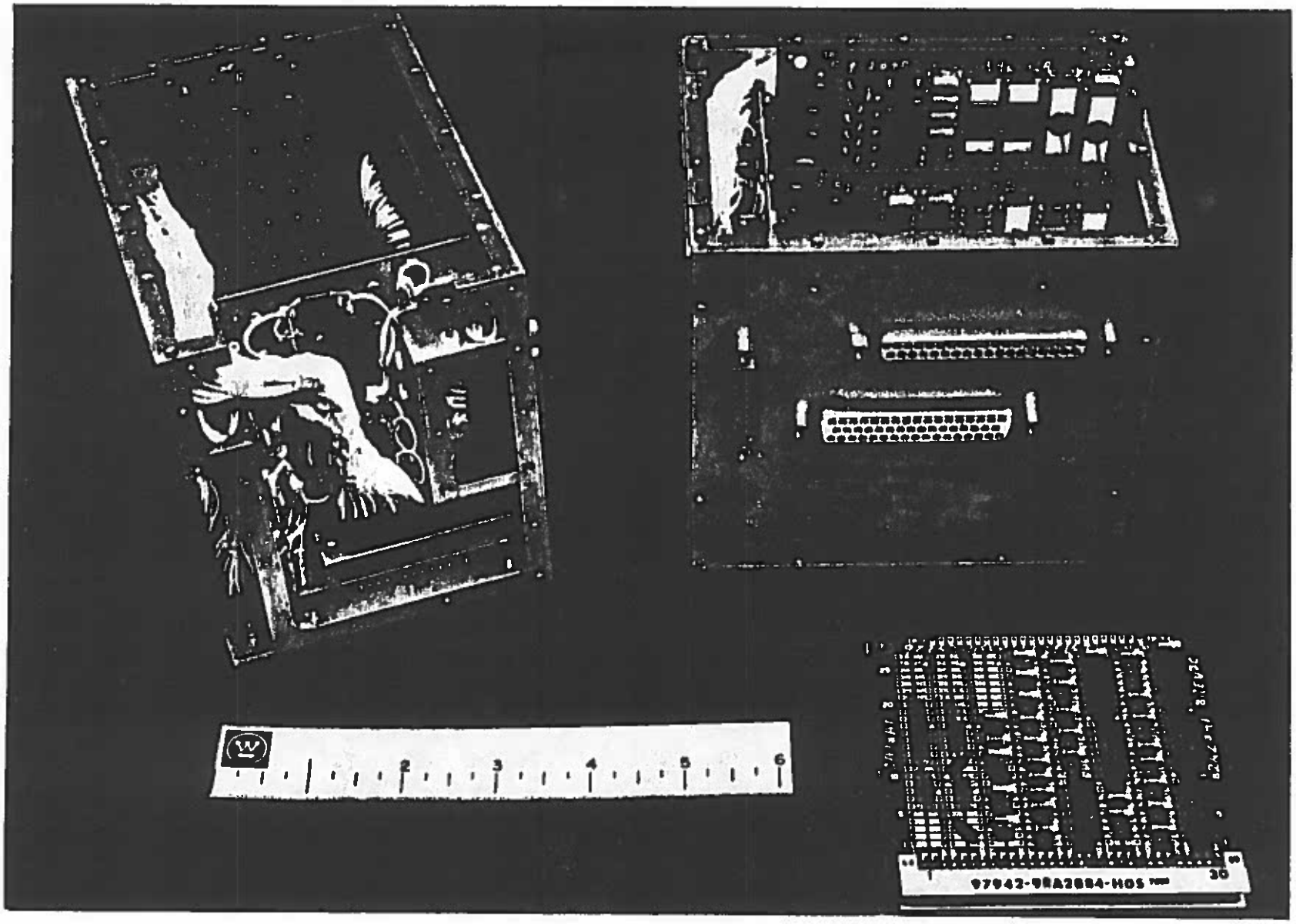


Figure 2.2.3-5. Red/Black Assemblies

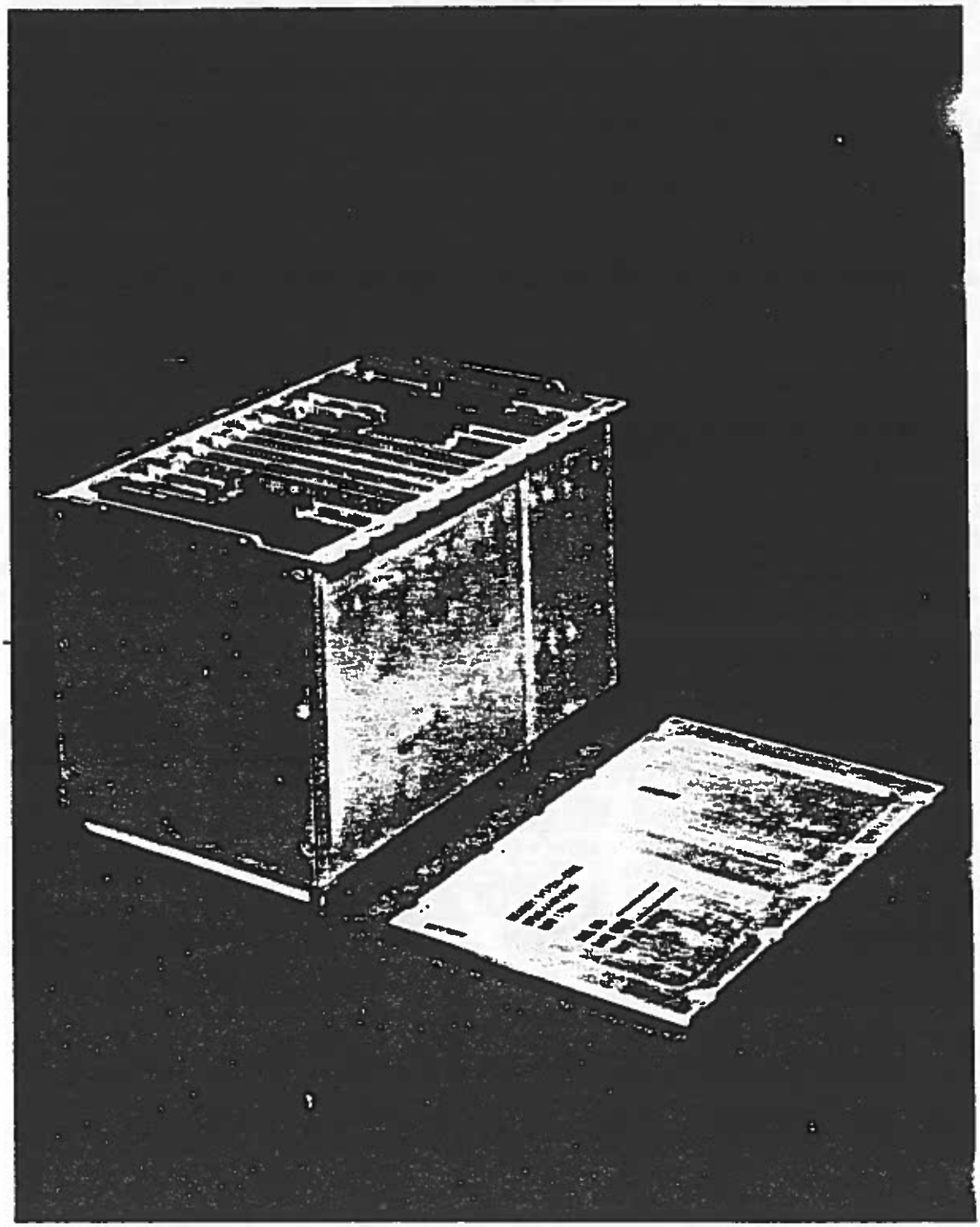


Figure 2.2.3-6 Core Memory Assembly

plugs into the matrix plate and is wired to the power input connector through point-to-point wiring at the bus bar header input terminals. Two bus bars are used in the SPS to segregate the dual processor power distribution.

2.2.3.4.3 I/O Connector Assemblies

Input/output connector assemblies for the SPS are point-to-point wired from I/O connectors to matrix plate connector headers. These units plug directly into the matrix plate at one end and are bolted to the structure of the SPS at the other end.

2.2.3.5 SPS Thermal Control

Thermal control for the SPS box is provided by conduction and radiation. In general, the heat generated by component dissipation is conducted from the components into the thermal plane of each board. From there it is conducted through board ears to the SPS cover and then into the spacecraft structure. The design of the SPS wherein the board ear cover is the spacecraft mounting interface, provides the shortest conductive thermal path possible. The box is painted black to improve the radiation capabilities so that a large part of the energy in the unit is radiated from the SPS surface to its surroundings.

Using data generated by the mathematical thermal model of the SPS for the condition of full up power, nominal board dissipation and a nominal SPS/spacecraft interface temperature of 20°C, the highest component temperature is expected to be about 98°C. For the condition of full up power; maximum board wattage dissipation and maximum interface temperature of 30°C, the highest component temperature is predicted to be about 108°C.

Under nominal operating conditions, one side powered and a spacecraft interface temperature of 20°C, the highest component temperature is predicted to be about 91°C.

2.2.4 Special Processing Unit (SPU)

The special processing unit is about 13 x 13 x 6 inches in size, weighs about 18 pounds and dissipates 5 watts. A picture of the SPU is shown in Figure 2.2.4-1. The SPU mounts on panel 1 of the spacecraft equipment support module (ESM) as shown in Figure 2.2.0-3.

The SPU contains dual special sensor processing and dual RTD processing units as shown by the family tree in Figure 2.2.4-2.

SPU major subassembly designs are typical to those used in the SPS except the matrix plate and bus bar are scaled down in size and the SPU does not require a red/black assembly or a core memory. All electronics in the SPU is packaged on 28 plug-in, nonthermal-plane boards, identical to those used in the SPS. A total of 2290 parts are distributed over these 28 boards.

2.2.4.1 SPU Thermal Control

The SPU is similar in thermal design to the SPS but dissipates much less power a total of 5.3 watts at full up power.

Average component temperature under nominal conditions is predicted to be about 82°C and under worst case conditions, maximum component temperatures are predicted to be 96°C based on the SPU mathematical thermal model.

2.2.5 Power Supply Unit

The power supply unit (PSU) is about 14 x 14 x 7 inches in size, weighs about 27 pounds and dissipates about 45 watts of electrical power. A picture of the PSU is shown in Figure 2.2.5-1. The PSU mounts on panel 5 of the spacecraft equipment support module (ESM) as shown in Figure 2.2.0-3.

The PSU contains the dual power supply system and partially dual analog board assemblies and is described in the subsections which follow via brief

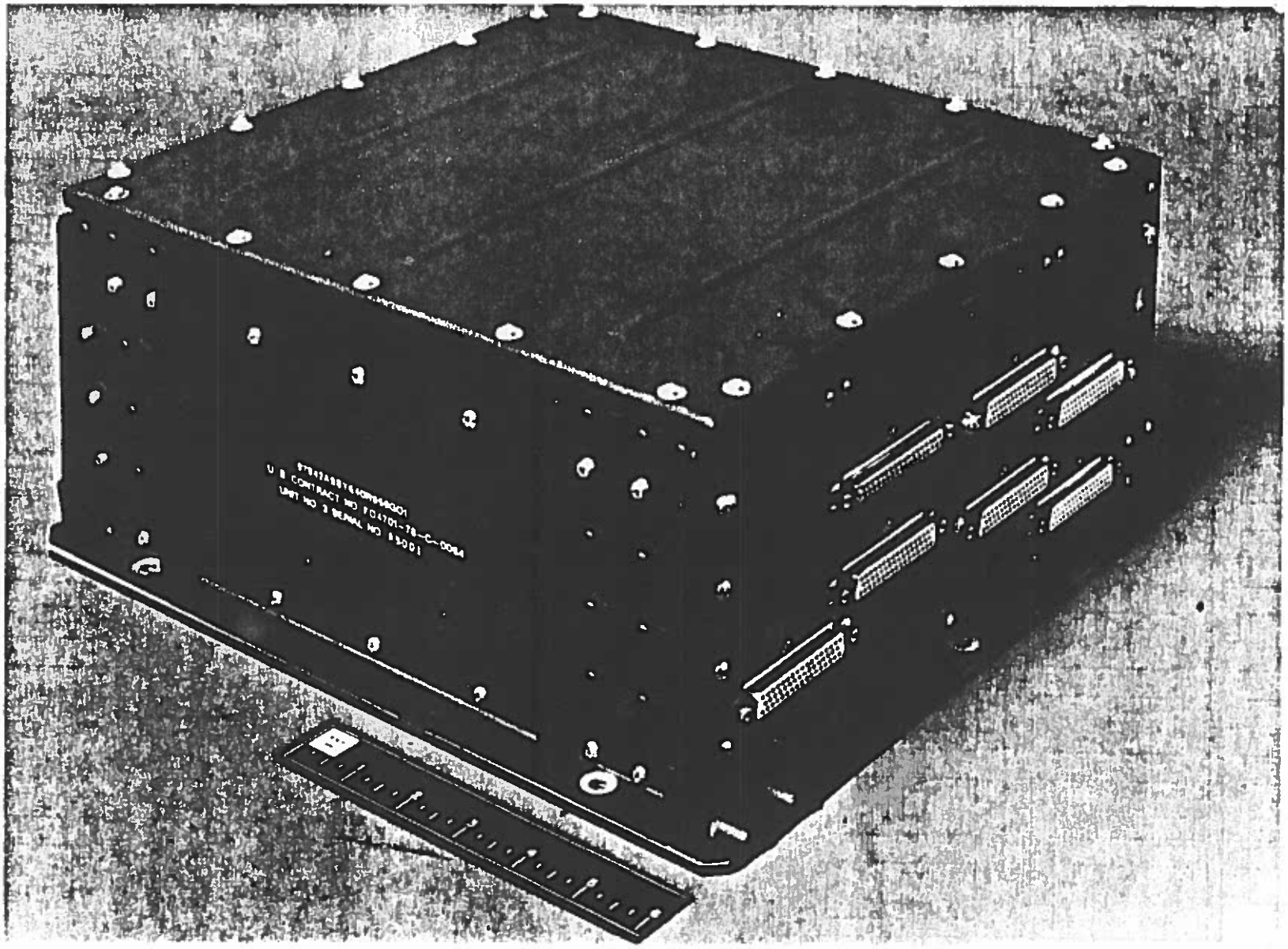


Figure 2.2.4-1. SPU Assembly

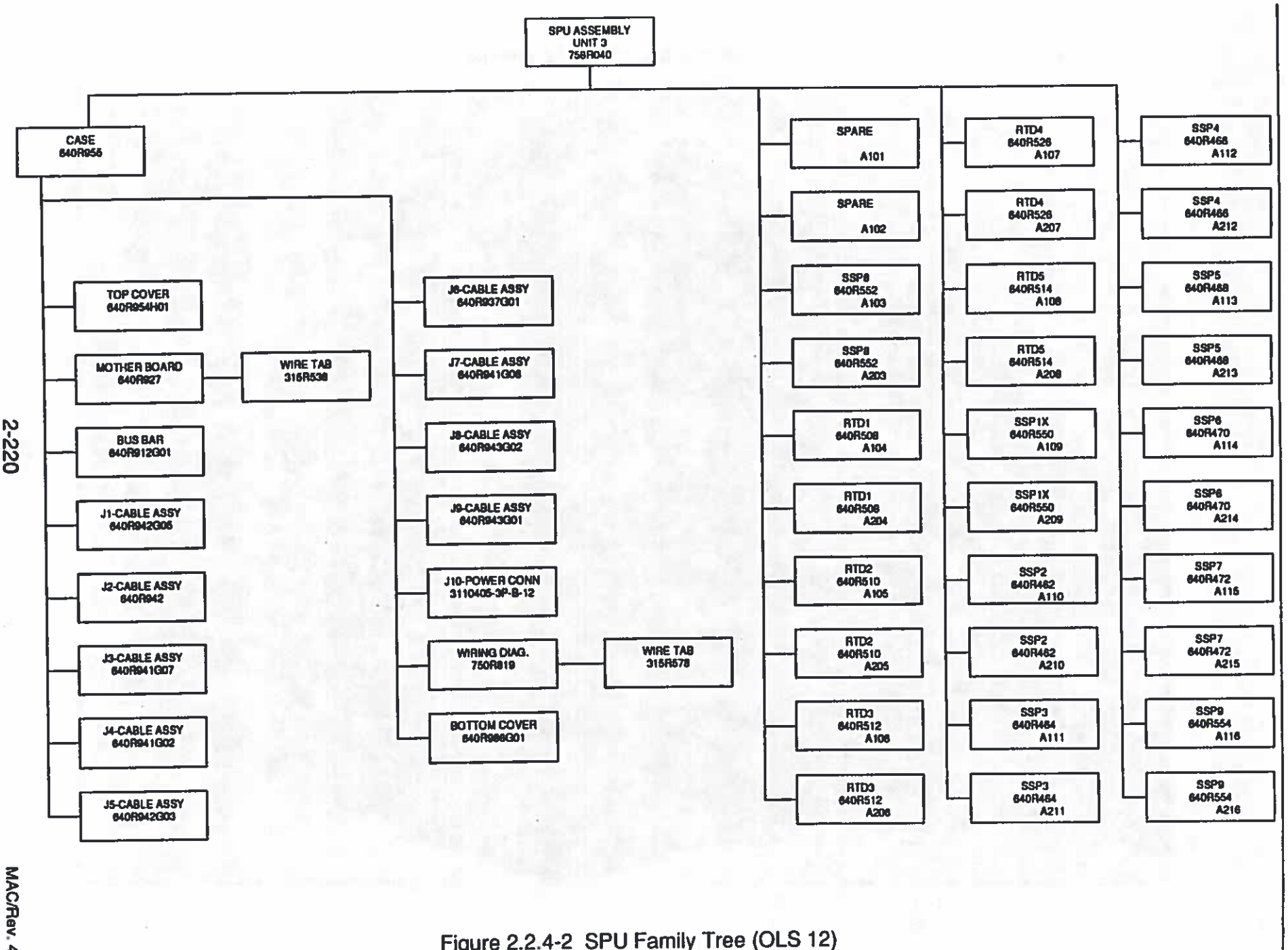


Figure 2.2.4-2 SPU Family Tree (OLS 12)

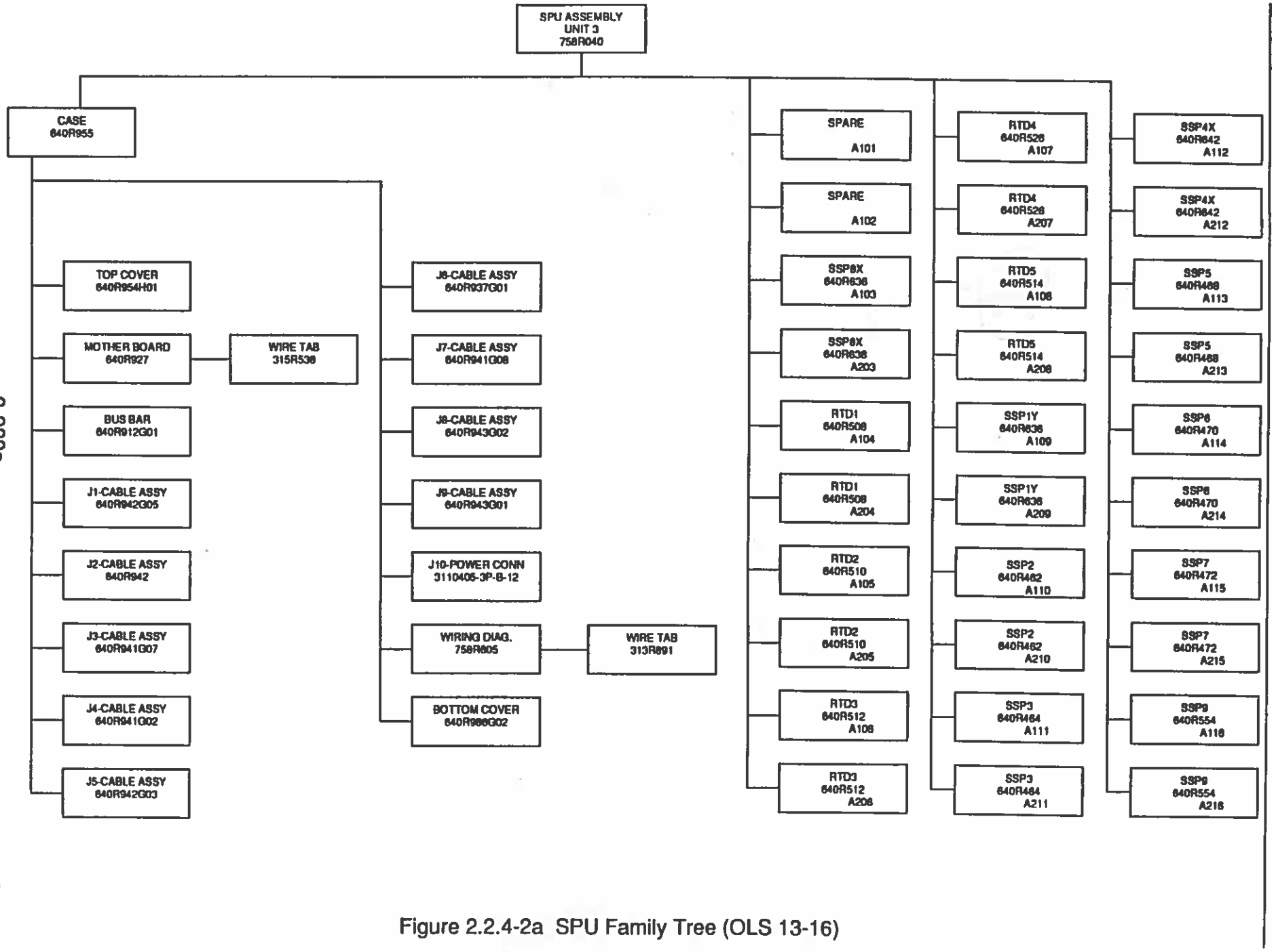


Figure 2.2.4-2a SPU Family Tree (OLS 13-16)

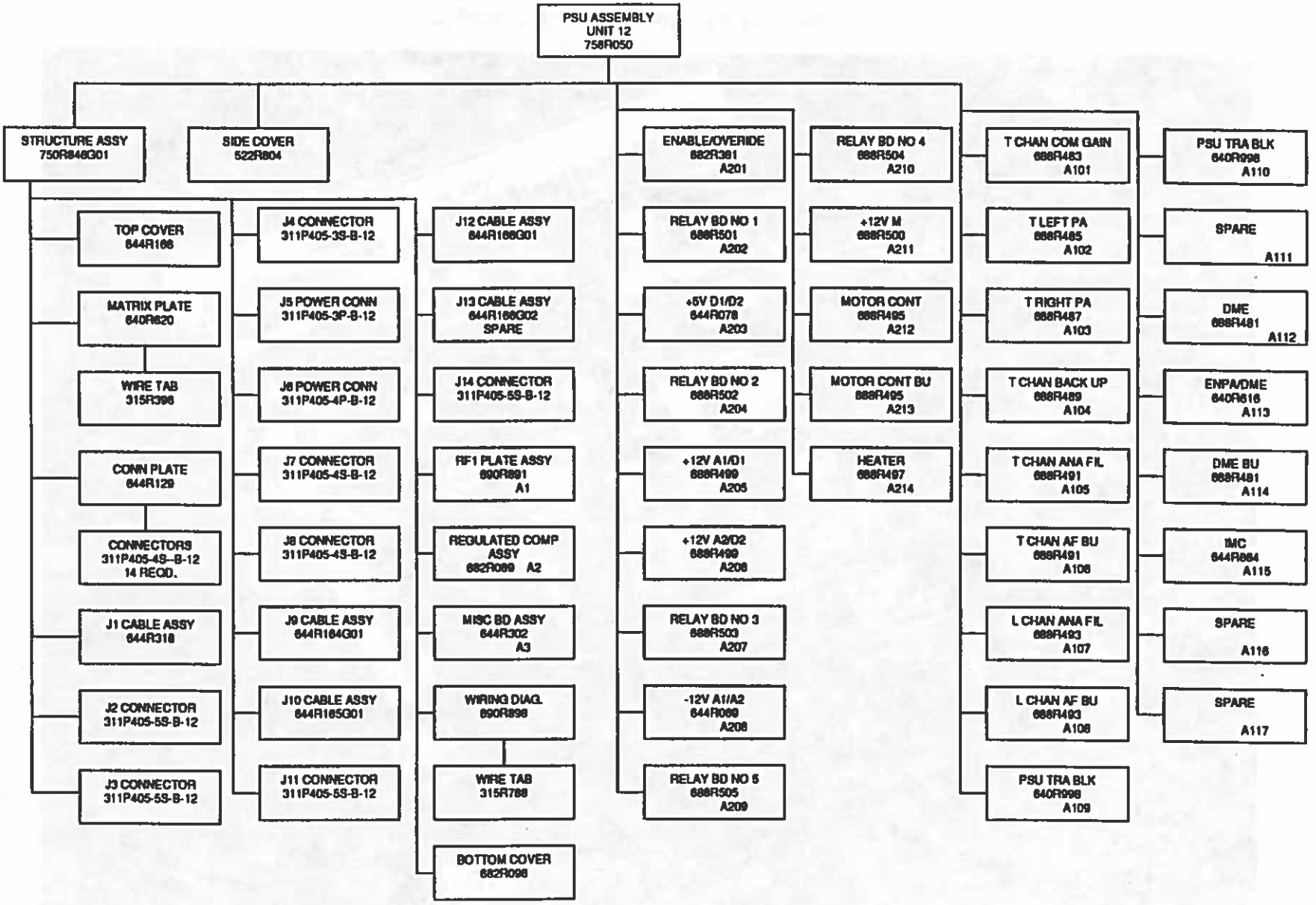


Figure 2.2.5-2 PSU Family Tree (OLS 12)

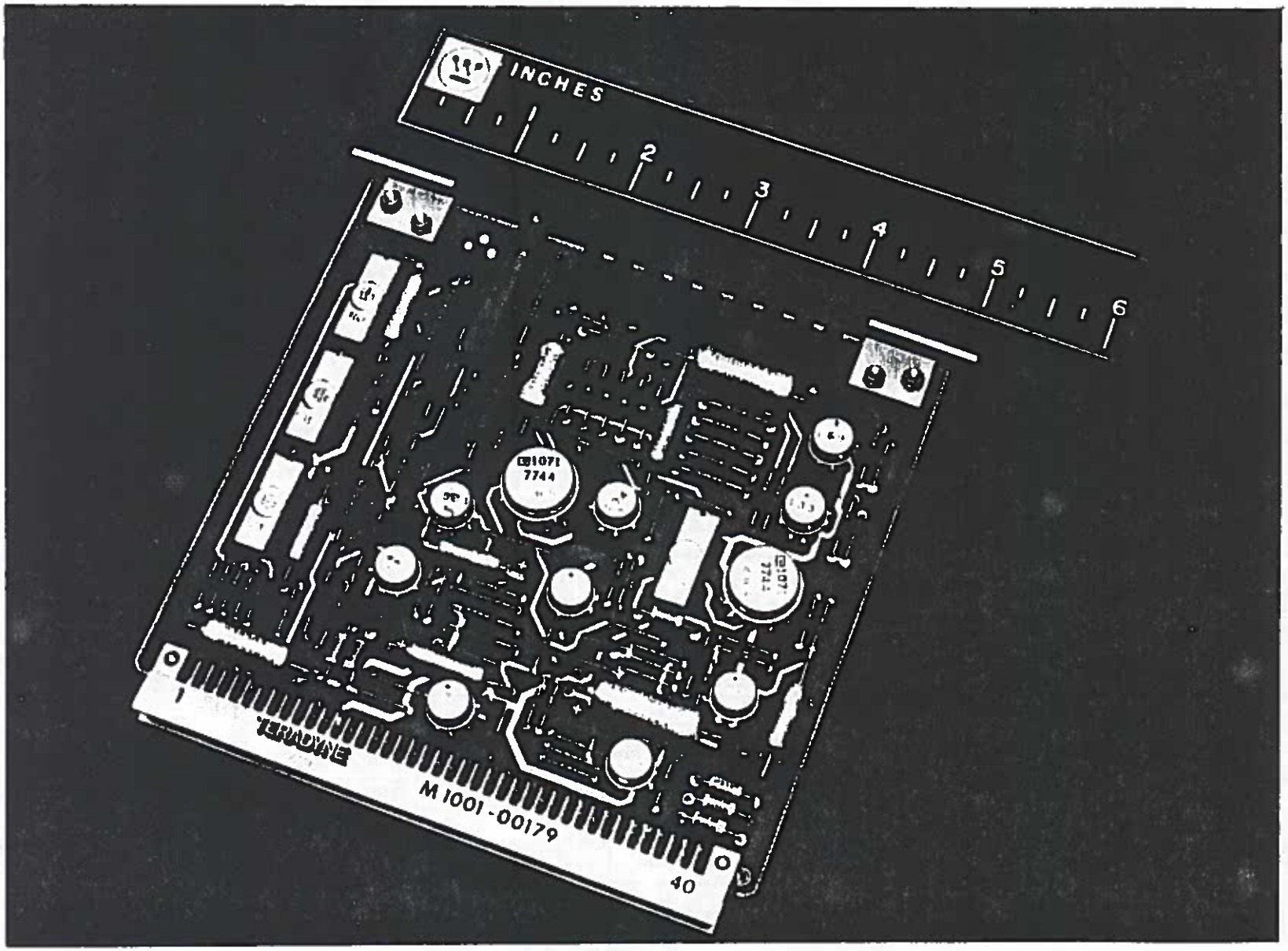


Figure 2.2.5-3. Sample Analog Board

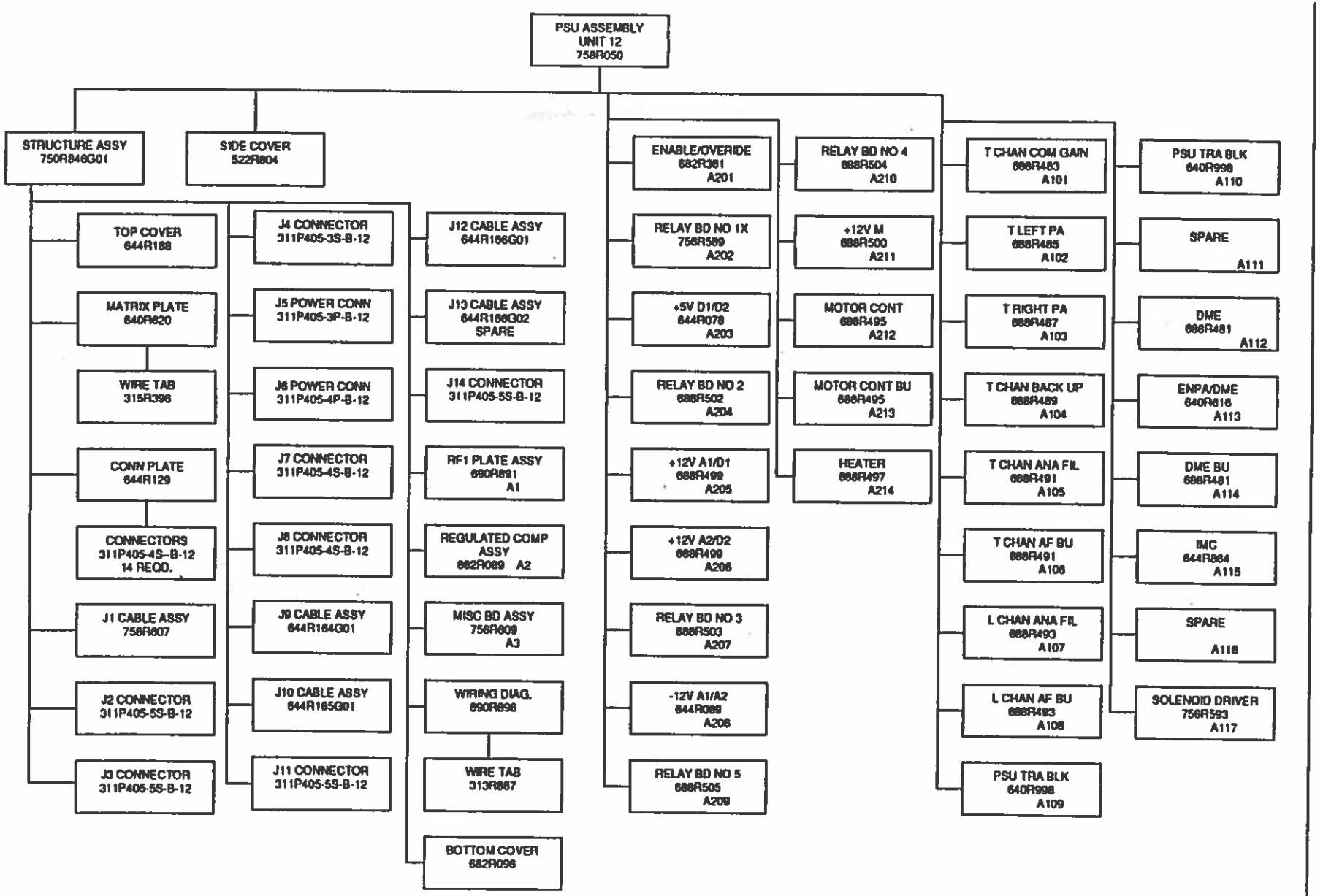


Figure 2.2.5-2a PSU Family Tree (OLS 13-16)

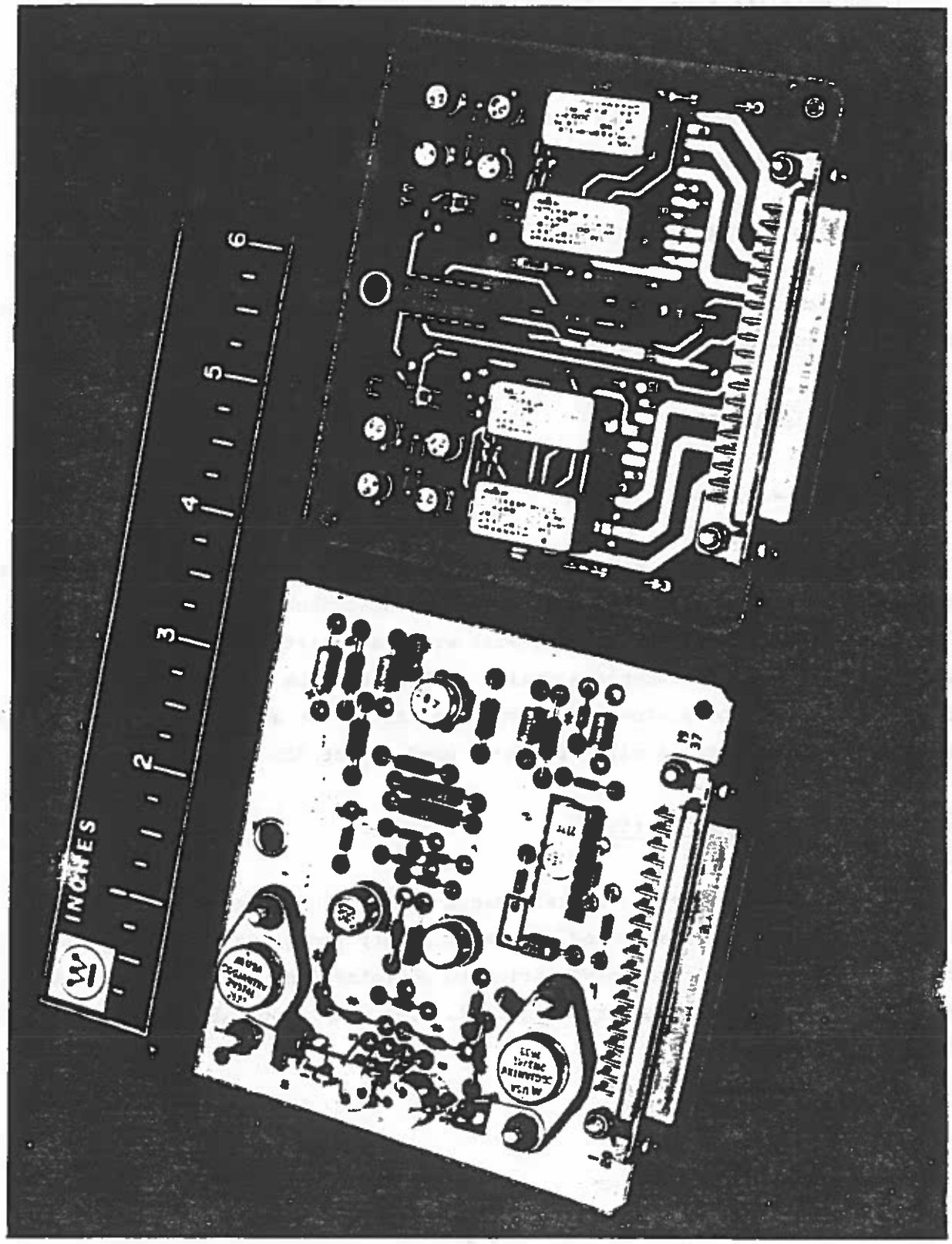


Figure 2.2.5-4. Sample Power Supply Board

2.2.5.3.2 Regulated Component Assembly

High wattage dissipation components, power transistors and resistors associated with the power supply are mounted to another cover of the power supply. This cover has assembled to it the 18 power transistors and 50 associated resistors and capacitors for regulation of the power supply voltages. It also contains the thermistor network used to generate the PSU temperature EST outputs.

2.2.5.3.3 Miscellaneous Board Assemblies

The miscellaneous boards contain 79 components associated with the PSU and contain the system fuses and EST buffer resistors.

2.2.5.4 Interconnection

2.2.5.4.1 Analog Section

The analog boards are connected together via a matrix plate similar to the SPS and SPU except that no bus bar is used to distribute power. All power and signals are distributed through the wire wrapped interconnections on the matrix plate. Wiring between the analog section and the power supply section is provided by two point-to-point wired headers on the analog matrix plate and input/output connectors similar to those used on the SPS and the SPU.

2.2.5.4.2 Power Supply Section

The power supply boards, miscellaneous boards, EMI section feedthroughs, regulated component assembly and all power supply input/output connectors are interconnected by point-to-point wiring to minimize line losses and provide ample current carrying capacity. Figure 2.2.5-5 shows typical matrix plate and PSU wiring.

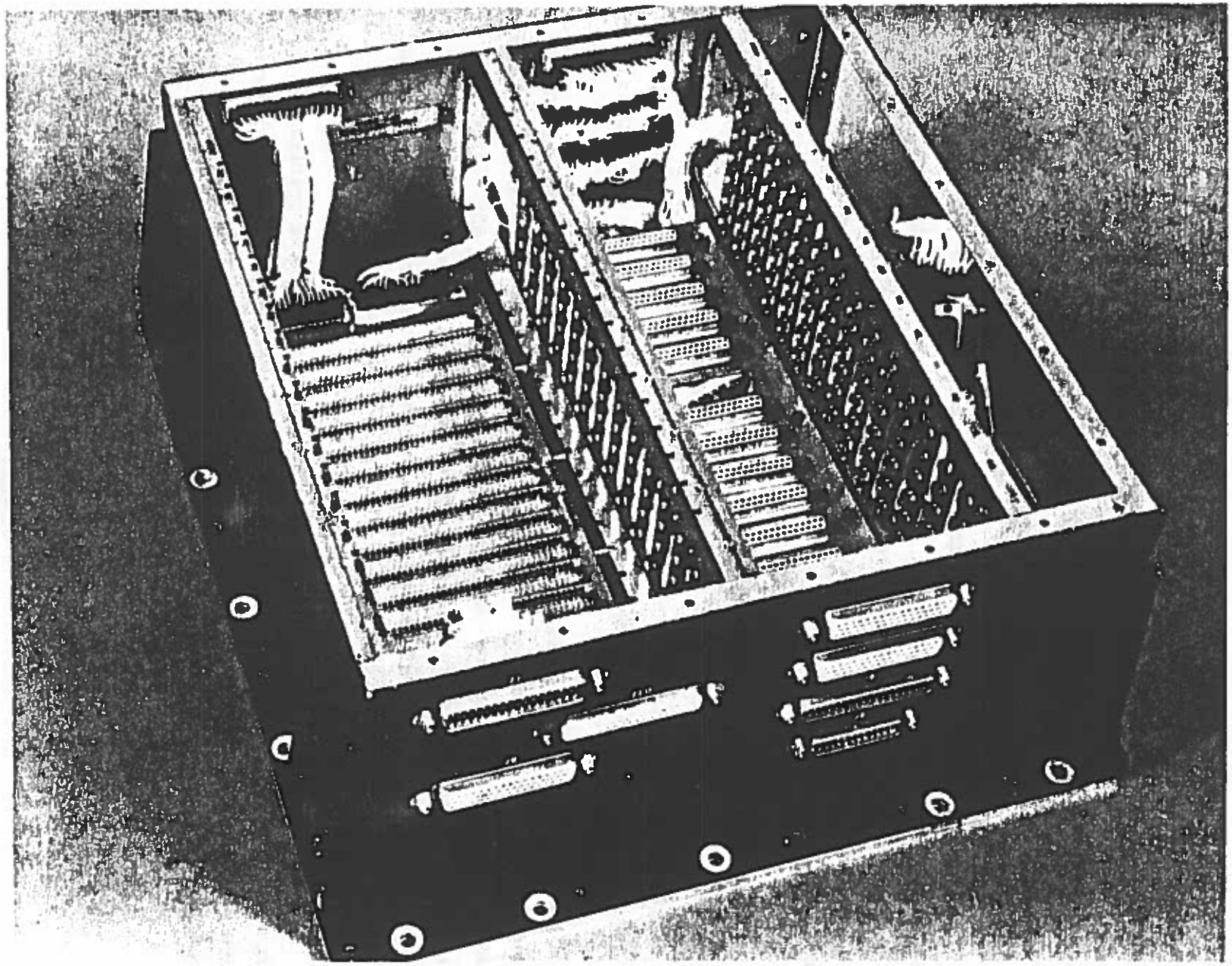


Figure 2.2.5-5 Matrix Plate and Wiring

2.2.5.5 PSU Thermal Control

The power modules, regulated power transistors, and associated components are mounted to the bottom covers which interface with the spacecraft. This provides the minimum thermal path for these high dissipation units. All boards are mounted in the upper two-thirds of the assembly and thermal control is accomplished through conductive cooling from the components through the board thermal plane, the top cover, the structure and then into the spacecraft mounting surface.

From data generated by the PSU mathematical thermal model, at the nominal spacecraft interface temperature of 20°C with full power conditions and both sides up, the predicted component temperatures for typical parts on analog boards will be about 25°C; for parts on power supply boards about 30°C, and for the powercubes about 29°C.

At maximum interface temperature of 30°C and maximum power conditions, the temperature will increase about 12°C above the values stated above.

2.2.6 Output Switching Unit (OSU)

The output switching unit (OSU) channels clear or encrypted data to the spacecraft data transmitters. The OSU also contains redundant clock oscillators and differential drivers for the primary clocks going to the SPS. This assembly integrates two stitch-welded board assemblies, a component assembly, a top cover assembly, a matrix plate, filters and connectors into a functional electronic assembly (Figure 2.2.6-1).

The OSU is an EMI-tight assembly with spacecraft power and critical signals filtered and enclosed in EMI-tight compartments. The OSU is 6.5 inches wide by 9.3 inches long by 3.0 high, weighs a maximum of 3.5 pounds and dissipates 3.6 watts of electrical power.

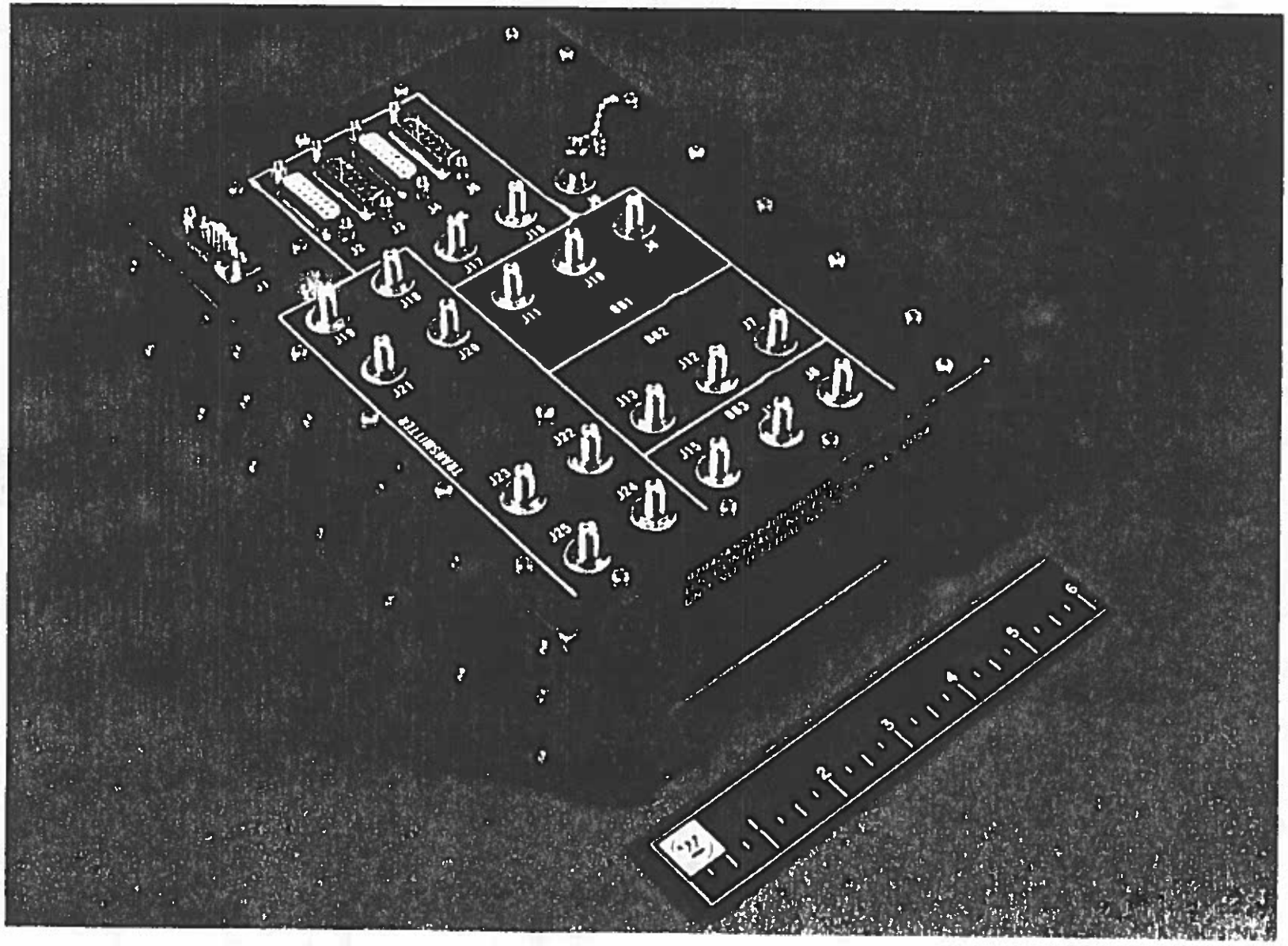


Figure 2.2.6-1. Output Switching Unit

The stitch-welded boards are identical in design and size to those used in the SPS and SPU.

The component assembly is an aluminum chassis used to interconnect four crystal oscillators and their discrete components through insulated standoffs and point-to-point wiring to a plug-in header for matrix plate integration.

The top cover contains the coax connectors wired to a plug-in matrix plate header.

All assemblies are interconnected together through a wire-wrapped matrix plate.

The OSU is mounted on panel 6 of the spacecraft equipment support module (ESM) as shown in Figure 2.2.0-3.

The OSU family tree is shown in Figure 2.2.6-2.

2.2.6.1 OSU Thermal Control

The 5D-2 OSU thermal design is similar to the SPS and SPU thermal design except that there is a slightly longer conductive thermal path from the component to the spacecraft structure due to the horizontal board mounting configuration.

From data generated by the mathematical thermal model of the OSU, at an interface temperature of 20°C and full power conditions, maximum board component temperatures are predicted to be about 75°C and component assembly parts about 36°C.

2.2.7 Encrypters (BBT)

The BBT's are the spaceborne portion of the system which provides cryptographic security for transmissions between the spacecraft and the ground. The three units in the OLS for this purpose are Government Furnished

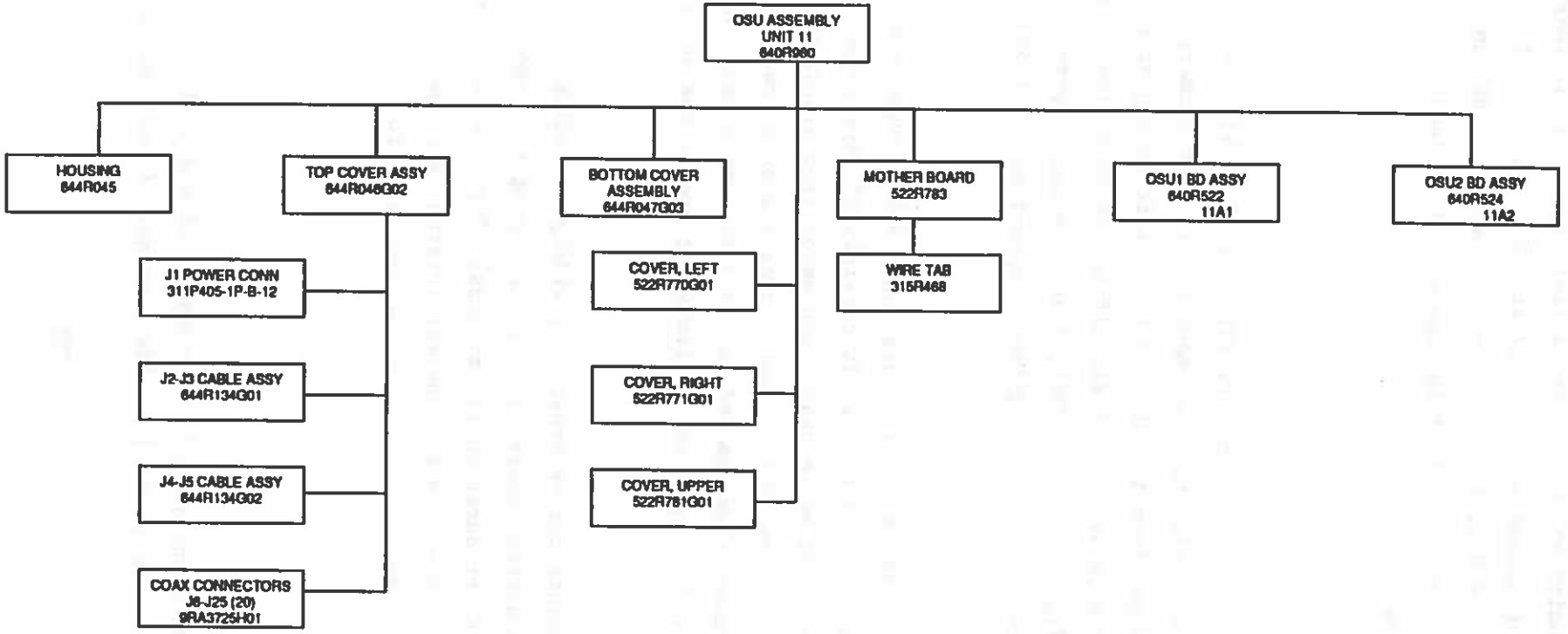


Figure 2.2.6-2 OSU Family Tree (OLS 12)

Equipment (GFE) KG-43 units which encipher serial digital data. They are each 3.87 inches high by 4.56 inches wide by 5.57 inches deep, weigh 3.25 pounds, and dissipate a maximum of 9 watts of electrical power. All BBT units (BB1, BB2 and BB3) are mounted on panel 6 of the spacecraft equipment support model (ESM) as shown in Figure 2.2.0-3.

2.2.8 Tape Recorders

There are four Digital Tape Recorders (DTR1, 2, 3, & 4) in each 5D-3 OLS system and are government furnished equipment (GFE). Each primary recorder receives a digitized input from the SPS and records it on magnetic tape for playback on command at a later time. A simplified expanded view of a tape recorder is shown in Figure 2.2.8-1. DTR1, 2 and 3 mount on panel 4 and DTR4 mounts on panel 3 of the spacecraft equipment support module (ESM) as shown in Figure 2.2.0-3.

Each tape recorder unit is 13.05 inches long, 9.00 inches wide, and 7.12 inches high and weighs about 22 pounds. It consists of tape reels, drive motor, tape guides, read and write heads, and associated electronics encased by a pressure-tight enclosure. The enclosure consists of a brazed assembly incorporating two machined aluminum end panels joined by a thin- walled, sheet metal, tubular section. One end panel is removable and is sealed by means of an O-ring type seal.

The power requirements per recorder vary widely depending on the operational mode, the highest power (44.1 watts) being required for high speed playback which is of short duration (10 minutes). The tape recorder mass acts as a heat sink for such short term transient internal dissipations. Long term average cooling is provided by conduction and radiation to the surrounding spacecraft structure.

2.2.9 Cable Harness

The Cable Harness Assembly (CHA) is composed of a set of all cables necessary to interconnect units of the OLS. The contents of each set are described.

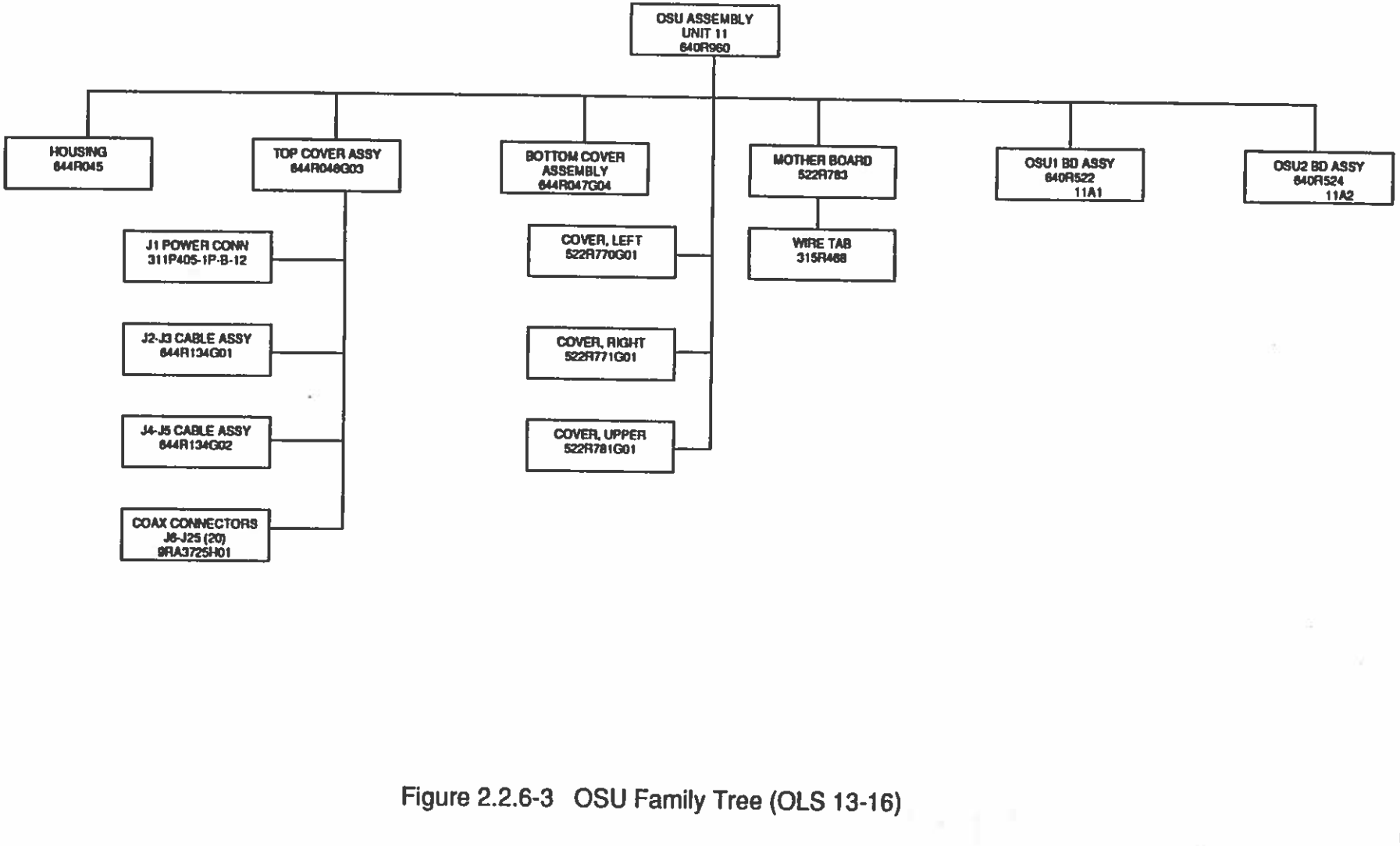


Figure 2.2.6-3 OSU Family Tree (OLS 13-16)

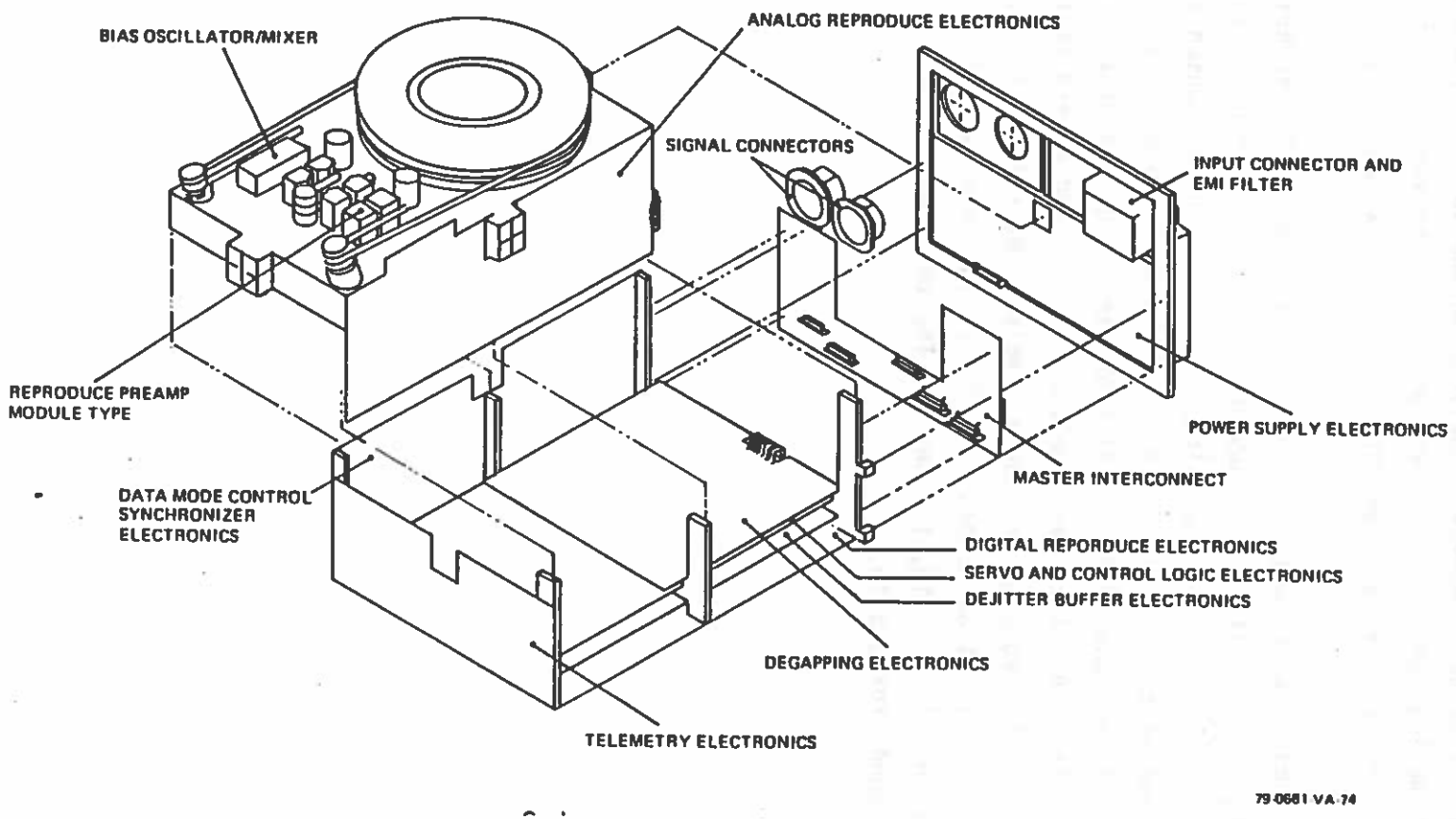


Figure 2.2.8-1. Tape Recorders

There are a total of 17 different coaxial cables with varying lengths and coax connector styles to accommodate routings on the spacecraft and properly interface with mating connectors on each unit. Lengths vary from approximately 6 inches to 18 inches. The total weight of the 17 coax cables is 0.7 pounds.

There are 7 main cables with varying lengths, number of branches, and sizes depending on the units which they interconnect. Their basic construction is the same and consists of contrahelically wound conductors which form the cable bundle over which is installed a metal braided shield and a nylon braided jacket. A multipin connector is provided at the end of each branch. Back shells for the connectors are completely closed and bonded to the metal braided shield of the cable to provide a complete EMI shield. The total weight of the seven cables is 21.30 pounds for OLS 12. The total weight of the seven cables is 24 pounds for OLS 13, 14, and 15. The total weight of the seven cables is 30 pounds for OLS 16.

3. OPERATIONAL CONTROL

Section 3.1 describes the on-board processor and its associated memory. Section 3.2 describes the major tasks performed by the flight software that runs in the on-board processor and Section 3.3 describes the controls the operator has over the OLS which enable it to perform its specific tasks. Section 3.4 describes the telemetry available from the OLS, including the OLS CPU telemetry.

3.1 Internal Processor

This section describes the OLS processor structure, the instruction set, pseudo instructions, number representation, and interpretation of the program listing so that an understanding of the assembly language program instructions can be obtained.

3 1.1 Structure of Processor

The OLS processor is a 16-bit, fractional, two's complement, stored-program data processing unit that uses MSI technology. This processing unit consists of a program and data storage unit, a microprogrammed matrix, eight registers, including four accumulators, and decoding and execution control logic. Figure 3.1.1-1 is a Functional Block Diagram of the unit.

3.1.1.1 Major Processing Components

Each of the major processing components shown in Figure 3.1.1-1 and the abbreviations used are described in the following paragraphs.

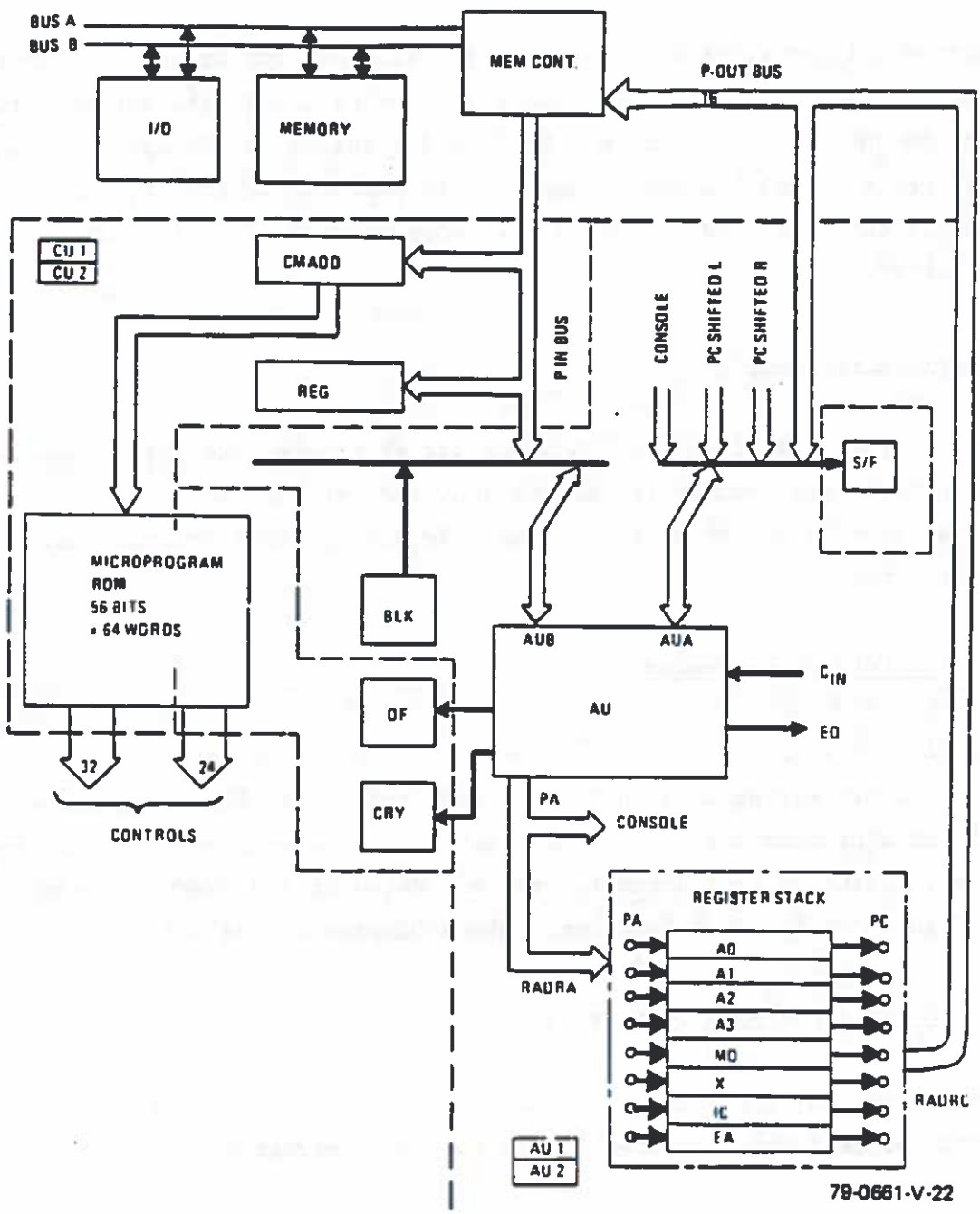


Figure 3.1.1-1. Processor Functional Block Diagram

Memory

The memory consists of 16,384 words of RAM and ROM memory, which is divided into blocks. Each block is made up of 256 16-bit words. The 64 blocks are allocated as follows:

Block Number (Octal)	Number of Words	Type of Memory
0-13	3,072	ROM
14-17	1,024	CMOS RAM
20-77	12,288	CORE RAM

Each instruction fetch from memory cycle takes 2.44 microseconds.

REG

This 3-bit register is used to store the register code that determines which register of the register stack is to be operated on.

CMADD

This 4-bit register is used to address the microprogrammed matrix.

AU

The arithmetic unit (AU) has two entry ports, AUA and AUB, for operands. AUA accepts words from the register stack; AUB accepts words from the memory or an I/O channel. PA is the result produced by the AU. The arithmetic operations used from the available set are:

PA = AUA + AUB	Addition
PA = AUA - AUB	Subtraction
PA = AUA NAND AUB	Boolean NAND
PA = AUA -1	Subtract one
PA = AUA	Copy AUA
PA = AUB	Copy AUB
EQ = 1 if AUA = AUB	Equality
EQ = 0 if AUA AUB	Unequality

The AU sets EQ for every arithmetic operation; it sets CRY and OF when appropriate. The AU can input and output BLK. Cin can be used to add 1 to the contents of the AU.

CRY

This 1-bit carry register is used to store the carry bit during an add, subtract, or divide operation.

OF

A 1-bit overflow register which is set to indicate overflow during an add, subtract, or divide.

BLK

A 16-bit register used to store the block number of memory location being addressed. The high order eight bits serve as an extension of the address field in an instruction word. All 16 bits are used in the XB instruction.

SF

A 1-bit register used with shift instuctions. The SF may be connected to either position 1 or 16 of a register being shifted.

REGISTER STACK

Eight 16-bit registers. A pointer, RADRA, determines which of the eight registers is loaded via input channel PA. Another pointer, RADRC, controls which register is to be routed to channel PC. The eight registers have the following assignments:

A0-A3 Accumulators; i.e., general purpose registers used for holding operands.

MQ Multiply/quotient accumulator - used by multiply or divide instructions to hold parts of the product or dividend.

X Index accumulator - contents are added to the address field of an instruction by the address computation cycle if indexing is specified.

IC Instruction counter - an accumulator reserved by the instruction fetch cycle for holding the address of the next instruction to be executed. Use for any other purpose must be avoided.

EA Effective address accumulator - reserved by the address computation cycle to hold the operand memory location to be referenced.

3.1.1.2 Major Computer Cycles

The execution of an instruction is accomplished by the sequence of steps illustrated in Figure 3.1.1-2.

3.1.1.2.1 Instruction Fetch Cycle

An instruction is fetched from the memory location specified by the IC. Bits 16-13 of the instruction are placed in the microprogrammed address register, CMADD; bits 12-10 are placed in REG; and bits 16-1 are stored on the memory bus. The IC is incremented.

3.1.1.2.2 Address Computation Cycle

The contents of BLK are concentrated with memory bits 8-1 (on the bus) and the result is placed in port AUB. The index is placed in port AUA. The index bit (9) is checked and if it equals 1, the contents of the two ports are added and stored in EA (RADRA = 7). If indexing is not specified, the contents of the AUB are stored in EA.

3.1.1.2.3 Instruction Execution Cycle

The microprogram associated with the instruction sets pointers RADRA and RADRC. The instruction specified in CMADD is then executed. After execution, control is transferred to the instruction fetch cycle.

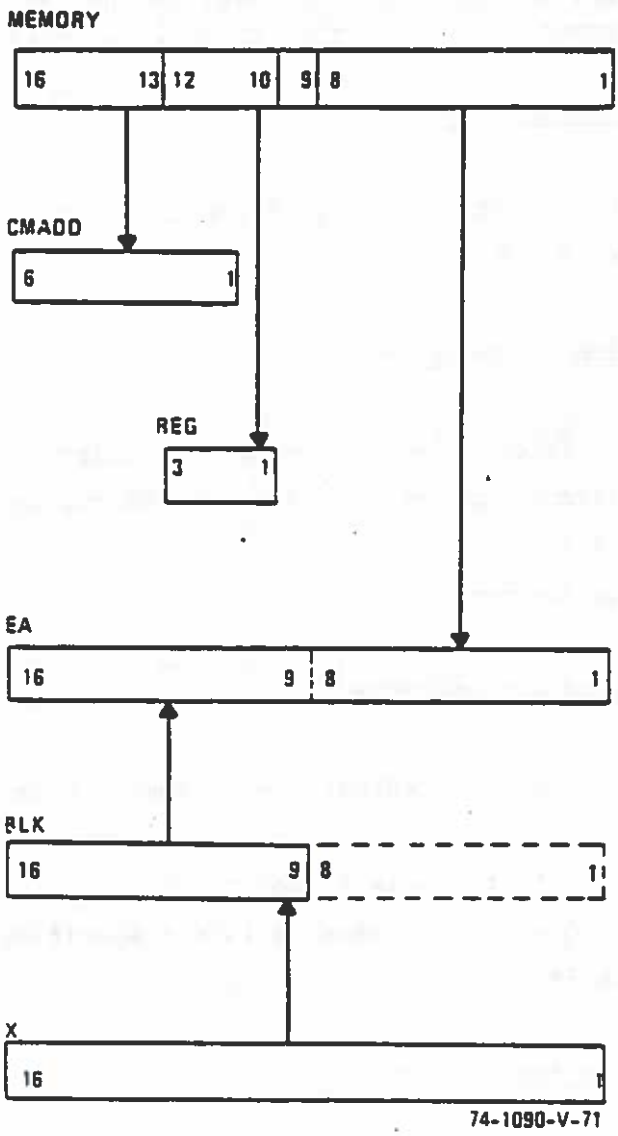


Figure 3.1.1-2. Processor Instruction Field Gating

3.1.2 Instruction Set

The instruction set, which is described in detail in the following pages, includes algebraic, logical, I/O, and control instructions. The multiply and divide instructions are fractional; i.e., each data word has an implied binary point between bit 16 (sign bit) and bit 15. Thus, the product of 1/2 (040000) and 1/4 (020000) is 1/8 (010000), and the quotient of 1/4 (020000) by 1/2 (040000) is 1/2 (040000), where the numbers in parentheses are octal representations of data words. For divides, the numerator must be less than the denominator to avoid divide overflow. Table 3.1.2-1 lists all the computer operation codes, with corresponding mnemonic instruction names.

Table 3.1.2-1. Instruction Codes

Code Octal	Mnemonic	Instruction	Cycles	Time* (usec)
01	XB	Exchange block register	3	3.66
02	SH	Shift	2+N	2.44+
03	SK	Skip	4 (+1 if jump)	4.88++
04	JC	Jump back & count	4 (+2 if jump)	4.88+++
05	J	Jump (inside block)	4	4.88
06	I	Input	5	6.10++++
07	O	Output	5	6.10++++
10	LD	Load	4	4.88
11	ST	Store	4	4.88
12	A	Add	4	4.88
13	S	Subtract	4	4.88
14	M	Multiply	21	25.62+++++
15	D	Divide	54	65.88
16	N	NAND	4	4.88

*Includes indexing and 2.44 usec for the instruction fetch and address computation cycles.
+ Add 1.22 usec for each N bits shifted.
++ Add 1.22 usec for true test on skip.
+++ Add 2.44 usec for true test on jumpback & count.
++++ Add 1.22-4.88 usec if I/O in use by other processor.
+++++ Add 1.22 usec if negative.

3.1.2.1 Instruction and Data Word Formats

In general, an instruction comprises the following information within the microprogrammed matrix.

INSTR

Instruction code field - Four bits to reference an instruction within the microprogrammed matrix.

REG

Register - Three bits to select a register.

X

Indexing indicator - One bit to show that the index register, X, is to be added to the address field in the EA register.

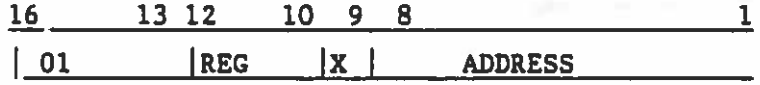
AD

Address field - Eight bits to reference a memory location within a block of 256 locations.

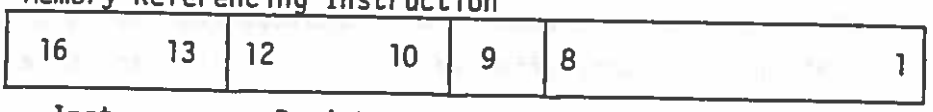
Figure 3.1.2-1 summarizes the various instruction word and data formats.

3.1.2.2 Instruction Descriptions

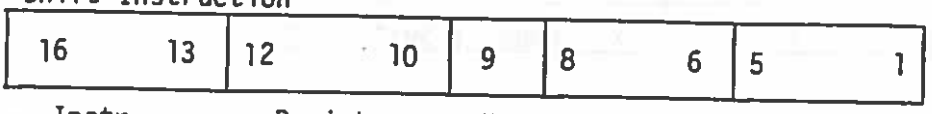
01 Exchange Block Register XB



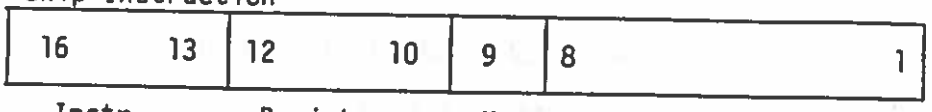
Memory Referencing Instruction



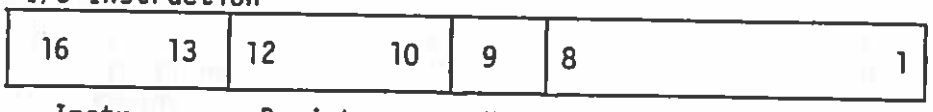
Shift Instruction



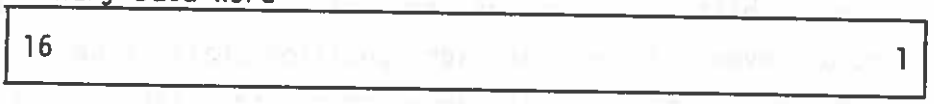
Skip Instruction



I/O Instruction



Binary Data Word

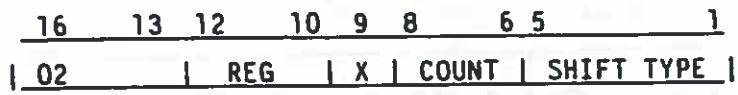


Fractional Data Word

Figure 3.1.2-1. Instruction and Data Word Formats

The contents of the selected register are exchanged with the contents of the block register. Only bits 9 through 16 of the block register are used in address computation. Registers affected: block register and selected register.

02 Shift SH



The five low order bits of the address field, AD, are decoded to determine the type of shift to be performed on the register specified. The shift mnemonics have been assigned the value indicated in Table 3.1.2-2.

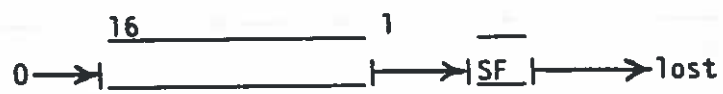
Table 3.1.2-2. Shift Instructions

Mnemonic	Address Field Value (Octal)	Shift Type
SRL	1	Shift right logical
SLL	2	Shift left logical
SRA	5	Shift right algebraic
SRC	11	Shift right cyclic
SLC	6	Shift left cyclic
SRF	21	Shift right Insert shift flag
SLF	22	Shift left Insert shift flag

The count specifies the number of positions the content of the selected register is to be shifted. A count of zero indicates a one position shift while a count of seven indicates an eight position shift. A description is given below for each shift mnemonic. Indexing has no effect on the operation type and/or count.

Registers affected: SF, selected register

SRL Shift right logical



The contents of the selected register are shifted right the number of positions specified by the count. Zeroes enter position 16. Bits leaving position 1 enter SF and bits leaving SF are lost.

SLL Shift left logical

The contents of the selected register are shifted left the number of positions specified by the count. Zeroes enter position 1. Bits leaving position 16 enter SF and bits leaving SF are lost.

SRA Shift right algebraic

The contents of the selected register are shifted right the number of positions specified by the count. The sign bit, position 16, remains unchanged. Bits leaving position 16 enter position 15. Bits leaving position 1 enter SF and bits leaving SF are lost.

SRC Shift right cyclic

The contents of the selected register are shifted right the number of positions specified by the count. Bits leaving position 1 enter both position 16 and SF. Bits leaving SF are lost.

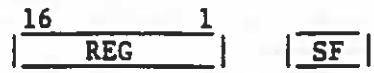
SLC Shift left cyclic

The contents of the selected register are shifted left the number of positions specified by the count. Bits leaving position 16 enter both position 1 and SF. Bits leaving SF are lost.

SRF Shift right, insert SF

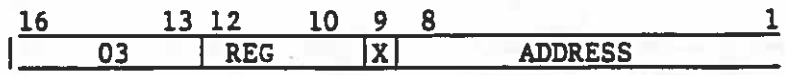
The contents of the selected register are shifted right the number of positions specified by the count. Bits leaving position 1 enter SF. Bits leaving SF enter position 16.

SLF Shift left, insert SF



The contents of the selected register are shifted left the number of positions specified by the count. Bits leaving position 16 enter SF. Bits leaving SF enter position 1.

03 Skip SK



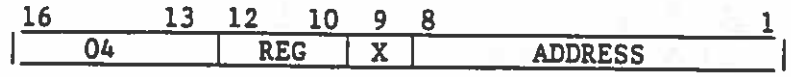
Each bit of the address field specifies a test condition. If any of the conditions specified by the address field are true, the next instruction will be skipped. Tests results are ORed together. A mnemonic has been assigned in Table 3.1.2-3 to the more commonly used conditions. Using these mnemonics, the assembler will automatically generate the correct address field value along with the skip instruction code. Indexing has no effect on the operation type.

Registers affected: none

Table 3.1.2-3. Skip Instruction

Mnemonic	Condition	Address Field Value (Octal)
TLZ	Register selected < 0	1
TEZ	Register selected = 0	2
TLEZ	Register selected ≤ 0	3
TGZ	Register selected > 0	4
TNZ	Register selected ≠ 0	5
TGEZ	Register selected ≥ 0	6
TNS	SF = 0	10
TOV	OF = 1 (overflow)	20
TNC	CRY = 0 (carry bit)	40
TSS	SENSE SWITCH = 1	100

04 Jump back and count JC



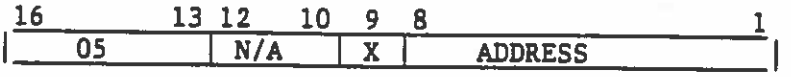
If the selected register is zero, the next instruction is executed. If the selected register is non-zero, the IC is decremented by the lower eight bits of the instruction (the address field) and the selected register is decremented by 1; execution commences at the location specified by the new value of the IC. Indexing has no effect on the address.

Registers affected: IC, selected register.

NOTE

If the initial value of the register selected is N, normally N + 1 passes through the loop will be made.

05 Jump (inside block) J

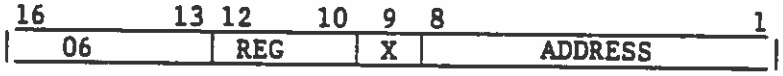


The lower eight bits of the effective address register, EA, are put in the lower eight bits of the IC.

Register affected: IC

NOTE The IC may be loaded, LD, with any 16-bit data value. Thus, a jump may be made to any memory location.

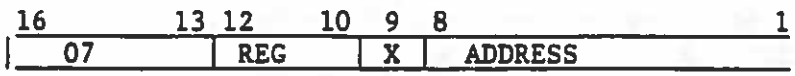
06 Input I



The seven bits of the address field of the instruction serve as a select code to address a particular external input device. The data value from the external input device is placed into the register selected.

Register affected: selected register

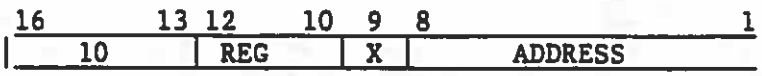
07 Output 0



The seven bits of the address field of the instruction serve as a select code to address a particular external output device. The contents of the register specified is output to the external output device specified.

Registers affected: none.

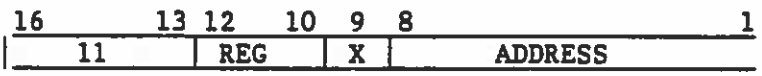
10 Load LD



The contents of the memory location specified by the value of the EA are placed in the register selected.

Register affected: selected register

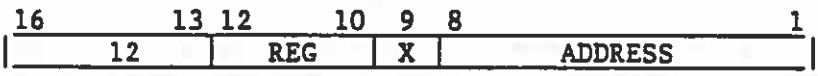
11 Store ST



The contents of the selected register are placed in the memory location specified by the value of the EA.

Register affected: none.

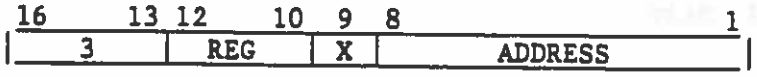
12 Add A



The two's complement sum of the contents of the selected register and the memory location specified by the value of the EA are placed in the register specified. The carry (either 0 or 1) from bit 16 of the adder is placed in the carry flip-flop. If the algebraic sign of the final contents of the register differs from both the original register contents and the memory operand, the overflow flip-flop is set. In the case of no overflow, OF is set to zero.

Registers affected: CRY, OF, selected register

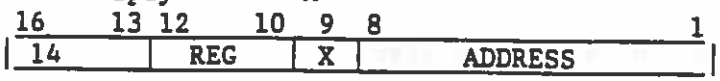
13 Subtract S



The two's complement of the contents of the memory location specified by the value of the EA is formed and added to the contents of the selected register. The sum is placed in the selected register and the carry (either 0 or 1) from bit 16 of the adder is placed in the carry flip-flop. If the algebraic sign of the final contents of the register differs from both the original register contents and the complemented memory operand, the overflow flip-flop is set. In the case of no overflow, OF is set to zero.

Registers affected: CRY, OF, selected register

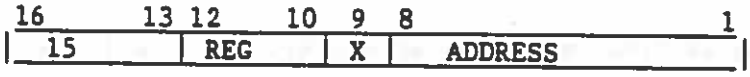
14 Multiply M



The fractional, two's complement product of the selected register and the contents of the memory location specified by the value of the EA are formed. The most significant 16 bits of the 31 bit product are placed in the selected register, and the least significant 15 bits of the product are placed in the high order 15 bits of the MQ register. The least significant bit of the MQ is indeterminate. If the selected register is the MQ itself, the results of the multiplication are indeterminate.

Registers affected: MQ, selected register, SF

15 Divide D



A fractional, two's complement divide is performed with the 32 bit contents of the selected register concatenated with the MQ forming the dividend, and the contents of the memory location specified by the value of the EA forming the divisor. The quotient is placed in the MQ register while the uncorrected

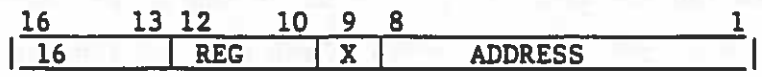
remainder is placed in the selected register. If the absolute value of the selected register is greater than the absolute value of the memory operand, overflow will occur, and the overflow flip-flop will be set. In case of no overflow, OF is set to zero.

If the selected register is the MQ itself, the results of the divide are indeterminate. As a result of the nonrestoring division algorithm used, the quotient may not be exact. If an exact quotient (the quotient may be off by 1 in the least significant bit) or remainder is desired, the approprite correction cycles must be performed.

Registers affected: MQ, OF, selected register, SF

Registers affected: MQ, OF, selected register, SF

16 NAND N



The logical product of the selected register and the contents of the memory location specified by the value of the EA is formed. This product is logically complemented and the result is placed in the selected register.

Register affected: selected register

3.1.3 Interpretation of Program Listing

Each OLS program listing is produced by an assembler. The listing includes the machine code and the assembly language statement for each instruction along with comments for the statements. A description of the assembly language format, number representation, assembler directives and sample program (Figure 3.1.3-1) is included to allow easier interpretation of an OLS program listing.

```
Block No.→ Block Address→ Oper. Code→ Register Code→ Indexing Ind.→ Instr Address→ Operand Block No.→ Label Field→ Command Field→ Operand Field→ Comments→

1 0 5 0 0 0 2 + 1 E6CALC J E6L000 . Put Literal Block in BR
1 1 5 5 0 0 42 + 1 E6CKSS J E6L400 . Get Data Block
1 2 1 7 0 0 1 E6L000 XB EA,E6CB . Initialize First Block to 0
1 3 1 3 0 0 0 XB A3 . Initialize Checksum to 0
1 4 2 3 0 0 2 SLL A3,8 . Words in Block -1
1 5 1 3 0 0 0 XB A3 . Put Data Block in BR
1 6 10 3 0 0 177 + 1 LD A3,(E6DBA) . And Save Test Block
1 7 10 2 0 0 200 + 1 LD A2,(0) . Test Block to BR
1 10 10 0 0 0 200 + 1 E6L100 LD A0,(0)
1 11 10 5 0 0 206 + 1 LD X,(0377) . Compute Checksum
1 12 1 3 0 0 0 XB A3
1 13 11 2 0 0 302 + 33 ST A2,E6BUT . Data Block to BR
1 14 2 2 0 7 2 SLL A2,8
1 15 1 2 0 0 0 XB A2
1 16 12 0 1 0 0 A, A0,0
1 17 2 0 0 11 SRC A0,1
1 20 4 5 0 0 2 JC X,2
1 21 1 2 0 0 0 XB A2
1 22 10 5 0 0 302 + 33 LD X,E6BUT . Store Checksum
1 23 11 0 1 0 0 + 33 ST, A0,E6CKSM . Literal Block to BR
1 24 1 3 0 0 0 XB A3
1 25 2 2 0 7 1 SRL A2,8
1 26 12 2 0 0 203 + 1 A A2,(1-E6DB) . Increment Test Block
1 27 3 2 0 0 5 TNZ A2
1 30 12 2 0 0 201 + 1 A A2,(1)
1 31 12 2 0 0 204 + 1 A A2,(E6DB-0100) . Skip E6DB
1 32 3 2 0 0 2 TEZ A2
1 33 5 0 0 0 40 + 1 J E6L200
```

Figure 3.1.3-1. Sample Program

3.1.3.1 Assembly Language Statement

The assembly language statement is printed on the right-hand side of the listing and constitutes the assembly language format of the source language input. A total of 80 columns can be used to define each statement.

The assembly language statement consists of three main fields: the label field, the command field, and the operand field. A field may be further subdivided into subfields. Generally, fields are delimited by blank characters while subfields are delimited by commas. The type of field is determined by its ordinal occurrence in a symbolic line of code, the first being the label field, the second the command field, and the third the operand field. A complete description of these fields and the syntactic entries which they may contain are presented in the following paragraphs.

3.1.3.1.1 Label Field

The label field entry must start in column 1 with an alphabetic character and contain no more than eight alphameric characters.

3.1.3.1.2 Command Field

The command field starts with the first nonblank character following the terminating blank of the label field. The command field may contain:

A machine instruction mnemonic
An assembly language directive
A procedure reference
A data word

3 1.3.1.3 Operand Field

The operand field starts with the first nonblank character following the terminating blank of the command field. The assembly language formats of the various machine instructions are listed in Table 3.1.3-1. The designations REG and AD refer to a register selected value and an address/ shift type value, respectively.

Table 3.1.3-1. Assembly Language Symbolic Formats

Command ,Field	Operand Field	Significance
A	REG,AD	Add
D	REG,AD	Divide
I	REG,SC	Input
J	AD	Jump in block
JC	REG,AD	Jump back and count
LD	REG,AD	Load
M	REG,AD	Multiply
N	REG,AD	NAND
O	REG,SC	Output
S	REG,AD	Subtract
SH	REG,N	Shift - universal format
SK	REG,AD	Skip - universal format
SLC	REG,N	Shift left cyclic
SLF	REG,N	Shift left, insert shift flag
SLL	REG,N	Shift left logical
SRA	REG,N	Shift right algebraic
SRC	REG,N	Shift right cyclic
SRF	REG,N	Shift right, insert shift flag
SRL	REG,N	Shift right local
ST	REG,AD	Store
TEZ	REG	Test equal zero
TGEZ	REG	Test greater than or equal zero
TGZ	REG	Test greater than zero
TLEZ	REG	Test less than or equal zero
TLZ	REG	Test less than zero
TNC	REG	Test no carry
TNZ	REG	Test non-zero
TOV		Test overflow
TNS		Test no shift flag
XB	REG	Exchange block
TSS		Test sense switch

NOTES: Indexing is specified by placing a comma after the operation mnemonic in the command field.

REG may be any expression with a value in the range 0 through 7

AD may be any expression with a value in range 0 through 255 (0 through 377_8).

N may be any expression with a value in the range 1 through 8 (the actual shift length). The assembler subtracts one to create the 3-bit field in the shift instruction with values 0 through 7.

SC may be any expression with a value in the range 0 through 127 (0 through 177_8) the I/O select code.

3.1.3.1.4 Indexing

If it is desired to set the index bit of a machine instruction word, the machine instruction mnemonic should be immediately succeeded by a comma as in LD, AO, VECTOR.

3.1.3.1.5 Comments

Comments are introduced into the source text by the combination of symbols "period blank" (.). Then, all text to the right of the blank is considered as comments.

3.1.3.1.6 Data Word

If the first nonblank character of a command field entry is other than an alphabetic character, the field entry is regarded as a data word as in +3 or +LD, where +LD is a data word with a value equal to the address of label LD.

3.1.3.1.7 Control Counter Declaration

A maximum of 128 control counters, one for each 256 word block of memory, are used. Each control counter declaration is written as $(E) starting in column 1, where E is the memory block number in octal. The value of E will cause assignment of addresses under that control to proceed upwards from the value 0. The value of a control counter can be set via the RES directive.

3.1.3.2 Number Representation

If the first nonblank character of a command field entry is other than an alphabetic character, the field entry is regarded as a number.

3.1.3.2.1 Octal Number

All numbers preceded by a 0 (zero) are regarded as octal numbers, as in 03777 (right justified).

3.1.3.2.2 Decimal Number

All numbers not preceded by a 0 (zero) are regarded as decimal numbers, as in 3777 (right justified).

3.1.3.2.3 Fractional Numbers

The format of a fractional number in the OLS processor memory is shown below:

There is no characteristic; thus, any fractional result, R, must lie in the range:

$$-1.0 \quad R \quad 1.0$$

The mantissa can contain up to 15 bits of significance. For example, the fractional number 0.5 would be stored in the processor memory as 040000 (octal). S represents the sign bit and negative numbers are represented in two's complemented form.

3.1.3.3 Assembler Directive

Several assembler directives or pseudo-instructions are used to perform various functions during the assembly process.

EQU. If the statement L EQU E is used, the label L is assigend the value of the expression E.

RES. If the statement RES E is used, the value of the expression E is added to the current value of the control counter in effect at the time the RES directive is encountered.

LIST. If the statement LIST is used, the normal mode of assembly is to list all lines assembled. If UNLS is used, LIST is needed to turn the listing on.

UNLS. If the statement UNLS is used, the current and succeeding lines of assembly are not listed until a LIST directive is encountered.

PAGE. If the statement PAGE is used, the assembly listing will be continued on the next page.

3.1.3.4 Sample Program

The following sample program, reference Figure 3.1.3-1, illustrates an assembly language listing. The left-hand side of the listing constitutes the output listing while the right-hand side constitutes the assembly language formats of the source language input. The usage and effect of the various assembler directives and features can be ascertained by studying the output listing along with the comments made.

3.1.3.5 Redundant Processor/Memory

The OLS has both redundant processor and redundant memory that can be placed on line and switched via S/C commands. Processor C and memory E are considered primary. Processor D and memory F are cosidered backup although either can be used as primary, including processor C/memory F and processor D/memory E configurations. Both processors and both memories are identical. An instruction (TSS instruction) has been provided to enable the software to determine which processor is executing the program. The TSS returns a "TRUE" indication if processor C is in control and a "FALSE'' indication if processor D is in control.

Both processors can be on-line at the same time but, to avoid a confused operating state, only one should be executing the operational flight program (OLSP). The other processor can be performing diagnostics, analysis, or algorithms written so as not to interfere with the OLSP.

3.2 AVE Software

This section describes the AVE software development and validation philosophy. The major tasks performed by the software are described and the top level modules performing these tasks are identified. A detailed description of each software module is presented in the Program Maintenance Manual.

The specification to which the software was written and the AVE software source and object code is also presented in the Program Maintenance Manual.

3.2.1 Software Development and Validation

The OLS AVE software has been carried out in four phases: design, development, test, and follow. Figure 3.2.1-1 is a flow diagram of the processes involved.

3.2.1.1 Design Phase

The design phase started with the 5D-2 study task. During this phase, the system requirements were established. Estimates of program size were included and the program specification was prepared. This specification included functional flow diagrams. These diagrams were reviewed by each member of the software design team. A current copy of each functional flow diagram was also provided to the digital design group.

An interface document describing all processor input/output interfaces was prepared by the software design group in coordination with the digital design group.

3.2.1.2 Development Phase

The first project in the development phase was to write a Fortran simulation of the processor I/O for use in testing the flight software. This simulation was verified by inspection and by writing test drivers. The interface document served as the requirements for the I/O simulation.

The flight software was then coded from the functional flow diagrams, assembled, and debugged using the Westinghouse millicomputer cross-assembler on the Univac 1110 computer system. This effort was initially accomplished at the software module level.

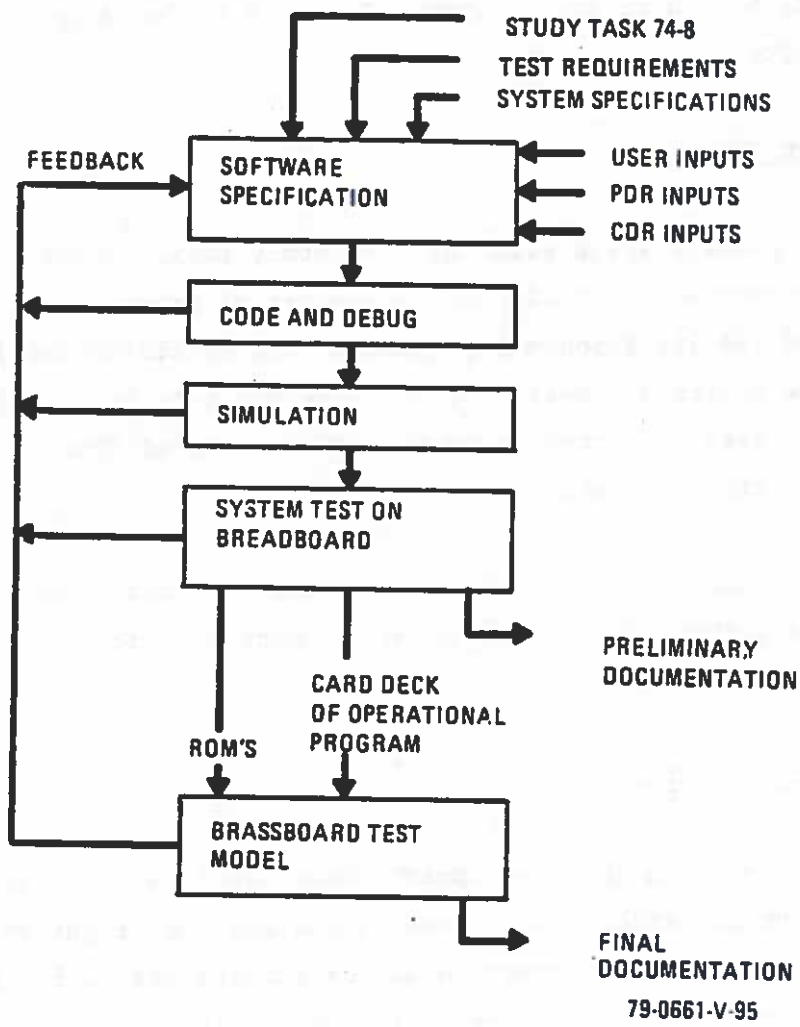


Figure 3.2.1-1. Software Development and Validation

At the same time the individual modules were being developed, a skeleton flight program was written. This program consisted of the EXEC and dummy modules. As each module became debugged, it replaced its dummy in the skeleton program. Simulation testing of the evolving flight software began at this point. The I/O simulator and the Westinghouse millicomputer simulator were used in this simulation testing.

The initial procedure followed during the simulation testing was to force the program into executing each branch at least once but not necessarily all combinations of branches. The simulation was used to supply inputs to and analyze outputs from the operational program. This includes monitoring the processor outputs used to control the L-channel Variable Digital Gain Amplifier (VDGA) gain. This allowed the simulator to compare the actual VDGA gain in the Along Scan Gain Control (ASGC) mode against the desired gain based on location data and scan angle and to compute the error.

Also during the development phase a worst-case timing analysis was conducted and the software was modified to minimize potential timing problems. The software design was reviewed near the end of the development phase. At the completion of the design review and after all action items had been resolved, the design was frozen and the software specification was placed under configuration control.

3.2.1.3 Test Phase

During the test phase, the operational program was loaded into the system breadboard (BTM) for an end-to-end test under a real time environment. The total system was checked against the following documents:

Government

IS-YD-810	5D-2 Spacecraft Interface Specification
IS-YD-821	DMSP Data Specification

Westinghouse

MN315R808	OLS 5D-2 Operator's Manual
ID315R808	Processor-I/O Interface Document
DS315R808	OLS 5D-2 Program Specification

A problem log and schedule were maintained showing problems encountered, the resolution of the problems, and the retest requirements. The test phase was concluded with a final timing analysis.

3.2.1.4 Follow Phase

At the start of the follow phase the documents listed above and also

OLSP01 Card Deck and Listing

were placed under formal configuration control. The software, hardware, and documentation were turned over to the System Test Section for independent and formal system testing. Problems found during system testing are documented on action reports. If the problem solution requires software changes, the change goes through the four phases discussed.

3.2.2 Software Configuration Control

The following items have been placed under formal configuration control. The Operator's Manual is included in Appendix 1.

315R808	OLS 5D-2 AVE Software Top Drawing
S315R808	Software Specification
ID315R808	Interface Document
MN315R808	Operator's Manual
OLSPOX	Card Deck and Listing

Modifications are made to the software as the result of problems encountered in test, system improvement, and customer requests. An approved "change request" (CR) is required to begin a modification. The CR states the modification desired, the reason for modification, the effects on other parts of the system including test, and details the modification design as completely as possible. The CR is circulated to the different design groups (hardware, software, and test) for inputs.

After the software modification has proceeded successfully through its phases of design, development, and test, the software is documented and turned over to the configuration control section with an approved "software change

notice" (SCN). The SCN lists the software documents changed and gives the CR authority for the change. The SCN is circulated to notify all groups.

3.2.3 Software Tasks

The software tasks have been broken down into functional modules. This section provides a general description of these tasks and identifies the modules associated with these tasks. The Program Maintenance Manual gives a detailed description of each module along with their locations in memory. The data base containing constants and variables for the tasks is contained in four modules. V1DB and V2DB contain the data base for the tasks associated with data management and command execution. V3DB and V4DB contain the data base for the tasks associated with the primary sensor (scanner subsystem) control.

3.2.3.1 Loading

Module L1LOAD performs the loading of the operational flight software. This module will also load any other software in any portion of RAM memory. In order to perform load verification, module E6CKSS is called to perform checksum calculations.

The operational flight software also performs program loads as a part of a real time command sequence. These program loads are controlled by D5MAC, which is called by L2UPLK during MAC load sequences.

3.2.3.2 First Orbit Telemetry

The collection of telemetry prior to the loading of the operational flight program is controlled by module L3FOT. This routine calls module L3TEL to collect the spacecraft serialized 2 Kbit telemetry data.

3.2.3.3 Initialization

When the program is initialized, I3INIT is called. This module initializes the processor I/O as well as the data base modules and then calls the executive routine.

3.2.3.4 Executive

Module E1EXEC, which controls the execution of all tasks, is called by the initialization module. E1EXEC is composed of three parts. The first part is the interrupt supervisor in which the I/O is polled according to a priority to determine when tasks need servicing. The second part is a table driven fast scheduler in which a task is pulled from a table for execution. The third part is the table driven slow scheduler in which tasks are also pulled from a table for execution but with a slower service time than with the fast scheduler.

3.2.3.5 Real Time Commanding

Real time commanding is controlled by module L2ACPT. This module accepts: commands and memory load data. Command execution is performed by modules C0-C7 and D0-D7 where C0 refers to the GNC command (CMD0) and D7 refers to the SPC command (CMD017). The command execution modules are called from L2ACPT.

3.2.3.6 Command Verification

Command verification data is downlinked via the spacecraft CVDATA interface. The S/C will accept CVDATA at 4 words per second in the 2-kilobit PIP mode and 20 words per second in the 10-kilobit PIP mode. Module L2DNLK removes command verification data from a 20-word buffer. This data is placed on the CVDATA line when the S/C is ready to accept. Within the CVDATA word is the processor ID bit. Commands received with bad parity have bits 1-15 inverted.

3.2.3.7 Stored Program Commnding

Module M1MMC controls the operation of the main memory program and module M20MC controls the operation of the orbit memory program. These modules call either module C0-C7 or D0-D7, as appropriate for command execution. The time of execution of the stored program commands is controlled by a reference clock maintained by module M40TC.

3.2.3.8 Memory Load/Dump Data

Memory loads of the OLS or mission sensors are controlled with real time commands through modules L1LOAD and D5MAC. All load data is echoed back to the ground.

Memory dump data is defined as that data appearing on the S/C MDDATA interface and consists of program load data, memory load data, memory dump data, and CPU telemetry. When a load or dump is not taking place, CPU telemetry will appear on this interface. The data is separated and identified with sync words and ID words which are defined in the Operators Manual (Appendix 1). Module L1LOAD controls MDDATA for memory loads and memory dumps. Memory dumps are also controlled by module D7SPC, which can be called from L2ACPT, M1MMC, or M20MC. CPU telemetry is controlled by module E4EST.

3.2.3.9 Gain Control

The primary sensor gain control is set up at each positive end-of-scan by module G2PEOS. Gain control calculations are made at each end-of-scan for PGC, ATGC, and ASGC modes in module G1EOS. The ASGC mode requires calculation during active scan to predict the sensor and gain required. These calculations are performed in A1ASGC. If a switch to another sensor is required, that switch is made in S3SNSW. The actual test for a sensor switch is of the highest priority and is located in the executive routine.

3.2.3.10 Constant Spatial Resolution

Module S1SEGS provides control outputs to select detector segments as a function of scan angle. This provides nearly constant spatial resolution across scan.

3.2.3.11 Scanner Offset Correction

Scanner operation is monitored and the resulting information is placed in the CPU telemetry data. Scanner period and scanner offset are calculated in module S1SEGS. The offset information is used to center the data collection about the scanner center of motion.

3.2.3.12 Stored Telemetry Collection

Telemetry from the spacecraft is input in the 2-kilobit PIP mode and placed in the stored data smooth format. The M5TEL routine processes this stored telemetry. Up to 854 bits of telemetry are placed in each stored data smooth line format.

3.2.3.13 Mission Sensor Data Collection

The mission sensors are sampled once per second and placed in the real time data and stored data smooth formats. The M6SSP module performs the mission sensor sampling.

3.2.3.14 CPU Telemetry

CPU telemetry is output via MDDATA at a word rate dependent on PIP mode.

PIP MODE	WDS PER SEC
10 Kbit OLS-DMP	220*
OLS DMP	40
2 Kbit OLS-DMP	40
OLS DMP	4

*220 words per second is the maximum allowable rate; however the OLS software will only produce up to 70 words per second, depending on program loading. A CPU telemetry frame consists of 40 words as follows:

SYNC	123456
SYNC	123456
ID	IOOXXX
CH1	
CH36	
CKSM	

where I = processor ID and XXX defines the telemetry parameter table in use, which will normally be OOO. CPU telemetry processing is performed by module E4EST. Section 3.4 describes the CPU telemetry parameters.

3.2.3.15 Data Formatting

Modules S1SEGS and S2SCOF perform such data formatting functions as defining the location of start and end of active data, wow/flutter region, and nadir. These events are adjusted for scanner offset such that the data sampling is symmetric about the scanner center of motion. Scanner offset can then be treated the same as spacecraft roll.

3.2.3.16 Calibrations and Ancillary Data

The T and L channel calibrations are performed by S1SEGS. The calibration data along with other pertinent data are formatted for the stored data subsync frames by module F1CAL.

3.2.3.17 Location Data Processing

Location data from the spacecraft is input and processed by module S4SASD. Some of this data (lunar and solar azimuth, lunar and solar elevation, lunar phase, and altitude) is used for gain control. All the location data is placed in the subsync stored data frames. The stored data smooth frames always contain a correlated set of location data where the stored data fine frames contain the last value input.

3.2.3.18 Direct Mode Data Message Processing

If the direct mode data message has been commanded on during real time data transmission, this data is removed from stored program memory and placed in the real time data format by module M3DMDM.

3.2.3.19 Data Management

Some functions take a long time to execute. These functions are controlled by the data management routine C8CTIM. Included are memory dumps, recorder monitoring for end of tape and beginning of tape, transmitter warmup, mission sensor and stored telemetry turn-on, recorder and channel turn-off. Since the primary sensor switching test must be made about once per millisecond, any routine taking more than a millisecond must be broken into parts. The execution of the parts is then controlled by C8CTIM.

3.2.3.20 Data Storage

Data can be stored on primary recorders PR1-PR4. The enabling of the formatters, data type, formatter to recorder connection, and records made are controlled by module C3SDC, which is called from L2ACPT for real time commands, M1MMC for main memory commands, and M20MC for orbit memory commands.

3.2.3.21 Data Readout

Data readout consists of real time data performed by module C1RTR or stored data playbacks performed by C3SDC. The module connects the source to the channel destination after the required transmitter warmup. These routines are called from L2ACPT for real time commands, M1MMC for main memory commands, and M20MC for orbit memory commands.

3.2.3.22 Processor Diagnostic

The processor instruction set is tested by module E7DIAS. Module E9DIAG selects the test to be performed and calls E7DIAS. Any errors found are placed

in the system error table. This diagnostic is one of the tasks in the slow scheduler.

3.2.3.23 Memory Diagnostic

Precomputed checksums of all blocks are located in address 0-077 of block 033. Module E6CKSS performs a checksum of a selected block. Module E8CKSM selects the block to checksum, calls E6CKSS, and compares the result with the precomputed checksum. Errors are noted in the checksum error table. Module E8CKSM steps through blocks 0-067 except block 033 and the data blocks V1DB-V4DB. The memory diagnostic is one of the slow scheduler tasks.

3.2.3.24 Error Processing

All system errors, as defined in the Operator's Manual (Appendix 1), are placed in the system error table via module E5ERS. This module also tags the time of occurrence of the error and turns on the processor status word error EST. Checksum errors are time tagged and placed in the checksum error table by E8CKSM. A checksum error also turns on the processor status word error EST. The various error tables can be dumped with an SPC command (module D7SPC).

3.2.3.25 Encoder Simulator

Module S1SEGS uses timing information derived from the encoder control track to control the operation of the encoder simulator. The encoder simulator is locked to the scanner motion and can be used to produce the delphi pulses in the case of an encoder delphi failure. Module S1SEGS will also operate the encoder simulator in a free-run mode in order to format stored telemetry and mission sensor data in the event of a control track failure.

3.2.3.26 OLS Controls

Functional modular redundancy of the I/O and formatter is performed by module D2SGN which is called by modules L2ACPT for real time commands, M1MMC for main memory commands, and M2OMC for orbit memory commands. Module D2SGN also controls the Drive Motor Electronics pulse width.

Controls for the Image Motion Compensation, Photomultiplier Tube Power Supply, Scanner, Encoder Simulator, and T-Channel Cone Cooler Heaters are performed by module C7PSC. Conrols for the Data Transmitter Interlocks, Output Switching Unit, and additional controls on the Data Encryptors and Data Transmitter are performed by module C6TBC. Both of these modules are called by L2ACPT, M1MMC, or M2OMC depending on the source of the command.

3.2.3.27 Load Shedding

Load shedding commands from the spacecraft are input through module S4SASD and executed by module C7PSC.

3.2.3.28 Scanner Protection

Scanner amplitude is computed in module E2EMAX. This module turns off the scanner if the amplitude exceeds a limit which can be redefined by module C7PSC based on real time or stored commands.

3.3 Program Control

Section 3.3 describes the commands necessary to communicate with the OLS and to direct the OLS to perform its various tasks. The first part deals with the spacecraft commands that power and configure the OLS. The second part discusses the commands to the OLS and includes a description of the initial memory load. Also discussed is the diagnostic commanding capability built into the operational flight program.

3.3.1 Spacecraft Commanding

Section 3.3.1 addresses the various controls of the OLS that are available to the ground via spacecraft decoded commands (CIU) and OLS decoded commands, dwelling on the former. Section 3.3.2 will dwell on the later. In addition, to put the S/C commands into perspective a brief discussion on OLS Redundancy and OLS Turn-On examples will be presented.

3.3.1.1 OLS Controls

OLS controls can be basically divided into three areas. They are Power Control, CPU Control and a catch all category as Additional Controls. In configuring an OLS system a proper sequence must be followed in establishing these controls.

3.3.1.1.1 OLS Controls - Power

Power Control requires that the various subsystems desired to be used are connected to the OLS power supply that will be enabled. This function requires the following areas to be addressed:

Processor Power Selection
Memory Power Selection
I/O Power Selection
Formatter Power Selection
Analog Power Selection
Power Enable 1
Power Enable 2
Power Override

3.3.1.1.2 OLS Controls - CPU

CPU Control occurs once the power selection has been successfully completed. It involves connecting the appropriate Processor and Memory via a signal bus, steering the S/C interface signals to the appropriate I/O and loading some executable type program into the RAM portion of Memory. These functions require the following areas to be addressed:

Processor Bus Selection
Memory Bus Selection
Interface Selection
Load Processor
OLS Commands
Processor Load Complete

3.3.1.1.3 OLS Controls - Additional

Additional Controls can occur somewhere during the CPU Control section such as First Orbit Telemetry or after the OLS operational program has been initiated. For the case of configuration, once the operational program has been initiated some additional action may still be required based on the selections made during the Power Control and CPU Control phases. OLS System Generator (SGN) commands may be needed to select the appropriate elements within each subsystem. The OLS SGN command will be discussed in more detail in section 3.3.2. The only other action required before using the command capability offered by the OLS Operational Program is the Drive Motor Electronics Selection. This selection could have been made in either of the two above phases without introducing any problems.

3.3.1.2 OLS Redundancy Summarized

In sections 2.1.2 Analog Signal Processing, 2.1.3 Digital Signal Processing, 2.1.4 Power Supply and 2.1.5 Scanner Monitor and Control, the details of the OLS redundancy for that section were discussed. The following is a summary of that redundancy with respect to command and control.

3.3.1.2.1 OLS Processor and Memory Units

There are two OLS Processors - C and D.

There are two OLS Memories - E and F.

A Processor and A Memory are connected by a Bus - either A or B.

When one Processor is connected to Bus A, then the other Processor is connected to Bus B.

When one Memory is connected to Bus A then the other Memory is connected to Bus B.

Eight possible combinations exist.

A Processor can be connected to either power supply and this automatically connects the other processor to the other power supply.

A Memory can be connected to either power supply and this automatically connects the other Memory to the other power supply.

Both Processors and both Memories cannot be connected to the same power supply but both can be used if both power supplies are ON.

3.3.1.2.2 OLS Input/Output Units - I/O X and Y

Each I/O contains the following functions which can be selected from either I/O if both I/Os are powered:

Spacecraft Interface (I/F)- via "IFSEL" S/C commands
Clock Drivers (CLKS)
Gain Control (GAIN)
Sensor Control (SENS)
Encoder and Wow/Flutter Processor (W/F)
Output Data Multiplexing (ODM)
} via SGN OLS commands

An I/O responds to processor commands via either Bus A or Bus B.

It does not matter to the I/O which processor, memory and bus combination is selected.

An I/O can be connected to either power supply.

Both I/Os can be connected to the same power supply.

The OLS initializes to the I/O X functions (except S/C I/F) upon power turn-on.

3.3.1.2.3 OLS Formatter Units - Formatter G and H

Each Formatter contains the following functions which can be selected via SGN commands from either formatter if both formatters are powered:

Special Sensor Processor (SSP)
Real Time Data Formatter (RTD)
Stored Data Fine Formatter (SDF)
Stored Data Smooth Formatter (SDS)

It does not matter to the formatter whether one or both I/O units are powered or which processor, memory and bus combination is selected.

A formatter can be connected to either power supply.

Both formatters can be connected to the same power supply.

The OLS initilizes to the Formatter G functions upon power turn-on.

3.3.1.2.4 OLS Analog Processing

In the analog section of the OLS, for each detector type, redundancy exists past the Postamplifier. Both the primary and redundant paths are powered by the same power supply, either PS1 or PS2, hence the appropriate selection needs to be made. The analog filter, fine and smooth, outputs may be selected (independently for L and T) via SGN commands from either the primary or redundant paths. The OLS initializes to the primary set of filters, which requires no additional action unless a failure occurs in the primary path for either L or T. In addition the HRD postamplifier is selectable. In section 3.3.2 additional backup capability will be discussed for each detector via the GNC command.

3.3.1.2.5 OLS Scanner Monitor and Control

Two of the three Encoder signals that provide scanner position data can be generated by either of two different sets of detectors and electronics. They are the control track and nadir signals. This selection featu'e is via the SGN command and is independent of other configuration choices. The OLS initializes to the primary FID and AUX implementation (see section 2.1.5), which requires no additional action unless a failure occurs in this area. In section 3.3.2 additional backup capability will be discussed for the third signal, delphi track, via the PSC command.

Two redundant sets of Drive Motor Electronics (DME) are provided for scanner control. Both DME A and DME B are powered whenever the OLS has power enabled. However, in a turn-on sequence, the optimum time to select the DME using the DME SEL S/C commands is prior to power enable.

There are two types of DME pulse drive output selectable by the SGN command during the scanner start-up phase. The SGN primary output is a wider pulse for ground testing (AIR) and the SGN redundant output is a narrower

pulse for operational use (VAC). The operational program initializes to the VAC pulsewidth, which requires no additional action for on-orbit operations unless scanner startup difficulties are experienced. (This is the only case when the operational program initializes to the SGN redundant case and the reason is the on-orbit operational primary position is the SGN redundant case.)

3.3.1.2.6 OLS Power Supply - PS1 and PS2

There are two separate and independent supplies, each of which is capable of supplying power to the entire system, minus the second processor and memory. Hardware design automatically inhibits the connection of two processors and/or two memories to the same power supply. Although normal operational requirements only use one supply at a time, both can be enabled simultaneously.

3.3.1.3 Sources of OLS Controls

The following areas will be discussed in detail:

Power Control via Spacecraft Commands
CPU Control via Spacecraft Commands and OLS Commands
Miscellaneous Control via Spacecraft Commands
OLS System Selection via OLS System Generator (SGN) Commands

Spacecraft commands are CIU decoded, level and pulse, discretes that interface with the OLS PSU and OLS SPS RED/BLACK Interface Units. OLS commands are OLS decoded spacecraft commands. The CIU transfers 16-bit words, MSB first (bit 16), to the OLS SPS RED/BLACK units via the COMDAT interface signal.

3.3.1.3.1 OLS Power Control via Spacecraft Commands

Table 3.3.1-1 lists all commands that result in a power configuration action. The Nomenclature column defines the interface signal name. The Function column gives the results of the signal as well as indicating for level discrete interfaces the state of the signal at the OLS interface. The Signal Type and Switch Type columns are self-explanatory.

Table 3.3.1-1. OLS Power Control (S/C CMMDS)

NOMENCLATURE	FUNCTION	SIGNAL TYPE	SWITCH TYPE
Power Enable 1	On (Low)/Off (High) of PS1	Level	
Power Enable 2	On (Low)/Off (High) of PS2	Level	
Power Override	On (Low)/Off (High) of PS1 and PS2	Level	

When OLS Power Override (OPO) is commanded to a high level, the power supplies shall automatically turn off if the +28 volt regulated input bus voltage rises to 31±1 volt. When OPO is commanded to a low level, automatic turn off shall be disabled.

Processor PWR SEL 1	PROC C - PS1 PROC D - PS2	Pulse	Magnetically latched Relay (MLR)
Processor PWR SEL 2	PROC C - PS2 PROC D - PS1	Pulse	MLR
Memory PWR SEL 1	MEM E - PS1 MEM F - PS2	Pulse	MLR
Memory PWR SEL 2	MEM E - PS2 MEM F - PS1	Pulse	MLR
IO X PWR SEL 1	IO X - PS1	Pulse	MLR
IO X PWR SEL 2	IO X - PS2	Pulse	MLR
IO Y PWR SEL 1	IO Y - PS1	Pulse	MLR
IO Y PWR SEL 2	IO Y - PS2	Pulse	MLR
Form G PWR SEL 1	Form G - PS1	Pulse	MLR
Form G PWR SEL 2	Form G - PS2	Pulse	MLR
Form H PWR SEL 1	Form H - PS1	Pulse	MLR
Form H PWR SEL 2	Form H - PS2	Pulse	MLR
Analog PWR SEL 1	Analog Loads - PS1	Pulse	MLR
Analog PWR SEL 2	Analog Loads - PS2	Pulse	MLR

3.3.1.3.2 OLS CPU Control via Spacecraft Commands and OLS Commands

Table 3.3.1-2 lists all commands that result in a processor and memory configuration. The OLS Command interaction will be discussed later in this section as well as in more detail in section 3.3.2.

3.3.1.3.3 OLS Miscellaneous Control via Spacecraft Commands

Table 3.3.1-3 list all commands used for DME Selection, First Orbit Telemetry (FOT) and Deployables.

3.3.1.3.4 OLS System Selection via OLS System Generator (SGN) Commands

Table 3.3.1-4 list all the functions controllable by the OLS SGN command.

3.3.1.3.5 OLS Mode of Operation Control via OLS Commands

Although these areas will be discussed in more detail in section 3.3.2, they are mentioned here for completeness.

Sensor mode control is provided by the GNC and PSC commands
Data control & management is provided by the RTR, SDC and TBC commands
Special sensor processing is provided by the SSC command

Stored program control is provided by the OCP, UPC and MAC commands
Dynamic stored program capability is provided by the AIS command
Operational program diagnostic reporting is provided by the SPC command

Table 3.3.1-2. OLS CPU Control (S/C CMMDS)

NOMENCLATURE	FUNCTION	SIGNAL TYPE	SWITCH TYPE
Processor BUS SEL 1	PROC C - BUS A PROC D - BUS B	Pulse	Reset-Set Latch (RSL)
Processor BUS SEL 2	PROC C - BUS B PROC D - BUS A	Pulse	
Memory BUS SEL 1	MEM E - BUS A MEM F - BUS B	Pulse	RSL
Memory BUS SEL 2	MEM E - BUS B MEM F - BUS A	Pulse	
IFSEL 1	Enable (Low)/ Disable (High) (R/B X, IOCLKX, SGNREGX)	Level	RSL
IFSEL 2	Enable (Low)/ Disable (High) (R/B Y, IOCLKY, SGNREGY)	Level	
Load PROC C	See Below	Level	RSL
PROC C Load CMPT	See Below	Pulse	
Load PROC D	See Below	Level	RSL
PROC D Load CMPT	See Below	Pulse	

A low level from the spacecraft on LOAD PROC-J shall cause the OLS processor J to go to instruction count zero, thereby remaining reset. A high level following a low level from the spacecraft on LOAD PROC-J shall cause the OLS processor to accept and load the software program(s) that shall be transferred as the next information on COMDAT or execute First Orbit Telemetry if a FOT CMMD is next. A pulse from the spacecraft on PROC-J LOAD CMPT shall cause the OLS to:

(J = C or D)

A) Execute the Operational program
or B) Become idle looking for another load processor sequence
or C) Perform a checksum verification and then do (B)
or D) Go to some specified location and execute code
or E) Terminate First Orbit Telemetry and then do (B)

dependent on what occurred on the COMDAT input between the time load PROC J went HIGH to the occurrence of PROC J Load CMPT pulse occurred.

Table 3.3.1-3. OLS Miscellaneous Controls (S/C CMMDS)

NOMENCLATURE	FUNCTION	SIGNAL TYPE	SWITCH TYPE
DME A SEL	Connect DMEA to Scanner Motor	Pulse	MLR
DME B SEL	Connect DMEB to Scanner Motor	Pulse	
PFOT	See Below	Level	

When Primary First Orbit Telemetry (PFOT) is commanded to a high level with the processor in the loader, telemetry will be recorded using PR1. When PFOT is set low, PRI will begin playback through channel 1 - clear using PDT1.

BFOT	See Below	Level	

When Backup First Orbit Telemetry (BFOT) is commanded to a high level with the processor in the loader, telemetry will be recorded using PR3. When BFOT is set low, PR3 will begin playback through channel 2 - clear using PDT2.

SSS Scanner Cage Squib 1	Release Scanner Caging	Pulse
SSS Scanner Cage Squib 2	Release Scanner Caging	Pulse
SSS Cooler Cover Squib 1	Deploy T Cooler Cover	Pulse
SSS Cooler Cover Squib 2	Deploy T Cooler Cover	Pulse
SSS Optics Cover Squib 1	Deploy Optics Cover	Pulse
SSS Optics Cover Squib 2	Deploy Optics Cover	Pulse

Table 3.3.1-4. OLS System Configuration (OLS CMMDS)

The OLS Operational Program must be running to receive OLS commands.

The OLS SGN commands provide the ability to select Primary or Redundant Functions:

Within the I/O section they are:

Clock Drive X (Primary) or Y (Redundant)

Sensor Control X or Y

Gain Control X or Y

Wow/Flutter and Encoder Processor X or Y

Output Data Mux X or Y

Within the Formatter section they are:

SSP Formatter G (Primary) or H (Redundant)

RTD Formatter G or H

SDF Formatter G or H

SDS Formatter G or H

Within the Analog section they are:

L Video Output (Primary or Redundant)

T Video Output (Primary or Redundant)

HRD Post Amp (Primary or Backup)

Within the Encoder section it is:

FID and AUX Encoder (Primary or Redundant)

Within the Scanner Drive System it is:

DME Startup AIR (Primary) or VAC (Redundant).

The OLS GNC commands provide additional fallback capability.

The OLS RTR, SDC and TBC provide multiple data output paths.

3.3.1.4 OLS Configuration

The following paragraphs cover OLS turn-on flow configuration rules and examples of varios turn-on sequences.

3.3.1.4.1 Configuration Flow for Turn-On

Initially, the power control commands should be used to connect all the subsystems that are desired to be used to one of the two OLS power supplies that will eventually be enabled. This requires at least a Processor, a Memory, an I/O, a Formatter, and the Analog subsystem. The devices not required should be connected to the power supply that will not be enabled to minimize the power consumption.

In order to insure an orderly power up sequence, the IFSEL 1 and 2 should be selected so that the interface that is not desired is disabled and the one that is desired is enabled. For a single powered I/O system, IFSEL 1 is required when I/O X will be powered and IFSEL 2 is required when I/O Y will be powered. Also it is necessary to enable the LOAD PROC signal associated with the Processor connected to the power supply that will be enabled. This will keep the Processor at instruction count zero while power is applied allowing the hardware to keep all buses in the logic zero state and the vaious power reset circuits to keep all registors and flip-flos strobed to the off state.

Next the desired power supply is enabled, followed by no other commands to the OLS for at least one second to allow all voltages to stabilize. Then, the Processor and Memory that are powered have to be connected via Signal Bus A or B. This requires the appropriate Processor bus selection and Memory bus selection commands to be executed. This has to occur after power enable since the steering logic and switches are integrated circuits, not magnetically latched relays. At this point a system has been configured with the Processor at instruction count zero and the turn on now can branch to one of three different states. (See the flow diagram below of Figure 3.3.1-1.)

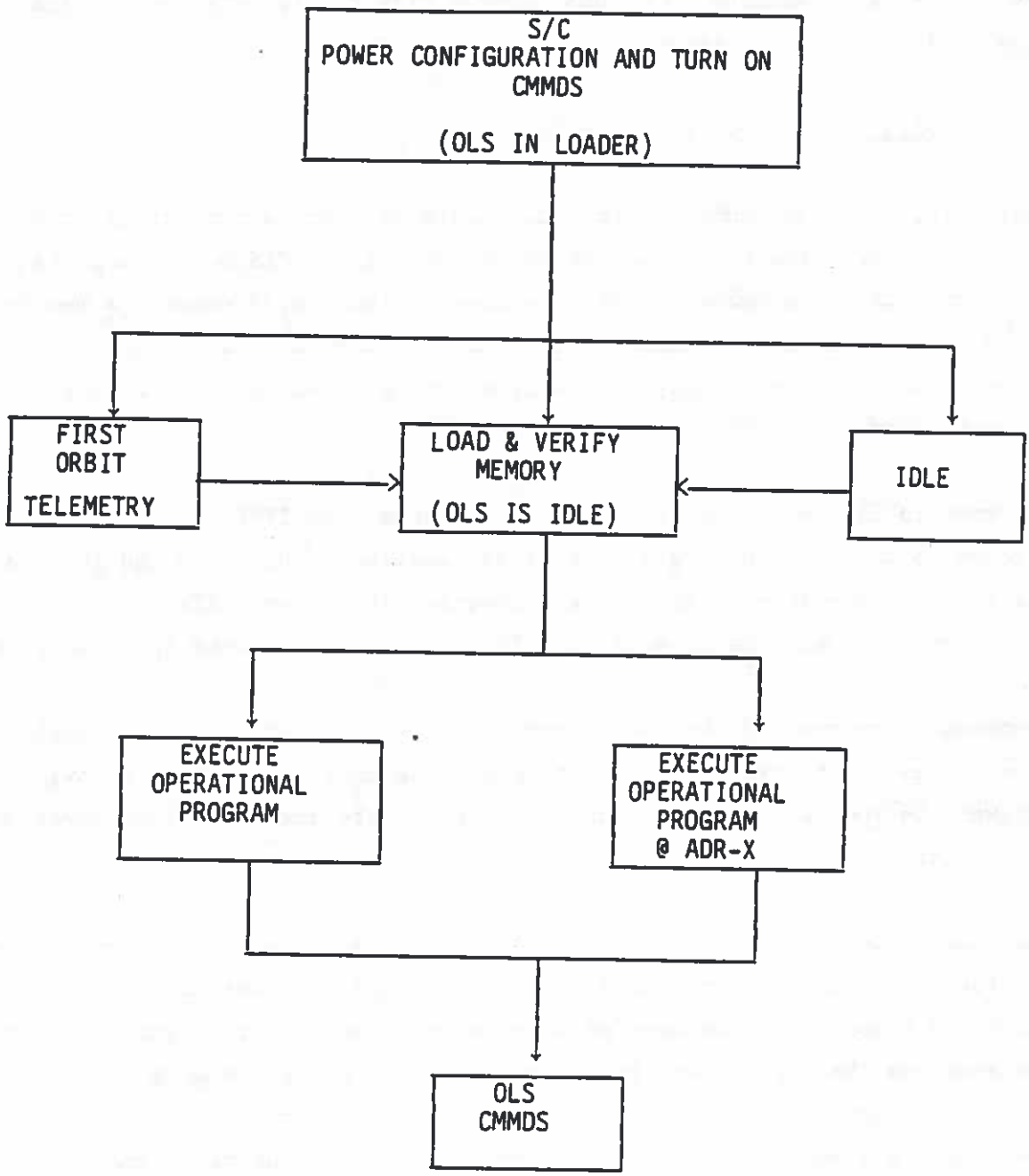


Figure 3.3.1-1. OLS Turn-On Flow Configuration

The second level of the flow diagram deals with Processor commanding which is described next. For the purposes of this section (3.3.1) the basic Processor command sequences are defined below. In section 3.3.2 additional sequences will be described as well as the sync words, ID words, and address words and program data. Commanding for First Orbit Telemetry will be discussed in section 3.3.1-5.

To Load Memory and Verify Memory - Resulting in an Idle Condition

LD PROC J - LOW
LD PROC J - HIGH
OLS CMMDS - Sync, Sync, ID, ADR, Program Data
PROC J LOAD CMPT

To Verify Memory - Resulting in an Idle Condition

LD PROC J - LOW
LD PROC J - HIGH
OLS CMMDS - Sync, Sync, ID
PROC J LOAD CMPT

This sequence is required after a Load and Verify because of a ground system limitation in acquiring the automatic verification checksum following the load echoes.

To Execute Operational Program with Automatic SGN to Primary Side - Once Verified

LD PROC J - LOW
LD PROC J - HIGH
PROC J LOAD CMPT

To Execute Operational Program with Automatic SGN to Redundant Side - Once Verifed

LD PROC J - LOW
LD PROC J - HIGH
OLS CMMDS - Sync, Sync, ID, ADR = 010006_8
PROC J LOAD CMPT

3.3.1.4.2 Configuration Rules

The statements below provide help in configuring an OLS system.

A Processor in the idle mode is looking for a Load processor flag in order to enter the loader. The Load processor J flag is set by the command LD PROC J-LOW whch also locks processor J. Both processor C and processor D Load flags should not be on at the same time unless at least one of the processors is locked. Both load flags must be off after the reconfiguration. The LD PROC J HIGH command unlocks the processor and allows it to enter the loader sequence. The PROC J LOAD CMPT command resets the Load processor J flag and performs the action which is a function of the intervening OLS CMMDS as shown below where the ID can contain any value:

```
Sync, Sync, ID, Adr, Data     - Load and verify
Sync, Sync, ID, Adr           - start execution at adr
Sync, Sync, ID                - verify and return to idle
Sync, Sync                    - Idle
Sync, Non-Sync                - Idle
Sync                          - Idle
no OLS CMMDS                  - Start execution - Primary Side
```

A Processor in the Loader is looking for:

FOT CMMD
Header CMMDS via COMDAT Interface
Processor Load CMPT Pulse

Power

At least a Processor, a Memory, an I/O, a Formatter, and the Analog subsystem must be powered.

Only one Processor can be connected to a power supply.
Only one Memory can be connected to a power supply.

One or both I/Os can be connected to a power supply.
One or both Formatters can be connected to a power supply.
Devices desired to make up a system obviously have to be connected to a power supply that will be enabled.

Do not connect a device to a PS that is that is running an operational program. This would result in a power transient followed by a crash to the loader.
Do not switch DME select while the scanner is operating.

A Processor and Memory are paired by being connected to the same BUS. If only one I/O is powered the IFSEL has to agree with that I/O:

IFSEL 1 goes with I/O X
IFSEL 2 goes with I/O Y

Do not enable both IFSELs at the same time - erroneous operation will result.

The operational program as part of its initialization selects:

All I/O X Functions - except S/C I/F
All Formatter G Functions
Primary L and T Filters
Primary HRD Post Amp
Primary Encoder FID and AUX Detectors (vanes)
Vacuum DME Startup Drive

The operational program as part of its redundant side initialization selects:

All I/O Y Functions - except S/C I/F
All Formatter H Functions
Redundant L and T Filters
Primary HRD Post Amp
Primary Encoder FID and AUX Detectors (mirrors)
Vacuum DME Startup Drive

3.3.1.4.3 Configuration Convention

The following discussion is a lead into the next section on Examples of various Turn On Sequences. To assist in defining an OLS Configuration the convention shown in Figure 3.3.1-2 was established.

The Power Enabled and the Signal Bus Connection configuration conventions are fully defined in the figure but more definition is given below for the Function Selection. Each function of the I/O and Formatter is represented by a designator of four characters or less as defined in the function listings in sections 3.3.1.2.2 & 3. The Analog functions which are described in sections 3.3.1.4 & 5 are assigned designators below:

L analog filter (L)
T Analog filter (T)
HRD postamplifier (HRD)
FID and AUX encoder (ENC)
Drive Motor Electronics (DME)

Primary (P) or Redundant (R) selection is made by SGN command except for the DME. DME A is assigned primary and DME B redundant and the select is by S/C command.

NOTE: For DME Startup there are 2 elements available but for on-orbit operation it should only be necessary to use the Vacuum Selection which is selected by the operational program, therefore this selection will not be addressed.

POWER ENABLED

Matrix Format:

PS	PROC	MEM	I/O		FORM		ANA
1	C	E	X		G		A
2	D	F		Y		H	

Line Format: PWR: 1(C,E,X,G,A) & 2(D,F,Y,H)

Power Supply (PS) may be 1 or 2 or both
i.e: 1(...),2(...),1(...) & 2(...)

Processor (PROC) may be only one (C or D) on either (1 or 2)
or both (C & D), one on each (1 & 2)
i.e.: 1(C),1(D),2(C),2(D),1(C) & 2(D),1(D) & 2(C)

Memory (MEM) may be only one (E or F) on either (1 or 2)
or both (E & F), one on each (1 & 2)
i.e.: 1(E),1(F),2(E),2(F),1(E) & 2(F),1(F) & 2(E)

Input/Output (I/O) may be one (X or Y) on either (1 or 2)
or both (X & Y) on either (1 or 2)
or both (X & Y), one on each (1 & 2)
i.e.: 1(X),1(Y),2(X),2(Y),1(X,Y),2(X,Y),1(X) & 2(Y),1(Y) & 2(X)

Formatter (FORM) may be one (G or H) on either (1 or 2)
or both (G & H) on either (1 or 2)
or both (G & H), one on each (1 & 2)
i.e.: 1(G),1(H),2(G),2(H),1(G,H),2(G,H),1(G) & 2(H),1(H) & 2(G)

Analog (ANA) may be on either (1 or 2)
i.e.: 1(A), 2(A)

SIGNAL BUS CONNECTION

Signal Bus BUS: A(C,E), & B(D,F)

Only powered MEM and PROC designators are indicated.
Operational Flight Program set is listed first.

FUNCTION SELECTION

Input/Output I/O: X(I/F, CLKS, SENS, GAIN) & Y(W/F, ODM)

Formatter FORM: G(SSP, RTD) & H(SDF, SDS)

Analog ANA: P(L, T, HRD) & R(ENC, DME)

Each function must appear once, and only once, and only in a block whose power is enabled.

Figure 3.3.1-2. Configuration Convention

3.3.1.4.4 Examples of Various Turn-On Sequences

Example 1 represents a single power turn on (see Figure 3.3.1-3). Note the undesired subsystems are commanded to the power supply that isn't enabled in order to minimize power consumption. In addition, OLS SGN commands are not necessary since the desired elements within the I/O, FORM, Video Selection and Encoder Detector are selected by operational program initialization. Hence, after the PROC LOAD CMPT command, the system is ready to receive the OLS Mode of Operation Commands that are referenced in Section 3.3.1.5 and discussed further in Section 3.3.2.

Example 2 also represents a single power turn on (see Figure 3.3.1-4). Beside the selection of some different subsystems, this example also demonstrates the need for some OLS SGN commands. Since FORM G, I/O Y, the redundant L and T filters and the redundant FID and AUX detector are desired, several SGN commands are required. Since the operational program redundant side startup will automatically select the elements within FORM H (which isn't powered) erroneous operation will result if the SGN commands for the elements in FORM G aren't sent. Hence, only after the FORM G SGN commands are executed is the system ready to respond properly to OLS Mode of Operation Commands.

Example 3 represents an OLS system with a single power supply on with both I/O's and both Formatters connected to it, (see Figure 3.3.1-5). Elements from each I/O are used to make up a complete I/O; the same is true for the Formatters.

Example 4 represents a Dual Power System Turn On (see Figure 3.3.1-6). For this example, even though the elements within each I/O and Formatter are to be mixed, it is not necessary to have them connected to the same power supply. The load is split between both power supplies to minimize thermal dissipation in each supply.

Desired Configuration

PS	PROC	MEM	I/O	FORM	ANA
1	C	E	X	G	A

Bus: A (C,E)
I/O: X (I/F, CLKS, SENS, GAIN, W/F, ODM)
FORM: G (SSP, RTD, SDF, SDS)
ANA: P (L, T, HRD, ENC, DME)

COMMANDING

Power Enable 1 - OFF — Pre Configuration Initialization
Power Enable 2 - OFF
Power Override - OFF
PFOT - LOW
BFOT - LOW
IFSEL 1 - HIGH
IFSEL 2 - HIGH
Load Proc C - HIGH
Load Proc D - HIGH

Processor Pwr SEL 1 — Power Configuration Turn On
Memory Pwr SEL 1
I/O X Pwr SEL 1
I/O Y Pwr SEL 2
Form G Pwr SEL 1
Form H Pwr SEL 2
Analog Pwr SEL 1
DME A SEL
IFSEL 1 - LOW
Load PROC C - LOW
Pwr Enable 1 - ON
Delay 1 second (minimum) from Pwr Enable 1 - ON
Processor BUS SEL 1
Memory BUS SEL 1

Load PROC C - LOW
Load PROC C - HIGH
OLS Operation Program Load CMMDS — Load and Verify
PROC C LOAD CMPT

Load PROC C - LOW
Load PROC C - HIGH — Verify
OLS CMMDS - Sync, Sync, ID
PROC C LOAD CMPT

Load PROC C - LOW — Start Program
Load PROC C - HIGH — @ LOC 010000
PROC C LOAD CMPT — Prime Side

No SGN CMMDS Required since the operational program selects prime functions

OLS Mode of Operations CMMDS

NOTE: Although the Load PROC C - LOW command in the Load and Verify section is not functionally required in this command sequence (it was sent prior to the power enable), experience has shown that for functional modularity it should be included in all program load command packages.

Figure 3.3.1-3. Single Power System Turn On - Example 1

Desired Configuration

PS	PROC	MEM	I/O	FORM	ANA
2	D	E	Y	G	A

Bus: B (D,E)
I/O: Y (I/F, CLKS, SENS, GAIN, W/F, ODM)
FORM: G (SSP, RTD, SDF, SDS)
ANA: P (HRD) & R (L, T, ENC, DME)

COMMANDING (Following 9 command Pre Configuration Initialization shown in Example 1)

Processor Pwr SEL 1 — Power Configuration Turn On
Memory Pwr SEL 2
I/O X Pwr SEL 1
I/O Y Pwr SEL 2
Form G Pwr SEL 2
Form H Pwr SEL 1
Analog Pwr SEL 2
DME B SEL
IFSEL 2 - LOW
Load PROC D - LOW
Pwr Enable 2 - ON
Delay 1 second (minimum) from Pwr Enable 2 - ON
Processor BUS SEL 1
Memory BUS SEL 2

Load PROC D - LOW
Load PROC D - HIGH
OLS Operation Program Load CMMDS — Load and Verify
PROC D LOAD CMPT

Load PROC D - LOW
Load PROC D - HIGH — Verify
OLS CMMDS - Sync, Sync, ID
PROC D LOAD CMPT

Load PROC D - LOW — Start Program
Load PROC D - HIGH — @ LOC 010006
OLS CMMDS - Sync, Sync, ID, Adr = 010006
PROC D LOAD CMPT — Redundant Side

SGN CMMDS for I/O Y and ANA functions not required
SGN - SSP Formatter G
SGN - RTD Formatter G
SGN - SDF Formatter G
SGN - SDS Formatter G

OLS Mode of Operation CMMDS

Figure 3.3.1-4. Single Power System Turn On - Example 2

Desired Configuration

PS	PROC	MEM	I/O		FORM		ANA
1	C	F	X	Y	G	H	A

Bus: B (C,F)
I/O: X (I/F, GAIN, W/F ODM) & Y (CLKS, SENS)
FORM: G (RTD, SDF, SDS) & H (SSP)
ANA: P (L, HRD, ENC) & R (T, DME)

COMMANDING (Following 9 command Pre Configuration Initialization shown in Example 1)

Processor Pwr SEL 1 — Power Configuration Turn On
Memory Pwr SEL 2
I/O X Pwr SEL 1
I/O Y Pwr SEL 1
Form G Pwr SEL 1
Form H Pwr SEL 1
Analog Pwr SEL 1
DME B SEL
IFSEL 1 - LOW
Load PROC C - LOW
Pwr Enable 1 - ON
Delay 1 second (minimum) from Pwr Enable 1 - ON
Processor BUS SEL 2
Memory BUS SEL 1

Load PROC C - Low
PROC C - HIGH
OLS Operation Program Load CMMDS — Load and Verify
PROC C LOAD CMPT

Load PROC C - LOW
Load PROC C - HIGH — Verify
OLS CMMDS - Sync, Sync, ID
PROC C LOAD CMPT

Load PROC C - LOW — Start Program
Load PROC C - HIGH — @ LOC 010000
PROC C LOAD CMPT — Prime Side

SGN CMMDS aren't necessary for the following since they are selected by the operational program:

Gain Control X, W/F X, ODM X
RTD G, SDF G, SDS G
Prime L Filt, Prime HRD Post Amp
Prime FID and AUX

SGN CMMDS are necessary for the following:
SGN - Clock Drive Y
SGN - Sensor Control Y
SGN - SSP Formatter H
SGN - Redund T Filt

OLS Mode of Operation CMMDS

Figure 3.3.1-5. Single Power, Dual I/O and Formatter System Turn On - Example 3

Desired Configuration

PS	PROC	MEM	I/O	FORM	ANA
1	C	E	Y	G	
2	D	F	X	H	A

Bus: A (D,F) & B (C,E)
I/O: X (CLKS, SENS, GAIN, W/F & Y I/F, ODM
FORM: G (SSP, SDF & H (RTD, SDS)
ANA: P (DME) & R (L, T, HRD, ENC)

COMMANDING (Following 9 command Pre Configuration Initialization shown in Example 1)

Processor Pwr SEL 1 — Power Configuration Turn On
Memory Pwr SEL 1
I/O X Pwr SEL 2
I/O Y Pwr SEL 1
Form G Pwr SEL 1
Form H Pwr SEL 2
Analog Pwr SEL 1
DME A SEL
IFSEL 2 - LOW
Load PROC C - LOW
Pwr Enable 1 - ON
Delay 1 second (minimum) from Pwr Enable 1 - ON
Load PROC D - LOW
Power Enable 2 - ON
Delay 1 second (minimum) from Power Enable 2 - ON
Processor BUS SEL 2
Memory BUS SEL 2

Load PROC C - LOW
Load PROC C - HIGH
OLS Go to ADR 0 CMMDS
PROC C LOAD CMPT — (PROC C Powered & Idle) Both PROC Powered - C is Idle, D is in Loader

---

Load PROC D - LOW
Load PROC D - HIGH — Load and Verify
OLS Operational Program Load CMMDS — (CMMDS go to PROC D since
PROC D LOAD CMPT — it is in Loader

Load Proc D - LOW
Load PROC D - HIGH
OLS CMMDS - Sync, Sync, ID — Verify
PROC D LOAD CMPT

Load PROC D - LOW — Start Program @ LOC 010000
Load PROC D - HIGH
PROC C LOAD CMPT

SGN CMMDS aren't necessary for the following since they are selected by the operational program:

Clock Drive X, Sensor Control X, SSP G
Gain Control X, Wow/Flutter X, SDF G

SGN CMMDS are necessary for the following:

SGN - RTD H — SGN - Output Data MUX Y
SGN - SDS H — SGN - Redund T Filt
SGN - Redund L Filt — SGN - HRD Backup Post Amp
SGN - Redund FID and AUX Encoder

OLS Mode of Operation CMMDS

Figure 3.3.1-6 Dual Power System Turn On - Example 4

3.3.1.4.5 Switching Power Configuration Once Operational

Any power switching once an operational program is executing could cause erroneous operation unless the following sequence is followed. Such erroneous operation is not catastrophic to the OLS or spacecraft but could cause delay in re-establishing OLS modes of operation and loss of valuable data. Prior to re-execution of the operational program, a verification sequence should be done on the program load. Errors in the executable code portion of memory would require reloading the program which should only be done when sufficient time for a reload is available.

For illustrative purposes the power switching in the sequence below is the enabling of the second power supply. However any reconfiguration of power requires the same command sequence. The command sequence is as follows:

```
Idle the Processor with the operational program. This resets all modes.
     Load PROC J - Low
     Load PROC J - High
     OLS CMMDS Sync, Sync, ID, ADR = 0
     PROC J LOAD CMPT
Load PROC C - Low
Load PROC D - Low
Power Enable (Power Supply that is OFF) - ON
Delay 1 second (minimum)
Recommand the Memory Bus Selection used originally
Recommand the Processor Bus Selection used originally
Idle both processors
     Load PROC C - Low
     Load PROC C - High
     OLS CMMDS - Sync, Sync, ID, ADR = 0
     PROC C Load CMPT
     Load PROC D - Low
     Load PROC D - High
     OLS CMMDS - Sync, Sync, ID, ADR = 0
     Proc D Load CMPT
```

Now the second side is powered and it's Processor and Memory are in the idle state. The action of bringing up the second side may have been done for many different reasons but let's assume it was done for either running Memory Diagnostics on the previously off side or a quick way to get the second I/O and Formater electronics powered and made available.

For the case of Memory Diagnostics, the following action could take place:

Execute the Operational Program using the same sequence in paragraph 3.5.1.4.1 addressing the correct processor. For precaution, a verification sequence should be done first per paragraph 3.3.1.4.1.

Send the appropriate SGN commands if necessary, to configure the OLS the same as it was originally.

Execute the appropriate OLS Mode of Operation Commands.

Load a Diagnostic Program data file using the command sequence in paragraph 3.3.1.4.1.

Execute the Diagnostic Program according to its commanding rules.

For the case of using the hardware of the newly powered I/O and/or Formatter:

The newly powered Processor and Memory can be left in Idle.

Execute the Operational Program using the command sequence in paragraph 3.3.1.4.1. For precaution, a verification sequence should be done first per paragraph 3.3.1.4.1.

Send the appropriate SGN commands for the elements desired.

Execute the appropriate OLS Mode of Operation Commands.

3.3.1.5 Configuration Commands for First Orbit Telemetry

First Orbit Telemetry operation will be discussed in more detail in section 3.3.2. Briefly, the OLS can record and playback spacecraft 2K-bit telemetry without an operational program loaded in its memory or, if it is loaded, without executing it. This is accomplished by using either of two level discretes (PFOT or BFOT) from the S/C CIU. The OLS has a redundant implementation of this function. Since the OLS is launched with power off, the S/C Stored Command Table is required to provide the necessary power configuration and turn on commands in order to accomplish this function after handover. Figure 3.3.1-7 provides the command sequence necessary for the primary and redundant turn-on configurations of First Orbit Telemetry and section 3.3.2 will discuss detailed commanding. The asterisks between the two columns identify the commands that are unique for each approach.

PRIMARY MODE		REDUNDANT MODE
Power Override - OFF		Power Override - OFF
Power Enable 1 - OFF		Power Enable 1 - OFF
Power Enable 2 - OFF		Power Enable 2 - OFF
PFOT - LOW		PFOT - LOW
BFOT - LOW		BFOT - LOW
IFSEL 1 - HIGH		IFSEL 1 - HIGH
IFSEL 2 - HIGH		IFSEL 2 - HIGH
Load Proc C - HIGH		Load Proc C - HIGH
Load Proc D - HIGH		Load Proc D - HIGH
Processor Pwr SEL 1		Processor Pwr SEL 1
Memory PWR Sel 1		Memory PWR SEL 1
I/O X Pwr SEL 1		I/O X Pwr SEL 1
I/O Y Pwr SEL 2		I/O Y Pwr SEL 2
Form G Pwr SEL 1		Form G Pwr SEL 1
Form H Pwr SEL 2		Form H Pwr SEL 2
Analog Pwr SEL 1	*	Analog Pwr SEL 2
DME SEL A	*	DME SEL B
IFSEL 1 - LOW	*	IFSEL 2 - LOW
Load Proc C - LOW	*	Load Proc D - LOW
Power Enable 1 - ON	*	Power Enable 2 - ON
Delay 1 second (minimum)		Delay 1 second (minimum)
Processor BUS SEL 1		Processor BUS SEL 1
Memory BUS SEL 1		Memory BUS SEL 1
Load Proc C - HIGH	*	Load Proc D - HIGH
PFOT - HIGH	*	BFOT - HIGH

OLS CONFIG:	PWR... 1 (C,E,X,G,A)	OLS CONFIG:	PWR: 2 (D,F,Y,H,A)
	BUS: A (C,E)		BUS: B (D,F)
	I/O: X (all)		I/O: Y (all)
	FORM: G (all)		FORM: H (all)
	ANA: P (DME)		ANA: R (DME)
	PR1 - SDS Record		PR3 - SDS Record

Figure 3.3.1-7. First Orbit Telemetry - Configuration
CMMDS Post Handover

3.3.1.6 Configuration ESTs

The OLS ESTs can be classified into five categories - power, environment, performance, configuration and fault isolation. This section will (specify what is available in the way of configuration ESTs while section 3.4.1 addresses the entire subject of ESTs. The following details what information may be derived from ESTs.

ESTs are provided to determine which blocks of the system are powered (PS1, PS2, Analog, PROC C, MEM E, MEM F, I/O X, I/O Y, FORM G, FORM H).

PROC D isn't present - but could deduce by knowing PS1, PS2, PROC C status).

System Block to PS connection is not stated but could be deduced for a single PS system once that power supply is enabled.

PS ESTs also provide the status of the Override Mode.

ESTs are provided to determine the Processor and Memory connections.

ESTs are provided to determine the Interface Selection.

ESTs are provided to determine which functions within the I/O are selected.

ESTs are provided to determine which functions within the Formatters are selected.

ESTs are provided to determine which Filter Outputs and HRD Postamp are selected.

ESTs are provided to determine Processor Mode and Commanding Input Status.

An EST for DME Selection is not available although once scanner motion is occurring DME selection can be deduced from performance ESTS and Scan Enable ESTs.

An EST is provided for Encoder Detector Selection.

An EST is provided for DME Start-Up Pulse Selection.

ESTs are provided to determine the status of the Primary Data Formatters.

ESTs are provided to determine the Configuration of the Output Data Multiplexer.

ESTs are provided to determine T Level, T Gain, L Chan and LIN/LOG Status, although left and right T Gains are not separately identified and will be sampled asynchronously by the PIP.

An EST is provided to determine the status of the PMT High Voltage (also provides performance information).

An EST is provided to determine the status of the T Channel Heater.

ESTs are provided to determine the Source of Encoder Pulses provided to the Processor.

ESTs are provided to determine the status of Heater Controllers & Hot Wire Devices.

3.3.2 OLS Commanding

This section describes loading and commanding the OLS. Additional information, including the command formats, is presented in the Operators Manual (Appendix 1). It is assumed throughout this section that the required spacecraft (S/C) commands have been executed to place the OLS in a mode for loading or commanding. Numbers in this section with a leading zero are octal; e.g., 0100 = 64.

3.3.2.1 First Orbit Telemetry

Telemetry in the SDS line format can be recorded during the first orbit, after handover, and before the OLS program is loaded. Either processor C or D can perform this function. The first orbit telemetry (FOT) software is available in ROM in both memories E and F. The processor must first receive an S/C LOAD PROCESSOR command. This command is then followed by a S/C PFOT or S/C BFOT command.

The primary FOT command, PFOT, will perform FOT using PR1, I/O X, formatter G, channel 1 clear, and DT1.

The back-up FOT command, BFOT, will perform FOT using PR3, I/O Y, formatter H, channel 2 clear, and DT2.

Receipt of PFOT (BFOT) starts the record sequence. Also, the record sequence is started if either PFOT or BFOT was on when the S/C LOAD PROCESSOR command was received. PFOT will take priority over BFOT when starting an FOT record mode.

FOT will continue to operate in the record mode until PFOT (BFOT) is commanded off. FOT will then switch to playback mode. FOT will be turned off if an EOT is encountered in record or a BOT is encountered in playback; however, mode switching can still occur with the use of PFOT (BFOT) commands; i.e, if an EOT was encountered during record, FOT is turned off but is still awaiting a PFOT (BFOT) off command. When this command is received, FOT is placed in the playback mode. When in playback mode, a new record sequence may be started at any time by commanding on either PFOT or BFOT.

Program delays are provided for equipment protection. When switching to the record mode, a 5-second delay is provided prior to turning on the PR. When switching to playback mode, the DT is turned on for 10 seconds before turning on the PR.

FOT will be terminated either by receipt of a sync word (0137465) on COMDAT or by a S/C LOAD PROCESSOR COMPLETE command. When FOT is turned off, the following takes place:

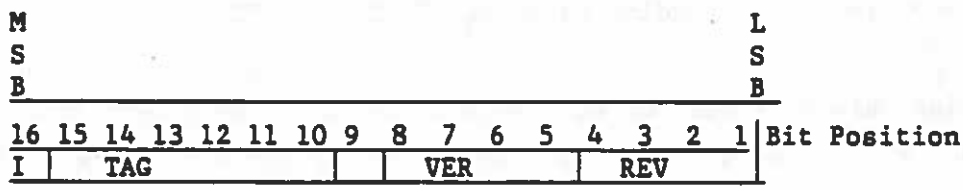
PR1-PR3 POWER	DISABLE
DT1-DT4 POWER	DISABLE
SSA-SSL POWER	DISABLE
BB1-BB4 POWER	DISABLE
SDS	DISABLE
SDFL, SDFT	DISABLE
SDSPR1-SDSPR4	DISCONNECT
SDFPR1-SDFPR4	DISCONNECT
IMC	ENABLE
TFLS	DISABLE
RTD	DISABLE
ENCSIM	DISABLE
T CHANNEL HEATERS	DISABLE
PMT POWER	DISABLE
SCAN A	DISABLE
SCAN B	DISABLE

in addition, the OSU is set (channel n to DTn), vehicle ID is set to 0 and orbit direction is set to 0 (+ Y Direction).

In order to provide timing pulses, FOT will use the encoder simulator set to the free run mode.

3.3.2.2 Program Load File Format

The program load file consists of a header sequence of three 16-bit words, an address word, and finally the data to be loaded. The data load starts at the address specified. The address is the absolute memory location. The first location in RAM is address 06000. The 3-word header consists of sync, sync, ID where sync = 0137465, and ID is the identifier whose format is:



Bits 10-16 can be any value, but they will be changed by the loaded program for the echo. Bits 5-8 contain the program version and bits 1-4 contain the revision of that version. The loader will echo bits 1-9 as transmitted. Bit 16 echo indicates processor ID (0=C, 1=D). Bits 10-15 echo indicates program load data tag of 077.

3.3.2.2.1 Card Image Format

The load file is supplied via a card deck of 1666 standard 80 column Hollerith cards. Each card image contains a decimal sequence number, right justified in columns 77-80. The first card contains a 1 in column 80, the last card contains a 1666 in columns 77-80.

Card number 1 is a header card and is not part of the load file. This card consists of 25 alphanumerics starting in column 1 containing the program name, version, revision, and date. Six octal characters starting in column 31 give the address of the first data word. Six octal characters starting in column 41 give the address of the last data word. Sequence number 1 in column 80.

Cards 2-1666 contain the load file to be uplinked to the OLS via the COMDAT interface.

Card 2 is the program load file header consisting of two sync words, the ID word, and the starting address. These are the first OLS words transmitted in a program load. The sync word (137465) is six octal characters in columns 1-6 and 8-13. The ID word (077VER) is six octal characters in columns 15-20. VER is program version (bits 5-8) and revision (bits 1-4). The address word is the starting address of the data to follow and is six octal characters in columns 22-27. Sequence number 2 is in column 80.

Cards 3-1666 contain program load data, with eight words per card except the last card, which may contain from one to eight words depending on the load length. There are six octal characters per word, starting in column 1 with one space between words. The sequence number is in columns 77-80, right justified.

3.3.2.2.2 System Test Equipment Format

The program load file is also available in the following binary format which is used by the System Test Equipment (STE) and also provided to the 1000 Satellite Operations Group. The STE has also provided this format on a Data General Eclipse computer produced 9-track, 800 BPI magnetic tape for interface with RCA. The format (Figure 3.3.2-1) consists of five functional blocks.

Name Block: 30 ASCII character name field packed two characters per 16 bit words. This block contains the program version, revision, and creation date.

Address Block: 2 words in binary. First word is the program start address, second word is the program end address.

Check sum Block: Variable length block in binary. First word contains number N, of checksums in this block. 2XN words follow in this block where the first word of each pair is a processor memory block number (0-077) and the second word in the pair is the computed checksum (at program assembly time) of that block.

Sync Block: First word in sync block contains the number of words in the sync block and is normally four. The remaining words of the sync block are the first four words to be uplinked in a program load and consist of sync, sync, ID, and address.

Data Block: First word in data block is the number of data words which follow (program data to be uplinked). The remaining words in the data block contain the actual program to be unlinked.

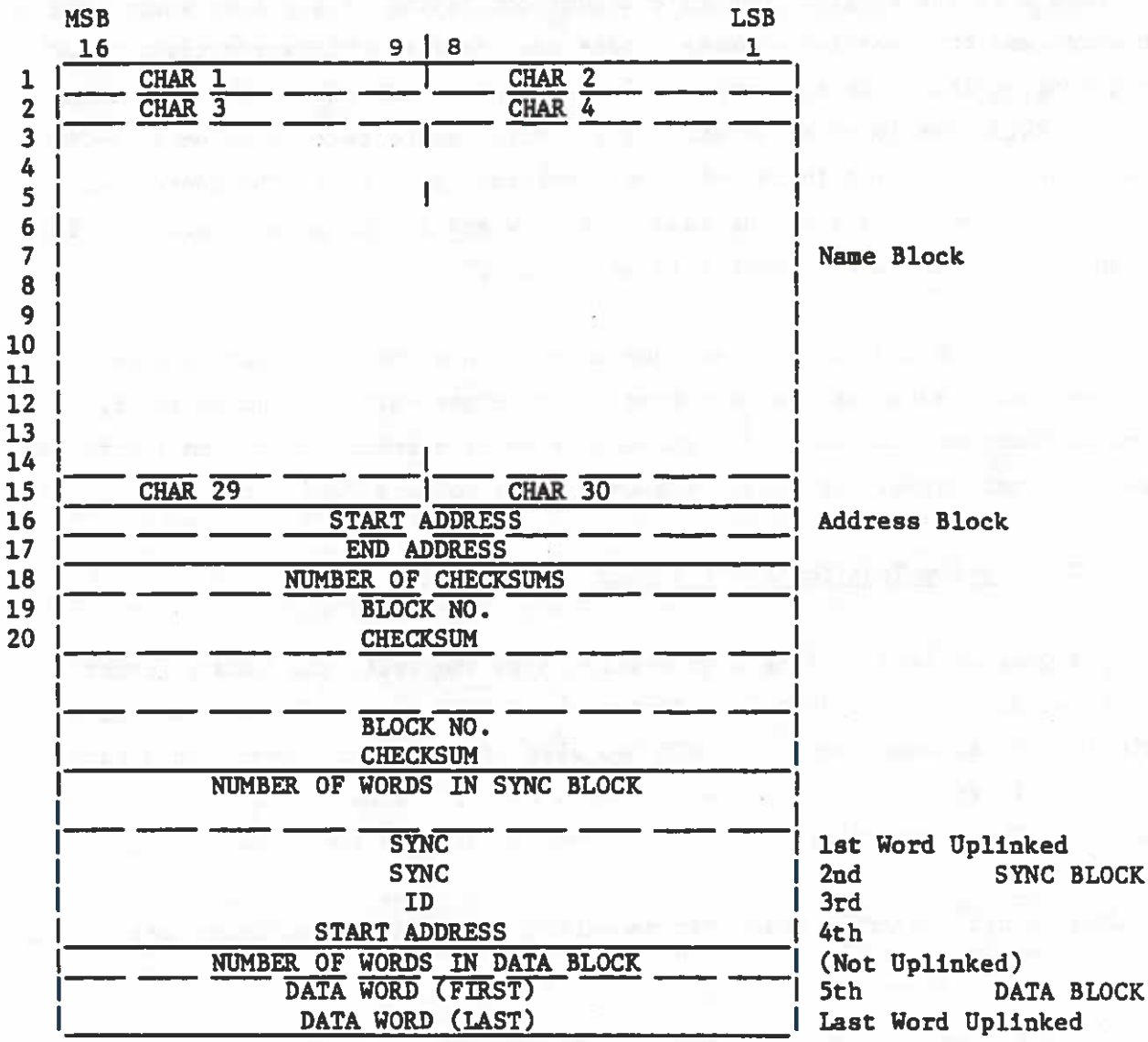


Figure 3.3.2-1. STE Program Load File Format

3.3.2.3 Loader Command Sequences

The loader program in ROM will respond to several command sequences (in addition to the FOT command sequences) to facilitate loading, verification, and start-up. These sequences are defined by the mnemonics:

LDM	Load and verify
VER	Verify
INO	Initialize program at location 010000
GTO ADR	Go to address ADR
GTO L1DUMP	Dump memory
GTO I3BPS	Bypass initialization
GTO E6CALC	Change precomputed checksums
GTO I3IRED	Initialize program at location 010006 (Redundant Side)

The following definitions are helpful in described the sequences:

LP (C or D)	S/C load processor C or D LOW followed by HIGH sequence
LPC (C or D)	S/C load processor C or D complete
HDR	OLS header (SYNC, SYNC, ID)
SYNC	OLS SYNC (0137465)
ID	OLS ID (ITGVER)
ADR	OLS address word
DATn	OLS data word n

All OLS words are echoed on MDDATA as received except for the OLS ID word whose echo contains processor ID in 1(0=C,1=D) and program load tag (077) in tag bits TG. Program version and revision are echoed as uplinked.

Since the uplink rate is 80 words per second, the PIP must be in the 10 Kbit OLS dump mode to receive all echoes. Since this may not be the desired PIP mode, the verify sequence following the load will provide a check nearly as good as a file compare in about 16 seconds in the slowest PIP mode (2KBPS OLSDUMP). In addition, the verify depends on the data stored in memory, whereas the echo is on data prior to going to memory.

3.3.2.3.1 Load and Verify

The load and verify is commanded by sending an LDM where for an n word load

LDM = LP, HDR, ADR, DAT1, DAT2, ..., DATn, LPC

The data will be loaded and echoed on MDDATA as received. Following the LPC a verify will be performed in which block checksums are computed and down-linked MDDATA at the rate allowed by the PIP. Block checksums start at block 0 and end with block 077, skipping block 033.

These checksums have been precomputed for a normal load and are stored in the load data address 0-077 of block 033 (absolute address 015400 015477). Block 0 checksum is in address 015400 and block 077 checksum is in address 015477. The ground can use the downlinked checksums compared with the precomputed checksums to establish load integrity. Only those blocks found bad need to be retransmitted; in which case

LDM = LP, HDR, ADR, DAT1,..., DAT256, LPC

is the sequence for a one-block load with ADR = address of that block and DAT1-DAT256 = the contents of that block.

For nonstandard loads, it may be required to compute the checksum on the ground if it is not already in the load file. The method that should be used to perform this 16-bit checksum is

```
      BLK = BLOCK TO CHECKSUM
      CKSM = 0
      X = 0377
AA    CKSM = SHIFT RIGHT CYCLIC 1 BIT[CKSM+MEM(BLK*256+X)]
      DONE IF X =  0
      DECREMENT X
      GO TO AA
```

3.3.2.3.2 Verify

The verify sequence is commanded by sending a VER where

VER = LP, HDR, LPC.

This will cause a new computation and downlinking on MDDATA of the 63 checksums starting at block 0 and ending with block 077, skipping block 033.

3.3.2.3.3 Initialize Program to Primary Side

The program in RAM is normally initialized (started) with an INO where,

INO = LP, LPC

This causes program control to go to address 010000 in RAM for its next instruction. The operational flight program will automatically SYSGEN to the primary functional blocks when started at this address.

3.3.2.3.4 Go to ADR

The GTO sequence will transfer control to the specified address.

GTO ADR = LP, HDR, ADR, LPC

The INO can also be done with a GTO 010000. The GTO is useful for providing access to special purpose routines or for performing the program initialization if RAM address 010000 is bad as an INO would not work.

3.3.2.3.5 Dump Memory

All memory starting at location 0377 of block 077 and ending with address 000 of block 0 is dumped via MDDATA using GTO L1DUMP where L1DUMP is the address in ROM block 0 of the L1DUMP routine. [L1DUMP = 0304 for OLSROM(0).]

GTO L1DUMP = LP, HDR, L1DUMP, LPC

The time required for dumping all of memory is a function of PIP mode.

10 Kbit OLS Dump	74 seconds
10 Kbit $\overline{\text{OLS}}$ Dump	6.8 minutes
2 Kbit OLS Dump	6.8 minutes
2 Kbit $\overline{\text{OLS}}$ Dump	1.1 hours

3.3.2.3.6 Bypass Initialization

When the operational program is started, the first routine executed is an initialization of the processor I/O and scratch memory. GTO I3BPS will bypass the initialization and proceed to the Exec. Note that none of the initialization functions are performed. These functions also include incrementing the initialization count in the processor status word and putting a fixed pattern in the stored telemetry buffer.

GTO I3BPS = LP, HDR, I3BPS, LPC

where I3BPS is the address of the initialization bypass located in RAM block 020 and depends on the version or revision of the OLS program loaded.

3.3.2.3.7 Change Precomputed Checksums

A table of precomputed checksums is stored in address 0-077 of block 033 and is part of a normal program load. During the running of the operational program, a memory diagnostic is periodically called to compute checksums of blocks 0-067 except for scratch blocks. These checksums are compared against the precomputed values stored in the table and errors are flagged. If the program is patched either by a MAC command or a program load, the checksum for the patched block will not match the table checksum and a processor status EST error indication will result. A GTO E6CALC will recompute all checksums and update the table. E6CALC is located in block 01 [E6CALC = 0400 for OLSROM (0)].

GTO E6CALC = LP, HDR, E6CALC, LPC

3.3.2.3.8 Initialize to Redundant Side

One method of initializing the operational flight program is with an INO or GTO 010000. This method will automatically SYSGEN to the primary functional blocks including I/O X and Formatter G. If the program is started with a

GTO I3IRED

the program will automatically SYSGEN to the redundant functional blocks including I/O Y and Formatter H. The address of I3IRED is 010006 which should be verified from the program listing.

In either of the cases above the DME pulsewidth will be set to VACUUM and the Primary HRD POST Amp will be selected.

3.3.2.3.9 Run-Load EST

Each processor has an EST which indicates whether it is in RUN or LOAD. If the processor is in the Loader, the EST is set to LOAD. If the processor exits the loader (INO, or GTO), the EST is set to RUN.

A S/C load processor command or illegal OP code execution will put the processor in the loader. An illegal OP code is a 00 or 017 OP code in bits 13-16 of a memory word. Thus, if the software malfunctions and runs into data, it will most likely encounter this bit configuration and crash to the loader.

An indirect way for the processor to get to the loader is through the core access rate limit hardware. If the core access rate exceeds 25,000 accesses in a 1/4-second band, the memory controller will send back an illegal OP code, forcing the processor to the loader.

3.3.2.3.10 OLS Reset

If the OLS returns to the loader for any reason and the other processor is not in run, an OLS reset will be performed to protect units such as tape recorders and transmitters. All recorders, transmitters, and encrypters will be disabled. In addition, the mission sensors, scanner, and T channel heaters will be disabled. The commanded status image of these units in the scratch memory will not be changed. It would be possible then to obtain the system status at the point where the reset occurred by bypassing initialization and dumping the scratch blocks or by commanding a complete 16K dump using the GTO L1DUMP sequence.

3.3.2.4 Real Time Commanding and Command Verification

After the operational flight program is initialized, real time commands may be sent and executed. When a command is received it is simply stored in memory. Receipt of the ACCEPT pulse will cause the previous command sent to be retrieved from memory and executed. A NO-OP command is then placed in the memory store. The NO-OP protects against multiple executes of the same command if back-to-back ACCEPT pulses are received.

Commands are checked for parity and must have odd parity for execution. If the parity is even, the command is placed in the system error table and the processor status word error EST is turned on.

A special command can be sent which will set a parity override flag. This command will be executed independent of parity. This essentially inhibits parity checking and allows all commands to be executed until the override is turned off.

If the command was accompanied by a REJECT pulse, it will not be executed.

Each command received is placed in a 20-word real time command verification buffer after receipt of the ACCEPT or REJECT pulse. The OLS signals the spacecraft when a word is ready for verification over CVDATA. The spacecraft will accept CVDATA within one PIP frame time. Bit 16 will indicate processor identification with a logic 1 referring to processor D and a logic 0 referring to processor C. Bits 1-15 are echoed as as received if the command was executed. If the command was not executed either because of even parity and no override or a REJECT pulse occurred, bits 1-15 will be logically inverted prior to downlinking via CVDATA.

3.3.2.5 OLS Commands

This section describes the OLS commands and provides information as to their use. The Operators Manual, Appendix A, contains a complete description of the command formats. The following is a list of the basic commands.

Command Code	Mnemonic	Description
00	GNC	Gain Control
01	RTR	Real Time Readout
02		Spare
03	SDC	Stored Data Control
04	RLC	Record Location Counter
05		Spare
06	TBC	Transmitter/BBT Control
07	PSC	Primary Sensor Control
010		Spare
011	SSC	Mission Sensor Control
012	SGN	System Generator
013	OCP	Orbit Clock Preset
014	UPC	Uplink Program Control
015	MAC	Memory Access Command
016	AIS	Auxiliary Instruction Set
017	SPC	Special Purpose Command

3.3.2.5.1 Preliminary Commands - SGN, PSC

When the program is initialized to the primary side, the scanner is turned off, the I/O X and formatter G are selected, and the vacuum DME pulse width, primary encoder, video filters, and HRD post amplifier are selected. If any redundant functional blocks are required, SGN commands should be used. The appropriate S/C commands should have been sent previously to power the functional blocks.

When the program is initialized to the redundant side, the scanner is turned off, the I/O Y and formatter H are selected and the redundant encoder and video filters are selected. The primary HRD post amplifier and vacuum DME pulse width are also selected. If any additional primary functional blocks are required, SGN commands should be used. The appropriate S/C commands should have been sent previously to power the functional blocks.

The PSC command will turn on the scanner, PMT, and IMC. Initialization will enable the IMC and turn off the scanner and PMT. If DME A has been selected via S/C command, scanner A enable should be sent. If a S/C command has selected DME B, scanner enable B should be sent.

3.3.2.5.2 Gain Selection - GNC

The GNC command is available for all gain mode and gain value selection. This command can be used to control the gain of the L channel and the T channel. The L channel gain is controlled through the selection of the sensor and the gain of the variable digital gain amplifier (VDGA). Also controlled by the command is the lin/log amplifier operation in the L channel.

Gain selection commands do not become effective until during the next end-of-scan region (+EOS for L channel, -EOS for T channel). This is done so that the mode during an entire active scan line is consistent. Since gain commands are processed only during end-of-scan regions, care should be taken to ensure two different gain commands are not sent closer than 168 milli-seconds apart. If the commands are too close together, the second will overwrite the first in the OLS software. Data such as azimuth, elevation, and spacecraft altitude ratio (h/R) obtained from the spacecraft and used in gain control are updated by software only during the positive end-of-scan.

3.3.2.5.2.1 Along Scan Gain Control

The along scan gain control (ASGC) mode software is the most automatic of the gain modes. During active scan, the software will control the gain value presented to the VDGA and perform the sensor selection. The computations performed for this control depend upon the spacecraft elevation, azimuth, and altitude, as supplied by the spacecraft, and the OLS scan angle. This computation produces the scene source elevation angle used to obtain a gain value from the gain value versus scene source elevation (GVVSSE) table which is then modified by the BRDF algorithm. Thus in the ASGC mode, the software will cause the VDGA gain to follow the GVVSSE curve as defined by the GVVSSE table values and modified by the BRDF.

3.3.2.5.2.1.1 Programming GVVSSE Curve

To determine the gain value to place in the VDGA, the software must have these values in a table form in memory. This table represents the GVVSSE. The values are stored in page 0 of the stored program memory. The following diagram shows the format of the table:

ANGLE	BIT POSITION															
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	P									.						
+80L										.						
+80L										.						
+79L										.						
+78L										.						
-										.						
-5L -15S										.						
-										.						
+78S										.						
+79										.						
+80S																
+80S	P	2^8								2^0	2^{-1}					2^{-6}

The first table value is the gain at a lunar elevation angle of +80 degrees. The last location in the table is the gain at a solar elevation angle of +80 degrees. The +80 degree gain value is within 1/8 dB of the +90 degree gain value and is therefore appropriate for use in the whole +80 to +90 degree range.

When in automatic modes (ASGC or ATGC, Along Track Gain Control, described later), the software uses this table to obtain gain values for the VDGA. For greater accuracy, the software performs a linear interpolation between two values when doing a table look-up. Note that gain values for +80 degrees are duplicated. This duplication is necessary to avoid special case interpolation at the ends of the table.

The gain values are the only data stored in memory for the GVVSSE curve. Since angles corresponding to the gain values are not stored, all gain values at one-degree increments must be loaded. It is possible to uplink an entire table or just a single value, if a single-value change is desired. Any uplinked value into the GVVSSE table becomes effective immediately; the

software does not wait until an active scan line is completed before using these new values.

The parity bit is shown in the GVVSSE table diagram, which shows that the bit is present when uplinked. When the table is actually stored in memory, the parity bit (position 16) is forced to zero (0). The format of the remaining bits (as shown in the diagram) has the radix point between bit positions 7 and 6. The least significant bit of each gain value is 2-6 dB. The range of gain values (with 16 always zero) is 0 to 512 dB. Figure 3.3.2-2 shows a typical GVVSSE curve and Table 3.3.2-1 shows the values that produced the curve.

3.3.2.5.2.1.2 Bias Modification

The bias modifier allows the indirect altering of the values obtained from the GVVSSE table values without changing the values of the GVVSSE table stored in memory. The bias value is initially set to zero by the OLS software. The equation using the bias value in the software is:

SSEA = TSSEA+B

where:

B = bias
TSSEA = true scene source elevation angle
SSEA = scene source elevation angle of GVVSSE curve

3.3.2.5.2.1.2.1 Bias Modifier

To change the bias value, one of the subcommands of GNC must be sent to the OLS. For negative bias values, the number must be in two's complement form. This value represents an angle by which the GVVSSE is shifted without changing its shape.

3.3.2.5.2.1.3 Selecting Sensor Switching Points

Eight values are stored in constants memory to control the selection of sensor when in an automatic (ASGC or ATGC) mode. These values define the points on the GVVSSE curve at which a switch is to be made from one sensor to the next and to define the variable digital gain amplifier offset in each sensor region. The parameters are as follows:

Code	Typical Value, dB	Parameter
P(0)	6	HRD Offset
S(1)	59	Switch point HRD-PMT 1/9
P(1)	47	Gain change HRD-PMT 1/9
S(2)	22	Switch point PMT 1/9-PMT LO
P(2)	0	Gain change PMT 1/9-PMT LO
S(3)	34	Switch point PMT LO-PMT HI
P(3)	30	Gain change PMT LO-PMT HI
Delta	4	Switch point Delta

If P(2) is zero, the PMT 1/9 mode will be bypassed but any other value of P(2) will enable selection of PMT 1/9. S(2) must be set to a value between S(1)-P(1)+ Delta and S(3)- Delta when P(2)=0, to obtain proper operation.

The above chart shows typical values for the parameters; the exact value may be different and must be determined from hardware characteristics.

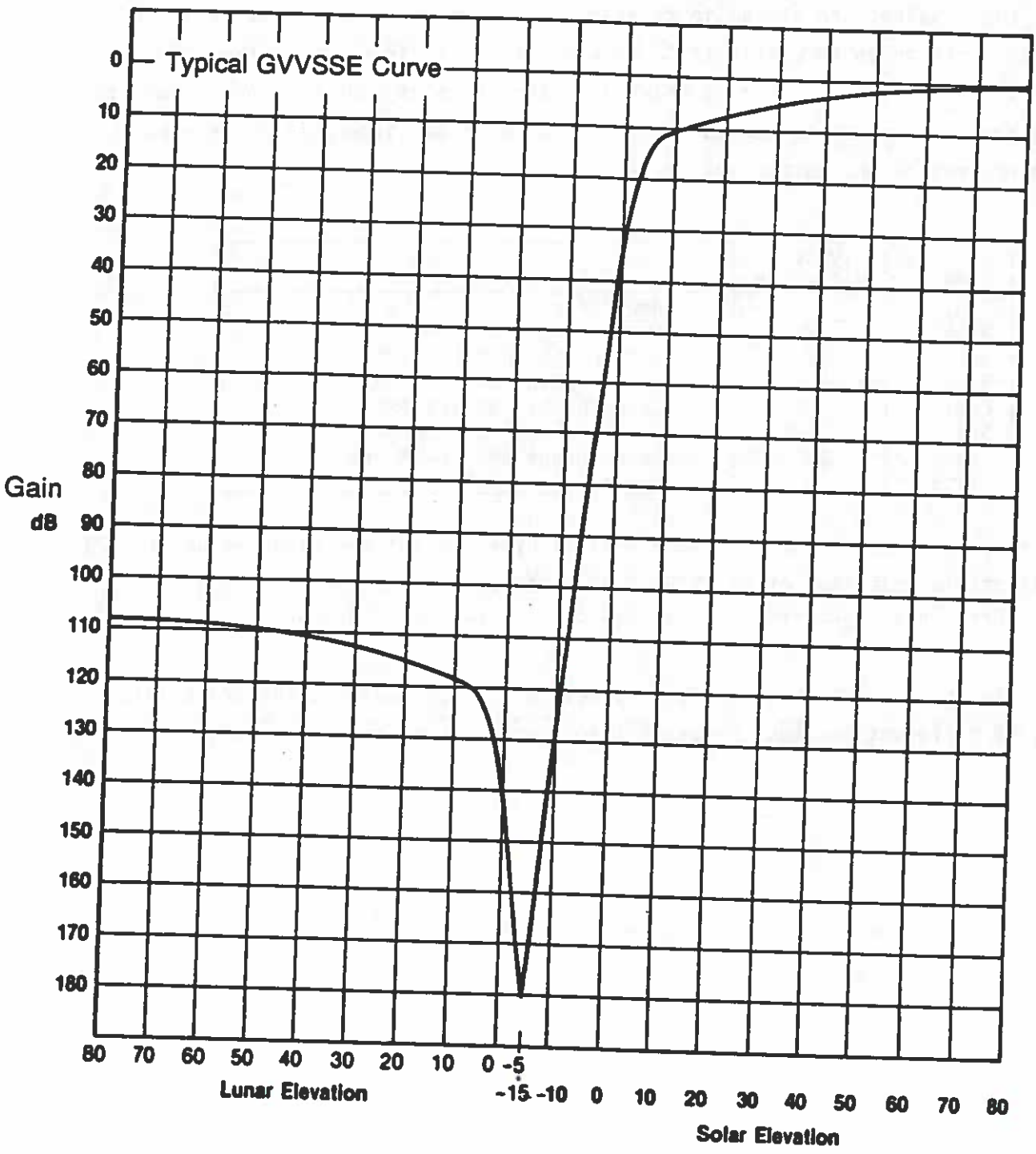


Figure 3.3.2-2. Gain Value Versus Scene Source Elevation

Table 3.3.2-1. Typical GVVSSE Values

ANGLE	OCTAL ADDRESS	OCTAL VALUE	GAIN, dB
80L	111	115406	108.09
80	112	115406	108.09
79	113	015407	108.11
78	114	115411	108.14
77	115	115414	108.19
76	116	015416	108.22
75	117	015420	108.25
74	120	115422	108.28
73	121	115424	108.31
72	122	115427	108.36
71	123	115430	108.38
70	124	115433	108.42
69	125	115436	108.47
68	126	115441	108.52
67	127	115444	108.56
66	130	115450	108.63
65	131	115453	108.67
64	132	115456	108.72
63	133	015462	108.78
62	134	115466	108.84
61	135	115472	108.91
60	136	015476	108.97
59	137	115502	109.03
58	140	115507	109.11
57	141	015514	109.19
56	142	015521	109.27
55	143	015527	109.36
54	144	015535	109.45
53	145	115543	109.55
52	146	015550	109.63
51	147	115557	109.73
50	150	015565	109.83
49	151	015574	109.94
48	152	015603	110.05
47	153	015611	110.14
46	154	115620	110.25
45	155	015627	110.36
44	156	115637	110.48
43	157	015647	110.61
42	160	115657	110.73
41	161	115667	110.86
40	162	115700	111.00
39	163	015710	111.13
38	164	115721	111.27
37	165	115733	111.42
36L	166	015745	111.58

Table 3.3.2-1. Typical GVVSSE Values (Continued)

ANGLE	OCTAL ADDRESS	OCTAL VALUE	GAIN, dB
35L	167	115756	111.72
34	170	015770	111.88
33	171	016003	112.05
32	172	116016	112.22
31	173	016030	112.38
30	174	016044	112.56
29	175	016060	112.75
28	176	116075	112.95
27	177	016113	113.16
26	200	016131	113.39
25	201	116150	113.63
24	202	116171	113.89
23	203	116212	114.16
22	204	116233	114.42
21	205	016254	114.69
20	206	016276	114.97
19	207	016317	115.23
18	210	016341	115.52
17	211	016365	115.83
16	212	116412	116.16
15	213	016443	116.55
14	214	116474	116.94
13	215	116526	117.34
12	216	116557	117.73
11	217	116610	118.13
10	220	016641	118.52
9	221	016671	118.89
8	222	016723	119.30
7	223	016767	119.86
6	224	017054	120.69
5	225	017200	122.00
4	226	117374	123.94
3	227	117656	126.72
2	230	020237	130.48
1	231	020726	135.34
0	232	021525	141.33
-1	233	122431	148.39
-2	234	023434	156.44
-3	235	124523	165.30
-4L	236	125662	174.78
-5L-15S	237	026410	180.13
-14	240	124707	167.11
-13	241	123504	157.06
-12	242	022301	147.02
-11S	243	021076	136.97

Table 3.3.2-1. Typical GVVSSE Values (Continued)

ANGLE	OCTAL ADDRESS	OCTAL VALUE	GAIN, dB
-10S	244	117672	126.91
-9	245	016467	116.86
-8	246	015264	106.81
-7	247	014061	96.77
-6	250	112656	86.72
-5	251	111452	76.66
-4	252	010262	66.78
-3	253	007123	57.30
-2	254	006034	48.44
-1	255	005031	40.39
0	256	004125	33.33
1	257	003326	27.34
2	260	102637	22.48
3	261	102256	18.72
4	262	101774	15.94
5	263	001600	14.00
6	264	001454	12.69
7	265	101367	11.86
8	266	101323	11.30
9	267	101271	10.89
10	270	101241	10.52
11	271	001210	10.13
12	272	001157	9.73
13	273	001126	9.34
14	274	001074	8.94
15	275	101043	8.55
16	276	001012	8.16
17	277	000765	7.83
18	300	000741	7.52
19	301	000717	7.23
20	302	000676	6.97
21	303	000654	6.69
22	304	100633	6.42
23	305	100612	6.16
24	306	100571	5.89
25	307	100550	5.63
26	310	000531	5.39
27	311	100512	5.16
28	312	100475	4.95
29	313	000460	4.75
30	314	000444	4.56
31	315	000430	4.38
32	316	100416	4.22
33	317	000403	4.05
34S	320	000370	3.88

Table 3.3.2-1. Typical GVVSSE Values (Continued)

ANGLE	OCTAL ADDRESS	OCTAL VALUE	GAIN, dB
35S	321	100356	3.72
36	322	000345	3.58
37	323	100333	3.42
38	324	100321	3.27
39	325	000310	3.13
40	326	100300	3.00
41	327	100267	2.86
42	330	100257	2.73
43	331	000247	2.61
44	332	100237	2.48
45	333	000227	2.36
46	334	100220	2.25
47	335	000211	2.14
48	336	000203	2.05
49	337	000174	1.94
50	340	000165	1.83
51	341	100157	1.73
52	342	000150	1.63
53	343	100143	1.55
54	344	000135	1.45
55	345	000127	1.36
56	346	000121	1.27
57	347	000114	1.19
58	350	000107	1.11
59	351	100102	1.03
60	352	000076	0.97
61	353	100072	0.91
62	354	100066	0.84
63	355	000062	0.78
64	356	100056	0.72
65	357	100053	0.67
66	360	100050	0.63
67	361	100044	0.56
68	362	100041	0.52
69	363	100036	0.47
70	364	100033	0.42
71	365	100030	0.38
72	366	100027	0.36
73	367	100024	0.31
74	370	100022	0.28
75	371	000020	0.25
76	372	000016	0.22
77	373	100014	0.19
78	374	100011	0.14
79	375	000007	0.11
80	376	100006	0.09
80S	377	100006	0.09

Figures 3.3.2-3 and 3.3.2-4 demonstrate how the software uses the sensor control values. One scale of the graph represents the gain value obtained from the GVVSSE table and the second scale represents the adjusted gain value as loaded into the VDGA. Because of the scaling of the values in the VDGA, the gain value in the VDGA must be less than 64 dB. The S(X) values represent the desired switch points and the P(X) values represent the amount by which the VDGA is to be modified when the sensor switching occurs. The switch point delta (DEL) is a commandable value in the constants memory.

The following description applies to the ASGC mode only. It is desirable that the switching occur at exactly the points defined by S(X) where $1 \leq X \leq 3$. Since the sensor switching is under software control, the switching cannot be done at exactly the points desired due to the rate of monitoring the VDGA value. The constant serves to define a band about the switch points. If, for instance, the gain in the VDGA is increasing, switching will occur at some point after S(X)-DEL. When the switching does occur, P(X) will be subtracted from the value in the VDGA. If, however, the gain in the VDGA is decreasing, switching will occur at some point after S(X)-P(X)+DEL.

For the along track gain control (ATGC) mode, described in a later section, the S(X) values define the exact decision points for selecting sensor and VDGA gain based upon GVVSSE gain. The PMT 1/9 mode may be bypassed by setting P(2) to zero and adjusting accordingly.

When selecting values for S(X) and P(X), care should be taken to ensure that $S(X)-P(X) > DEL$. Otherwise, a negative value can occur for the gain and produce erroneous results.

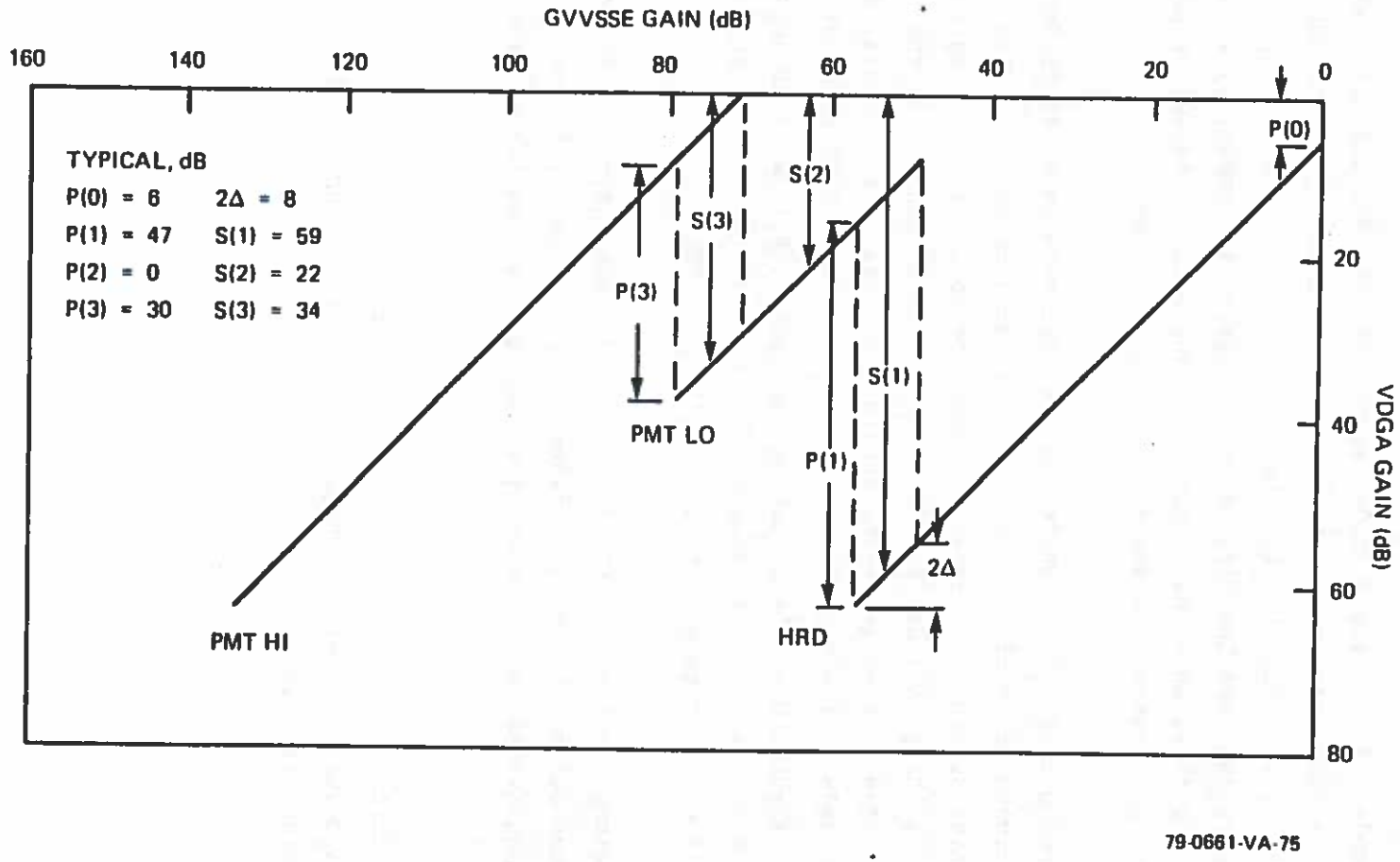
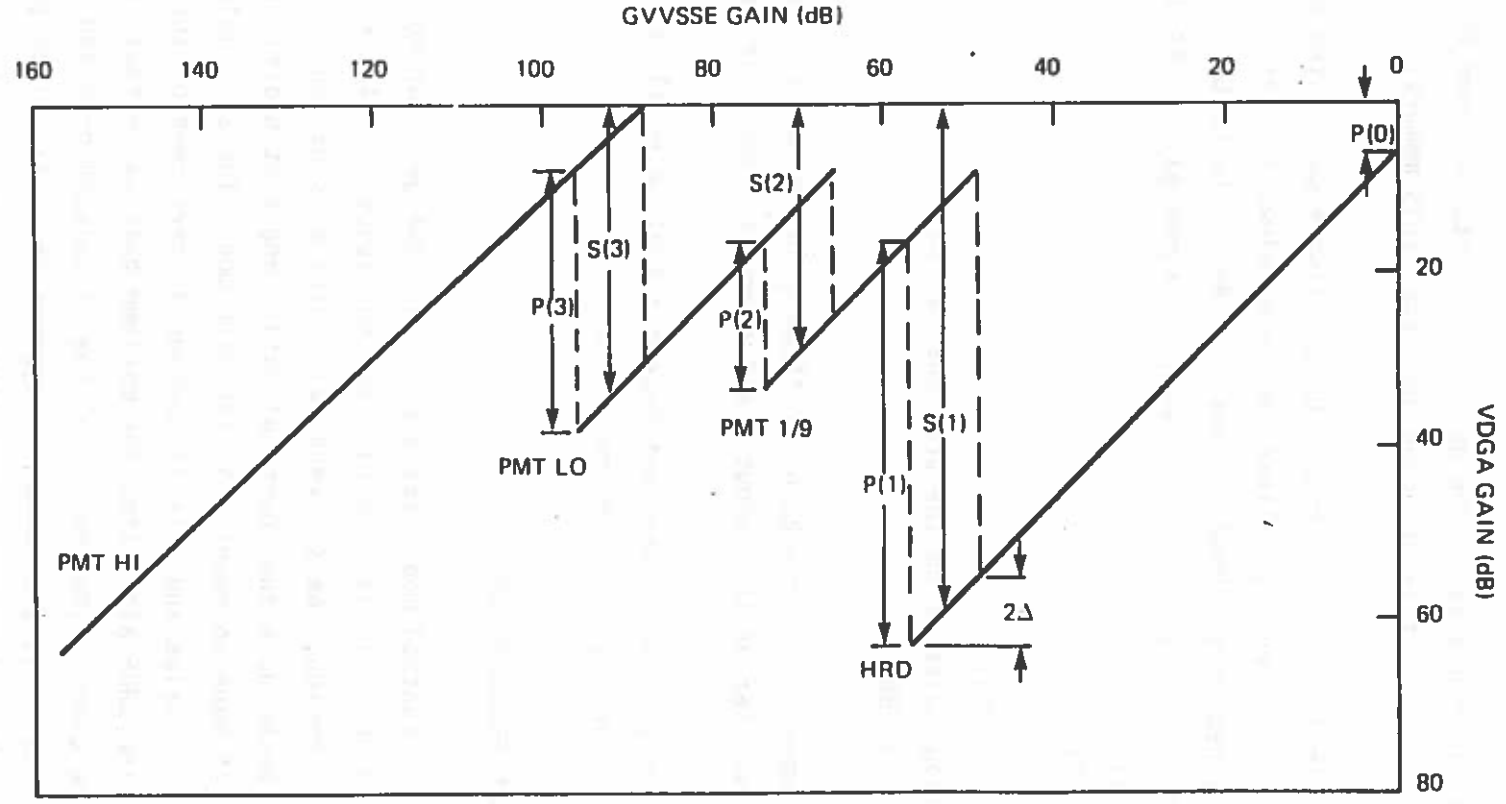


Figure 3.3.2-3. Sensor Switch Points - No PMT 1/9



TYPICAL, dB

P(0)	= 6	2Δ	= 8
P(1)	= 47	S(1)	= 59
P(2)	= 17	S(2)	= 29
P(3)	= 30	S(3)	= 34

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Figure 3.3.2-4. Sensor Switch Points - PMT 1/9

3.3.2.5.2.1.4 Selecting Maximum Gain Limit

There is a maximum limit placed on the gain values obtained from the GVVSSE table and BRDF. This limit is uplinked into constants memory.

This maximum gain limit may be overridden by a software-calculated maximum gain value if it is smaller than the uplinked maximum value. The largest gain value that can be contained in the VDGA is less than 64 dB. Using G as the gain from the GVVSSE table and sensor PMT HI with a maximum gain of 64 dB, the following equation exists:

64 = G+P(0)-P(1)-P(2)-P(3)

solving for G:

G = 64-P(0)+P(1)+P(2)+P(3)

Substituting the P(X) values from the previous section, give:

G = 64-6+47+0+30 = 135 dB

This is the software-computed maximum gain for these gain constants. The software will use the smaller of the computed and stored maximum gain values.

The uplinked maximum gain value does not become effective until the positive end-of-scan region following the reception of the value.

3.3.2.5.2.2 Along Track Gain Control

The along track gain control mode uses a constant VDGA gain during the active scan region, and the gain is changed along the spacecraft track only. During each end-of-scan region, the software calculates a scene source elevation (SSE) angle based upon the source elevation angle at nadir; the azimuth angle and height have no meaning in the ATGC mode. The SSE angle is then modified by the bias value and a table look-up is performed on the GVVSSE table and modified by the BRDF algorithm. The maximum gain value test is then made and the gain value used is the smaller of the calculated gain and the maximum gain. The gain value is then compared against the S(X) switch points and the gain value is adjusted by the appropriate P(X) values and the sensor is selected. Unlike the ASGC mode, the switch point delta has no meaning in the ATGC mode.

The command becomes effective only during the positive end-of-scan region following the processing of the command. Thus, the gain control mode cannot be changed during an active scan region.

3.3.2.5.2.3 Preset Gain Control

The four preset gain control commands provide manual control of the VDGA gain and sensor selection. The command, however, does not become effective until the next positive end-of-scan region following the processing of the command. The sensor selected and gain are then used during each active scan region until changed by another gain command.

The maximum gain test is not made on preset gain values. The OLS is initialized to preset HRD with a gain of 0 dB.

3.3.2.5.2.4 T Channel Gain Control

A GNC subcommand is available for controlling the four T channel gain bits TG1-TG4. The LSB (TG1) represents a gain of 0.2313 dB. The OLS is initialized to a gain of .925 dB, gain state 4 (0100). Subcommands are also available to control the left and right channel gain independently.

3.3.2.5.2.5 T Channel Level Control

A GNC subcommand is available for controlling the four T channel level bits TL1-TL4. The LSB (TL1) represents a 1.02K shifts at 210°K. The OLS is initialized to the set point of 210°K at TL4 ...TL1 = 1000. A table of level state as a function of M1 mirror temperature is provided with the data for each OLS system.

3.3.2.5.3 Data Storage - SDC, RLC

The stored data control (SDC) command is used for data storage. Primary recorders (PR) 1 through 4 can be selected to the record mode if the selected PR is already off. PR0 and PR5 are used for test only and enable the

formatters without selecting a recorder. Either the stored data fine (SDF) formatter or the stored data smooth (SDS) formatter can be selected to one or more recorders. In addition, the SDF formatter can be selected to LF data, TF data, or interleaved LF and TF data.

Software interlocks are provided to ensure that a PR has been off for at least 5 seconds before a PR on command begins its execution. If the selected PR has been off for at least 5 seconds, there is no start-up delay. A PR on command will be rejected and noted as a command error if that PR is unavailable (already on).

Since a formatter can be commanded to all PR's, it is possible to send an SDF command of one data type to one PR and SDF command of another data type to another PR. However, it should be noted that if that is done, the second data type will go to both PR's and the speed of the first PR will not change when the second command is executed. The second PR will record at the appropriate speed for the second command data type.

In addition to terminating the record command with an off command, the software will automatically terminate the command (and make it available for a playback command) when an end of tape is encountered.

The recorder location counter (RLC) command provides a means of setting the value of each recorder's tape position counter. The value is automatically set to 0 when a recorder reaches beginning of tape.

3.3.2.5.4 Data Readout - SDC, RTR

The SDC command, is used for stored data playback and the RTR command is used for real time data readout.

3.3.2.5.4.1 Stored Data Playback - SDC

PR1 through PR4 can be selected to the playback mode if the selected recorder is already off. If the PR is on or the playback channel is already in use when the playback command is received, a system error will be noted and the command will be rejected.

The PR can be selected to any one of four channels in either clear or encrypt mode and at high or low speed playback.

The playback command begins execution by enabling the data transmitter (DT) connected to the selected channel for 10 seconds. It then turns on the PR. If the DT is interlocked or has already been on for 10 seconds (i.e. TBC command), the playback starts immediately provided the PR has been off for the previous 5 seconds. If it has not been off the required 5 seconds, the software will delay the playback until this requirement is satisfied.

The SDC command can also place any PR in a fast forward mode. Again, the selected PR must have been turned off to execute a fast forward command. The action of the fast forward is to move the tape in a forward direction until turned off either by an end of tape indication or off command. The PR can then be recommanded to play back the data. This feature allows many playbacks of the same data. The following nominal information is useful in commanding the fast forward mode. One reel of tape holds 2100 feet. Tape slew-up and slew-down times are 5 seconds each.

Inches Per Second	Mode
40	Fast Forward
20	SDF Interleaved Record
10	SDF Noninterleaved Record
1	SDS Record
20	LOW Speed PLayback
40	HIGH Speed Playback

An SDC OFF command to a PR in PLAYBACK will turn off the PR and associated channel and DT.

In addition to an off command terminating a playback, a beginning of tape signal will terminate the playback, making the PR available for a fast forward or record command.

3.3.2.5.4.2 Real Time Data - RTR

The RTR command is used to connect the real time data (RTD) formatter to one or more channels. If the selected channel is already in use by a PR, the command is rejected. Each channel can be set up in the clear or encrypt mode.

The data type is selected to either LF/TS or TF/LS data. Consecutive on commands can be used to connect the formatter to additional channels, change data type, or change the clear/encrypt state of the text.

The direct mode data message (DMDM) can also be turned on and off with consecutive RTR on commands. The DMDM will be keyed to a particular channel or channels and those channels must be commanded in order to change the state of the DMDM. That is:

RTR CH1 ENCRYPT DMDM TFLS

will send encrypted TFLS data and DMDM down channel 1. If the following command is then executed:

RTR CH2 CLEAR LFTS,

encrypted LFTS and DMDM will be sent down channel 1 and clear LFTS and DMDM will be sent down channel 2.

If an RTR CH2 OFF command is sent, encrypted LFTS and DMDM will be sent down channel 1. If, instead, an RTR CH1 OFF command is sent, CLEAR LFTS (no DMDM) will be sent down channel 2 since DMDM was keyed to channel 1 only.

The DMDM is located in pages 1-7 of stored program memory. It boundaries are defined in uplink memory page 0. Both a starting address and memory length must be defined.

When an RTR is commanded on, the encrypter and DT connected to the specified channel is turned on for 10 seconds prior to enabling the RTD formatter. If the DT was interlocked, there is no delay and the formatter is turned on immediately. If other commands are received which use other channels, they are stored for later execution. Only one DT is warmed up at a time. If many commands are stored for later execution, they will be be executed according to the priority: channel 1 through channel 4.

An RTR channel OFF command will turn off a channel and associated DT which were commanded on by an RTR command.

3.3.2.5.5 Mission Sensor Programming - SSC, MAC

Mission sensor processing will be enabled in both the stored data record and real time readout modes. The SSC command and data in stored program memory page 0 control the sampling of the mission sensor data. The SSC command will turn on or off the selected sensor (SSA-SSL). The SSC command will also be used to control the MODE 1 and MODE 2 lines going to each sensor. The MODE on command will either pulse the mode line or set the mode line to on. The MODE off will either set the MODE line to off or to hold. MODE 1 and MODE 2 operate identically. The definition of whether the mode lines are pulsed or level is placed in two locations of stored program memory page 0. Bit 1 position 1 refers to sensor A and bit position 12 refers to sensor L. A logic 1 indicates pulsed type and a logic 0 indicates level type.

In addition, an 8-bit data value can be transmitted to any sensor. The data value must first be set with an SSC command. A separate SSC command is then executed to transmit the last data value received to the sensor. This same data value can be sent to other sensors with transmit commands. It is not necessary to resend the data command if the data value does not change. This two command sequence should not be programmed from more than one command source (real time, main, or orbit programs) at the same time in order to prevent command interleaving resulting in erroneous operation.

The sampling (one sample per second) of the data is controlled by the SS format words in stored program memory page 0. The SS FMT WD #1 defines the first sensor to be sampled and SS FMT WD #12 defines the last sensor to be sampled. The sampling will occur even if power has not been applied to the sensor.

In addition to the sensor ID, each format word defines the number of 36-bit words to sample from the sensor and tells whether to place that data in the LS stored data frames or in the TS stored data frames. The sensors destined for the LS frames should always be sampled first (occur first in the table) and the TS destined data should be sampled last. The LS and TS destined data should not be intermixed. Also unused format words (zero word count)

should be placed last in table. The LS data frames are capable of accepting at least 1800 bits of mission sensor data and the TS data frames are capable of accepting at least 3528 bits of mission sensor data.

The MAC command sequence can be used to send a large block of data to a specified mission sensor using the 8-bit serial interface. The data block can consist of up to 32767 words where the last word of the block is a checksum on the previous words. The checksum is computed starting with the first word of the load and consists of an ADD followed by a cyclic 1-bit right shift. The OLS will compute the checksum as the load is being received and indicate a processor error if it does not match the last word in the load.

Three MAC commands must precede the load sequence where the first two can be sent in any order and define the number of words to be loaded. The MAC word count command defines the 2^0 - 2^9 bit values of the load length and the MAC word count extension command defines the 2^{10} - 2^{14} bit values of the load length. The final MAC command must be a MAC mission sensor load command and it also defines the sensor to be loaded.

The MAC LOAD EST will turn on when the final MAC command is executed and turn off when the load length count has been satisfied.

During the load, the data file is echoed on MDDATA preceded by a 3-word header and is terminated by a checksum on the entire load file including the checksum in the load. The 3-word header consists of SYNC, SYNC, ID where SYNC = 0137465 and ID = I07XXX; where I is the processor ID and the 07 specifies that the following data is a MAC load mission sensor echo. The XXX refers to the CPU telemetry table in use and will normally be 000 unless a different table has been uplinked. The checksum is an ADD followed by a circular right 1-bit shift of the data as it is received starting with data 1 and ending with data n. The echoes will lag the data uplink by two words. When the MAC load mission sensor command is executed, SYNC 1 will be downlinked. Receipt of data 1 will downlink SYNC 2. Receipt of data 2 downlinks ID. Receipt of data 3 echoes data 1 and so on up to receipt of data n echoes data n-2, data n-1, data n, and downlinks checksum.

3.3.2.5.6 Stored Program Programming - MAC, UPC, OCP

The stored program memory is composed of eight 256-word pages numbered page 0 to 7. Page 0 is reserved for operational constants and the GVVSSE table. Pages 1-7 are reserved for the main memory, orbit memory, and DMDM memory, in that order. Main memory always starts in location 0400. The orbit memory starting location is defined in page 0 and must always be an even address. The DMDM starting location and length are also defined in page 0.

3.3.2.5.6.1 Loading the Stored Program Memory - MAC

The stored program memory is loaded by a sequence of three MAC commands. A MAC address command defines the address (0-256) within a page and a MAC word count (1-1023) defines the number of words to load, starting at the defined address. A word count of 0 defines a 1024-word load. The MAC word count and MAC address can be executed in any order. The final command in the sequence is a MAC LOAD PAGE command defining the page in which the load is to start. The data file to be loaded is then uplinked.

At the same time the load is taking place, the data file is echoed on MDDATA preceded by a 30-word header and terminated by a checksum. The 3-word header consists of SYNC, SYNC, ID where SYNC=0137465 and ID=I01XXX; where I is the processor ID and the 01 specifies that the following data is a MAC load page echo. The XXX refers to the CPU telemetry table in use and will normally be 000 unless a different table has been uplined. The checksum is an odd followed by a circular right 1-bit shift of the data as it is received (except parity error bit is placed in bit 16) starting with data 1 ending with data n. The echoes will lag the uplinking of the data by two words. When the MAC load page command is executed, SYNC 1 will be downlinked. Receipt of data 1 will downlink SYNC 2. Receipt of data 2 downlinks ID. Receipt of data 3 echoes data 1 and so on up to receipt of data n echoes data n-2, data n-1, data n, and downlinks checksum.

A MAC command sequence consisting of address, word count, and dump page can be used to verify the actual contents of memory. In this case, the dump file uses MDDATA and consists of SYNC, SYNC, ID, dump data where ID=I02XXX signifies a dump page file.

As an assist in performing a MAC load, a MAC LOAD EST has been provided which comes on during every MAC load and turns off when the word count has been satisfied.

3.3.2.5.6.2 Controlling the Stored Program - UPC, OCP

The UPC command is used to control the stored program. A single UPC command can turn off the main program, orbit program, or both. Two commands are needed to turn on either memory, an address within page UPC must initially be sent followed by a set page and turn on command. The memory to which the address points is the one that is turned on. This address should always be an even number. Commands should always be in even numbered memory locations and their associated time tags in the next odd numbered location. Since a two command sequence is needed to turn on a stored program (or cause a jump), this should not be programmed to occur at the same time in both memories (or real time) in order to prevent command interleaving resulting in improper operation.

Main memory time tags have an LSB (bit 1) of 4 seconds and an MSB (bit 15) of 2^{16} seconds. Orbit memory time tags have an LSB (bit 1) of 1/2 second and an MSB (bit 15) of 2^{13} seconds. Main memory commands will be executed when the associated time tag equals the elapsed time count (ETC). If the time tag is less than the ETC, it is interpreted as a bad time tage and not executed. The main memory can be placed in standby with a UPC command from main memory (not real time or orbit memory). In standby, no commands will be executed until the ETC is decreased by at least 2 seconds.

The orbit memory commands are executed when the associated time tag equals the orbit clock. If the time tag is less than the orbit clock it is a bad time tagged command and not executed. The orbit clock can be preset in any of four ways with an OCP command. An OCP zero command will zero the orbit clock. An OCP indirect command will set the orbit clock to the value in page zero which is addressed by the OCP indirect command. An OCP direct command can define the preset value within the command itself. The OCP direct command can define present values from 0.0 to 127.5 seconds. The OCP adjust command can be used to adjust the orbit clock -64.0 to +63.5 seconds or -128 to +127 minutes.

In both memories if the data uplinked by the MAC load has a parity error in either the command, time tag, or both, that command is executed only if the parity override command is on. The parity override is set by the SPC command, either in real time or from memory. Parity override commands from memory require good parity for execution if the parity override is off.

Some command interlocks are associated with memory commanding in addition to the main memory standby command, which can be executed from main memory only. A MAC command cannot be executed from memory and an AIS (CMD016) jump or skip command can be executed from memory only and not in real time.

Commands with identical time tags can be placed in both memories. The exact number depends on program loading and is currently equal to up to 20.

3.3.2.5.7 Miscellaneous Control - GNC, TBC, PSC, AIS, SPC

The following commands are a combination of seldom-used commands and commands that can provide individual control over parts of the OLS that may have been set up by some of the more basic commands or the flight software itself.

3.3.2.5.7.1 Sensor Segment Selection - GNC

Subcommands of the GNC command can override the automatic selection of the T, HRD, and PMT sensor segments. Any combination of the left, mid, and right segments can be commanded to be used for the entire active scan line overriding the automatic segment switching (overscan is always done in automatic). Each sensor is commanded independent of the others. The command can also switch the segment selection back to the automatic mode.

3.3.2.5.7.2 Transmitter/BBT Control - TBC

The SDC playback and RTR commands set up the data transmitter (DT) and encrypter (BBT) power as commanded. The TBC command can be used to override the normal selection of DT and BBT, turning a DT on or off and selecting the BBT to clear or encrypt. If a DT or BBT was turned on with the TBC, it must be eventually be turned off with the TBC unless an RTR or SDC command subsequently turns on the associated channel.

Another function of the TBC command is to interlock the DTs. When a DT is interlocked, its power is turned off and no other commands, RTR, SDC, or TBC DT on, can turn it on. The DT interlock off will remove the interlock but will not restore power to any DT which had previously been turned on prior to application of the interlock.

One final function of the TBC command is to set up the output switching unit (OSU). The flight software will initialize the OSU to connect channel 1 to DT1, channel 2 to DT2, channel 3 to DT3, and channel 4 to DT4. This configuration can be rearranged with the channel - DT select subcommand. The software will not, however, allow the connection of a single channel to more than one DT or multiple channels to a single DT.

3.3.2.5.7.3 Primary Sensor Controls - PSC

The PSC command is the only command which can be executed via the S/C Location Data interface. All other commands received on this interface will be rejected and placed in the System Error Table.

The PSC subcommands in addition to the scanner and PMT power commands previously discussed can turn the T channel cone cooler heaters on and off or enable and disable the image motion compensator (IMC). The IMC is initially enabled so the only purpose of this command is to disable it in case of an IMC failure.

A PSC subcommand is provided to set the scanner amplitude limit to a value other than the initialized value of 1050.5 delphis.

A PSC subcommand also provides a fast convenient way to shed OLS loads but still maintain SDS record mode.

In the event of an encoder Delphi track failure, the encoder simulator can be turned on. If the control track from the encoder is still functioning, the encoder simulator should be commanded to the locked mode. This will provide a good match to the actual scanner position in frequency, amplitude, and offset. This will allow the collection of video data in a slightly degraded mode. If the control track is not functioning correctly, the encoder simulator should be commanded to the free run mode. This allows the collection of mission sensor data and stored telemetry. The encoder simulator will output a sine wave at close to nominal scanner frequency in free run. Two constants, PDELBS and PDELSP, in the constants part of uplink memory are provided to fine tune the encoder simulator in the locked mode due to variations in the actual scanner motion. PDELSP adjusts the separation between DOS 0 and DOS 1 as output by the encoder simulator. This constant can be adjusted to remove any line to line jitter. PDELBS adjusts the bias and is used to align the encoder simulator nadir to the scanner center of motion thus providing data collection symmetric to the scanner. The value of the LSB of each constant is 1.878 microseconds and represents delay or advance in encoder simulator start up in end of scan.

3.3.2.5.7.4 Auxiliary Instruction Set - AIS

The AIS command allows dynamic programming in the stored main and orbit memories. The AIS commands are intended to be used in the stored memory although all but the jump and skip commands can be executed as real time commands.

A 15 bit accumulator (sign bit in bit 15) that can be loaded from or stored into any page in uplink memory is provided. Two's complement adds and subtracts can be performed on the accumulator using an operand in uplink memory. A set page command is provided to indicate the page to which the instruction operand is referenced. The address within the page is set by the command itself. Since the page register does not change until commanded, this command need be sent only once if all AIS memory references are confined to the same page. A CLEAR command is available to clear the page register and/or the accumulator to zero.

The jump command will always jump to a location within the page in which the jump instruction resides. The skip commands can, however, skip across page boundaries.

The skip command tests the accumulator for various conditions (<0, $=0$, >0, ± 0, etc.) and skips the next command/time tag pair if the tested condition is true.

It should be recognized that this command set operates on one accumulator and one page register making it possible for one program memory (or real time command) to set or clear a flag which can be tested or changed by the other program memory.

The following program shows two uses of the AIS instructions. The first part simply increments location COUNT in page 7 on every pass through the program. The second part causes the main program to sequence through a table of three commands, executing a different one on each pass through the program.

```
Page 5      SET Page 7
            TT
            LD COUNT
            TT
            ADD ONE
            TT
            ST COUNT
            TT
            LD TBL
            TT
            ST TMP
            TT
            LD TBL+1
            TT
            ST TBL
            TT
            LD TBL+2
            TT
            ST TBL+1
            TT
            LD TMP
            TT
            ST TB+2
            TT
            SET PAGE 5
            TT
            ST CMDX
            TT
CMDX        variable command
            TT
            .
            .
            .
```

```
page 7  TBL  CMD  1
             CMD  2
             CMD  3
        TMP       0
        COUNT     0
        ONE       1
```

3.3.2.5.7.5 Special Purpose Command - SPC

The execute command can be used from memory or real time to set or reset the parity override. If sent real time, the action takes place independent of parity. From memory, the parity must be odd or the override already on, for execution.

A NO-OP command is provided which causes no action and can be used to delete commands in the stored program memory without changing the addresses of other commands in the stored program memory.

3.3.2.5.7.6 Stored Program Constants Controls

There are other controls in the stored constants area of the stored program that have not been previously discussed. An inhibit offset bit (INHOFS) is available which: When set to a 1, it will inhibit the flight software from correcting the video sampling for scanner offset when the OLS is in the REAL ENCODER mode as contrasted with the ENCODER SIMULATOR mode which has not inhibit.

Another bit is available in stored program memory for controlling the direction of the image motion compensation. This bit should be set to 0 for a forward (+Y direction) flying spacecraft and a 1 for a backward (-Y direction) flying spacecraft.

3.3.2.5.8 Diagnostic Commanding - MAC, SPC, SPARES

In addition to the MAC command sequence that loads and dumps pages of the stored program memory, the MAC command can also be used for diagnostic purposes.

A three MAC command sequence can be used to patch and dump the operational flight software. The MAC load/dump BLOCK command is used for this purpose. Any memory block from 0 to 077 can be loaded into or dumped. The operation is the same as for the MAC PAGE command, i.e., word count and address MAC commands must be executed. The data file for the BLOCK load command contains no parity bit in bit 16. Bit 16 is used as an information bit in the flight software. Load echoes and dumps are preceded by a header. The tag bits in the ID of this header word are defined in the Operator's Manual (Appendix 1).

The other MAC command sequence is to change or dump the CPU telemetry address table. CPU telemetry is described in Section 3.4. The CPU telemetry address table contains the absolute addresses of the 36 telemetry parameters that appear on channels 1-36. Any or all channels may be redefined by storing the address of the desired parameter in the channel address position of the table. Also, the sampling rate on any parameter can be increased by supplying its address in more than one channel. Bits 1-9 of the CPU telemetry header ID word are reserved for controlling the configuration of the parameters. These bits are set to zero in the flight software as initially loaded. For this reason, a MAC TEL load sequence must always include an ID word as the first word of the load data file. Bits 1-9 should be set up so that the CPU telemetry can be identified to the new parameters when it appears in the data stream. The new channel addresses follow the ID word. The MAC address word contains the number of the first channel to be changed. The MAC word count always is one greater than the number of channels changed (because of the ID word). Each new parameter address and the ID word must have odd parity, as set by bit 16. For example, if it is desired to change the parameters associated with channels 33 and 34, the following sequence would be uplinked.

UPLINKED	CVDATA	MDDATA
MAC ADR 33	ICMD	CPU TLM
MAC WC 3	ICMD	CPU TLM
MAC TEL LOAD	ICMD	SYNC
ID (BITS 1-9 =XXX)		SYNC
ADDRESS FOR CH 33		ITT BBB
ADDRESS FOR CH 34		ID (BITS 1-9=XXX)
		ADDRESS FOR CH 33
		ADDRESS FOR CH 34
		CHECKSUM
		CPU TLM

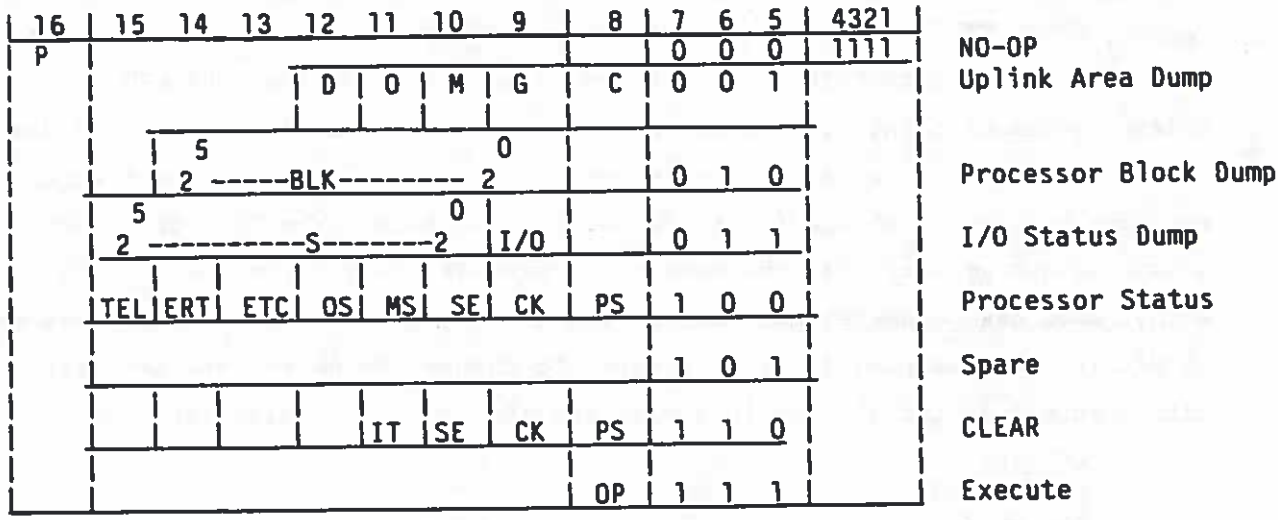
where I = processor ID, CMD is the command uplinked
TT = dump data type (see Appendix 1)
BBB = baseline telemetry (XXX replaces BBB after above execution)

The MAC TEL DUMP command will start dumping the telemetry address table starting with the channel address specified.

The SPC command can be used to dump information without the need for determining the starting address or length of dump. Such information includes the stored program constants memory. GVVSSE table, main program, orbit program, and DMDM memory. A single SPC command can also dump a specified memory block (0-077).

The processor communicates with the SPS via an input/output bus using various select codes. The SPC command can cause the processor to read the input bus using any input select and dump this information. In general, the processor saves the image of all output selects. An SPC command can also be used to dump the image of any output select. The definition of the processor I/O can be found in the Program Maintenance Manual.

The SPC command is useful in dumping certain status information as listed below:



C		Operational Constants
G		GVVSSE Table
M		Main Program
O		Orbit Program
D		DMDM Memory
I/O	0,	I/O Output Word
	1,	I/O Input Word
S		I/O Select Code
PS		Processor Status Word (CLEAR PS Clears Error Bits Only)
MS		Main Program Address Counter and Status
OS		Orbit Program Address Counter and Status
SE		System Error Table
CK		Checksum Error Table
ERT		OLS Status Error Time Code
ETC		Sampled Elapsed Time Count
OP		Override Parity
TEL		OLS TEL Table
IT		Init Count in Processor Status Word

Uplink Memory

Priority of Dumping Multiple Dumps Starts with Bit 8.

3.4 Telemetry

Information on the status of the OLS is communicated to the ground by means of telemetry. All OLS telemetry information is communicated to the Spacecraft Programmable Information Processor unit (PIP), where it is formatted along with other spacecraft telemetry for direct transmission to the ground, or for on-board recording. The OLS telemetry falls into two major categories: Equipment Status Telemetry (EST) which is carried on discrete lines to the PIP, and OLS CPU Telemetry which consists of messages output by the OLS processor using the Memory Dump interfaces to the PIP.

3.4.1 Equipment Status Telemetry (EST)

The 5D-3 ESTs are classified into five types of monitors - power, environment, performance, configuration and fault isolation. The list includes 88 analog and 60 digital ESTs. Of the 60 digital signals, 12 are time multiplexed (3 TAG, 9 DATA) and contain 61 information bits. Table 3.4.1-1 contains the list of OLS ESTs. A more detailed description of each EST follows the table.

TABLE 3.4.1-1 EST SIGNALS

OLS EST No.	S/C #	Designation	Type	Analog/ Digital	Function
1	348	+28 V S/C Inverter 1	Power	A	28 volts Spacecraft to OLS Inverter 1
2	349	+28 V S/C Inverter 2	Power	A	+28 volts Spacecraft to OLS Inverter 2
3	350	+5V BB1	Power	A	BB1 +5V Power Converter Output
4	351	+5V BB2	Power	A	BB2 +5V Power Converter Output
5	352	+5V BB3	Power	A	BB3 +5V Power Converter Output
6	353	+28 V S/C Fuse	Power	A	+28 V S/C to DME's, Relay and Cone HTR summed after fuse
7	354	+5V S/C	Power	A	+5 volts Spacecraft to OLS
8	355	+5 V S/C OSU X	Power	A	+5 volts Spacecraft to OSU X
9	356	+5 V S/C OSU Y	Power	A	+5 volts Spacecraft to OSU Y
10	357	-19.3 V (U)	Power	A	-19.3 volts Unregulated Uninterrupted
11	358	+19.5 V (U)	Power	A	+19.5 volts Unregulated Uninterrupted
12	359	-12.8 V (U)	Power	A	-12.8 volts Unregulated Uninterrupted
13	360	+13.4 V (U)	Power	A	+13.4 volts Unregulated Uninterrupted
14	361	+4.4 V (U)	Power	A	+4.4 volts Unregulated Uninterrupted
15	362	+12 $V(A)_1$	Power	A	+12V Regulated for Analog Circuitry (PS1)

TABLE 3.4.1-1 EST SIGNALS (continued)

OLS EST No.	S/C #	Designation	Type	Analog/ Digital	Function
16	363	+12 V $(A)_2$ Reg	Power	A	+12V regulated for Analog Circuitry (PS2)
17	364	+12 V $(D)_1$ Reg	Power	A	+12V Regulated for Digital Circuitry (PS1)
18	365	+12 V $(D)_2$ Reg	Power	A	+12V Regulated for Digital Circuitry (PS2)
19	366	+5.3 V $(D)_1$ Reg	Power	A	+5.3V Regulated for Digital Circuitry (PS1)
20	367	+5.3 V $(D)_2$ Reg	Power	A	+5.3V Regulated for Digital Circuitry (PS2)
21	368	-12 V $(A)_1$ Reg	Power	A	-12 V Regulated for Analog Circuitry (PS1)
22	369	-12 V $(A)_2$ Reg	Power	A	-12 V Regulated for Analog Circuitry (PS2)
23	370	+12 V (M)	Power	A	+12 V Regulated Uninterrupted Power
24	371	-13.1 (U) to HVPS	Fault Isolation	A	-13.1V Unregulated to HVPS
25	181	PSU Temp	Environment	A	PSU Temperature
26	182	SPSE Temp	Environment	A	SPS Core Memory E Temperature
27	183	SPU Temp	Environment	A	SPU Temperature
28	185	-Y SSS Temp	Environment	A	-Y SSS Structure Temperature
29	186	+Y SSS Temp	Environment	A	+Y SSS Structure temperature
30	187	Relay Optics Temp	Environment	A	Relay Optics Temperature
31	188	M1 Temp	Environment	A	Mirror 1 (Primary) Temperature

TABLE 3.4.1-1 EST SIGNALS (continued)

OLS EST No.	S/C #	Designation	Type	Analog/ Digital	Function
32	189	T Patch Temp	Performance	A	T Detector Cold Patch Temp
33	190	T Cone Temp	Performance	A	T Detector Cone Cooler Temp
34	191	T Clamp Temperature	Performance	A	T Detector Reference Clamp Temp
35	193	T Cal Temp	Performance	A	Temperature of T Cal
36	194	T Cal/Clamp	Performance	A	T Left and Right Cal and Clamp Video
37	195	T Cal/Clamp Backup	Performance	A	T Backup Left and Right Cal and Clamp Video
38	196	T Patch HTR	Performance	A	T Cold Patch Heater Power
39	197	T Left/Right	Performance	A	T Detector Left/Right Preamp dc Level
40	198	PMT Cal	Performance	A	PMT LED Calibration
41	199	PMT Cal Backup	Performance	A	PMT Backup LED Calibration
42	201	VCO Error	Fault Isolation	A	VCO Error
43	376	DME A Current	Performance	A	Drive Motor Current if DME A is active
44	377	DME B Current	Performance	A	Drive Motor Current if DME B is active
45	202	SENSEL	Configuration	A	Sensor Mode Select (HRD, PMT LO, PMT HI, PMT 1/9)
46	203	DOC SQB	Configuration	A	Monitors Scanner Cover Release Mechanism Squibs
47	204	DCC SQB	Configuration	A	Monitors Cooler Release Mechanism Squibs

TABLE 3.4.1-1 EST SIGNALS (continued)

DLS EST No.	S/C #	Designation	Type	Analog/ Digital	Function
48	205	SCNR CAGE SQB	Configuration	A	Monitors Pin Release Mechanism Squibs
49	206	PMT HV	Configuration	A	PMT High Voltage (ON or OFF)
50	209	PR1 RDY	Performance	A	PR1 Ready Voltage
51	210	PR1 Temp	Environment	A	PR1 Temperature
52	211	PR1 Pres	Environment	A	PR1 Pressure
53	24	PR1 Motor Current	Performance	A	PR1 Motor Current
54	32	PR1 Servo Error	Performance	A	PR1 Servo Error
55	212	PR1 EOT/BOT	Configuration	A	End of Tape/Beginning of Tape for PR1
56	215	PR2 RDY	Performance	A	Same as PR1 but for PR2, PR3 and PR4
57	217	PR2 Temp	Environment	A	
58	218	PR2 Pres	Environment	A	
59	56	PR2 Motor Current	Performance	A	
60	64	PR2 Servo Error	Performance	A	
61	219	PR2 EOT/BOT	Configuration	A	
62	222	PR3 RDY	Performance	A	
63	223	PR3 Temp	Environment	A	
64	225	PR3 Pres	Environment	A	
65	72	PR3 Motor Current	Performance	A	

TABLE 3.4.1-1 EST SIGNALS (continued)

OLS EST No.	S/C #	Designation	Type	Analog/ Digital	Function
66	80	PR3 Servo Error	Performance	A	
67	226	PR3 EOT/BOT	Configuration	A	
68	229	PR4 RDY	Performance	A	
69	230	PR4 Temp	Environment	A	Same as PR1 but for PR2, PR3 and PR4
70	231	PR4 Pres	Environment	A	
71	88	PR4 Motor Current	Performance	A	
72	96	PR4 Servo Error	Performance	A	
73	233	PR4 EOT/BOT	Configuration	A	
74	383	PSTATE	Fault Isolation	A	Processor State Status
75	207	SPSF TEMP	Environment	A	SPS Core Memory F Temperature
76	241	Scan Enable B	Configuration	D	Scan Enable to DME B Status
77	213	Cold Patch 1W Heater	Configuration	A	Cold Patch 1W Heater Status
78	235	Pwr Sup#1 Temp	Environment	A	Power Supply #1 Temp
79	242	Relay 2 Processor C	Configuration	D	Relay 2 Status
80	243	Relay 3 Memory E	Configuration	D	Relay 3 Status
81	244	Relay 4 Memory F	Configuration	D	Relay 4 Status
82	245	Relay 5 I/O X	Configuration	D	Relay 5 Status
83	246	Relay 6 I/O X	Configuration	D	Relay 6 Status
84	247	Relay 7 I/O Y	Configuration	D	Relay 7 Status
85	248	Relay 8 I/O Y	Configuration	D	Relay 8 Status
86	251	Relay 9 Analog	Configuration	D	Relay 9 Status

TABLE 3.4.1-1 EST SIGNALS (continued)

OLS EST No.	S/C #	Designation	Type	Analog/ Digital	Function
87	252	Relay 10 Formatter G	Configuration	D	Relay 10 Status
88	253	Relay 11 Formatter G	Configuration	D	Relay 11 Status
89	254	Relay 12 Formatter H	Configuration	D	Relay 12 Status
90	255	Relay 13 Formatter H	Configuration	D	Relay 13 Status
91	256	Processor Bus Select	Configuration	D	Processor C or D to Signal Bus
92	257	Memory Bus Select	configuration	D	Memory E or F to Signal Bus
93	258	IF Select	Configuration	D	Interface X or Y to Signal Bus
94	261	Gain Control Select	Configuration	D	Gain Control X or Y to Signal
95	262	Sensor Control Select	Configuration	D	Sensor Control X or Y to Signal Bus
96	263	Output Data Mux Selection	Configuration	D	Output Data Mux X or Y to Signal Bus
97	264	Encoder Processor (WF) Select	Configuration	D	Encoder Processor X or Y to Signal Bus
98	265	CLR/CLK SEL	Configuration	D	Clear/Clock Driver X or Y to Signal Bus
99	266	RTD Formatter Select	Configuration	D	RTD Formatter G or H to Signal Bus
100	267	SDF Formatter Select	Configuration	D	SDF Formatter G or H to Signal Bus
101	268	SDS Formatter Select	Configuration	D	SDS Formatter G or H to Signal Bus
102	271	SSP Formatter Select	Configuration	D	SSS Formatter G or H to Signal Bus

TABLE 3.4.1-1 EST SIGNALS (continued)

OLS EST No.	S/C #	Designation	Type	Analog/ Digital	Function
103	272	T Analog Select	Configuration	D	Selects data from TF, TS or TF', TS'
104	273	L Analog Select	Configuration	D	Selects data from LF, LS or LF', LS'
105	274	HRD Backup Select	Configuration	D	Selects HRD Backup Postamp
106	275	S0			
107	276	S1			SDF or SDS to PR1 through PR4 (8 bits)
108	277	S2			PR1 - PR4 or RTD - BB1 - BB4 (12 bits)
109	281	D1			BB1 - BB4 to DT1 - DT4 (8 bits)
110	282	D2			DT Pwr Enable (4 bits)
111	283	D3 12 Time Muxed Lines	Configuration	D	BB Pwr Enable (Clear or Encrypt) 4 bits
112	284	D4			PR Speed (16 bits)
113	285	D5			T Gain (4 bits)
114	287	D6			T Level (4 bits)
115	287	D7			IMC Enable (1 bit)
116	278	D8			BRDF RS-RV (2 bits)
117	288	D9			
118	291	Scan Enable A	Configuration	D	Scan Enable to DME A Status

TABLE 3.4.1-1 EST SIGNALS (continued)

OLS EST No.	S/C #	Designation	Type	Analog/ Digital	Function
119	292	RTD Enable	Configuration	D	RTD Mode Enabled
120	293	RTD TF/LS	Configuration	D	RTD TF/LS or LF/TS
121	294	SDF Enable LF	Configuration	D	SDF LF Mode Enabled
122	295	SDF Enable TF	Configuration	D	SDF TF Mode Enabled
123	296	SDS Enable	Configuration	D	SDS Mode Enabled
124	214	PMT Blank	Fault Isolation	A	PMT Blanker ON or OFF
125	297	Scan Offset	Performance	D	Scanner Offset wants to change
126	298	COM	Fault Isolation	D	Command Link Status
127	301	LOG	Configuration	D	L Channel Lin or Log Mode Select
128	220	Scanner Ready	Performance	A	Scanner Ready from DME
129	302	MAC Load	Configuration	D	MAC Load in Process
130	303	Processor Status	Fault Isolation	D	OLSP Program Status
131	221	+X, +Z HTR CTR	Configuration	A	+X, +Z SSS Heater Control
132	227	+X, -Z HTR CTR	Configuration	A	+X, -Z SSS Heater Control
133	228	-X, +Z HTR CTR	Configuration	A	-X, +Z SSS Heater Control
134	234	-X, -Z HTR CTR	Configuration	A	-X, -Z SSS Heater Control
135	304	PC Run	Configuration	D	Processor C Run/Load Status
136	305	PD Run	Configuration	D	Processor D Run/Load Status
137	306	Real Encoder	Configuration	D	Processor Encoder Source
138	307	DOCMD	Configuration	D	Operational Program Command Input Status

TABLE 3.4.1-1. EST Signals (Continued)

OLS EST No.	S/C #	Designation	Type	Analog/ Digital	Function
139	311	REDENC	Configuration	D	SSS Encoder Selection
140	312	VAC	Configuration	D	DME Drive Selection
141	-	PSU Spare	-	D	-
141 (OLS 13-up)	313	Sol. Cmd State	Configuration	D	Solenoid Command State
142	-	PSU Spare	-	A	-
143	-	PSU Spare	-	A	-
144	308	Free Run	Configuration	D	SPS Delphi Sim Status
145	-	PSU Spare	-	D	-
145 (OLS 13-up)	314	Sol. State	Configuration	D	Solenoid State
146	236	PS1 Status	Configuration	A	Power Supply 1 Status
147	237	PS2 Status	Configuration	A	Power Supply 2 Status
148	241	Pwr Sup #2 Temp	Environment	A	Power Supply #2 Temp

NOTE: The EST Numbers refer to the OLS EST numbering scheme, which agrees with the OLS EST numbering in the IS-YD-810A Interface Specification. The numbers in parenthesis, in the following descriptions, refer to the GE S/C channel assignment for each EST.

EST 1 (348) +28V S/C Inverter 1 EST

DC analog proportional to 0.142 of input. EST is voltage divider on the OLS side of the 28V fuse. The EST output for a 28V S/C input is 4.059 ± 5.6% volts. Applying tolerance gives a minimum output of 3.832 volts and a maximum output of 4.286 volts. The voltage is present when spacecraft power is applied.

EST 2 (349) +28V S/C Inverter 2 EST

Same as EST1.

EST 3 (350) +5 BB1 EST

The EST monitors the +5V output of the BB's own internal power converter. The signal reads +5V ± 10% when the power converter is activated by the power control signal and 0.0 ± 0.5 volts when it is disabled.

EST 4 (351) +5V BB2 EST

Same as EST 3.

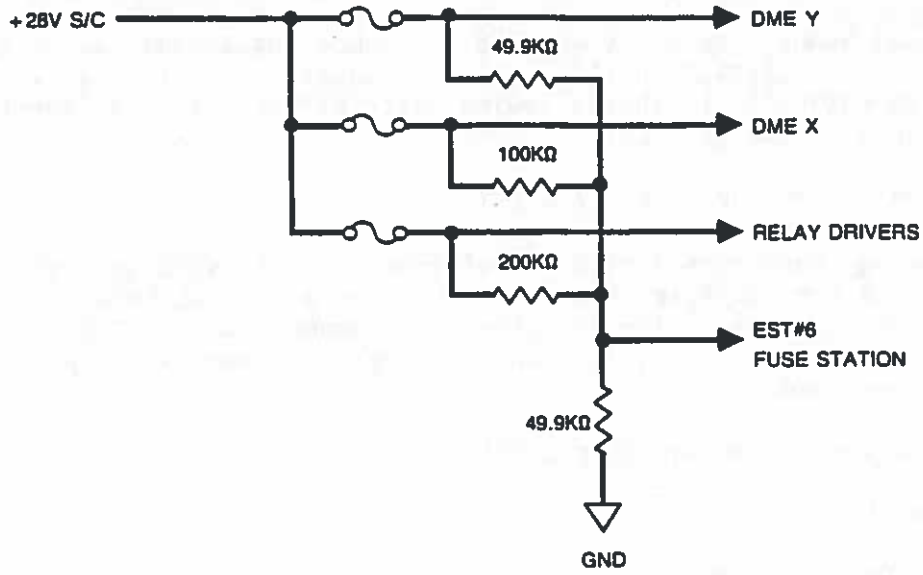
EST 5 (352) +5V BB3 EST

Same as EST 3.

EST 6 (353) +28V S/C Fuse EST

DC analog voltage which indicates the status of three sets of 28V fuses; 28V to the relay drivers, +28V to DME X and +28V to DME Y. Output levels are directly dependent on +28V S/C input supply voltage. Each level is ± 5%. The telemetry output voltages for various conditions are:

Nominal Output (no fuses blown)	+4.17V
Loss of Relay Drivers Fuse	+3.57V
Loss of DME X Fuse	+2.98V
Loss of DME X and Relay Drivers Fuses	+2.38V
Loss of DME Y Fuse	+1.78V
Loss of DME Y and Relay Drivers Fuses	+1.19V
Loss of DME X and DME Y Fuses	+0.59V
Loss of All three Fuses	0.0V



EST#6 +28V S/C FUSE EST

EST 7 (354) +5V S/C EST

DC analog voltage proportional to 0.50 of input S/C 5 volts. EST is divided directly from the S/C input in the PS. Nominal output is 2.50 volts. A ± 4% tolerance gives a range of 2.400 to 2.600 volts. The EST is present when spacecraft power is applied.

EST 8 (355) +5V S/C OSU X EST

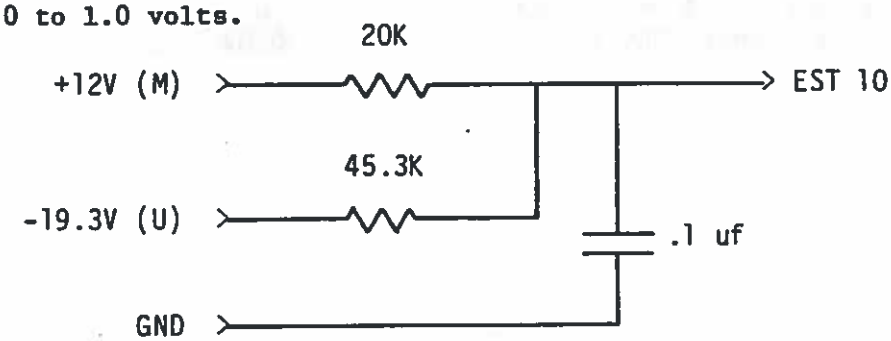
DC analog voltage proportional to 0.5 to input S/C 5 volts, less series current limiter. Nominal output is +2.485 volts for a 5.00 volt input. A ±5% tolerance gives an acceptable output range of 2.361 to 2.609 volts.

EST 9 (356) +5V S/C OSU Y EST

Same as EST 8 for OSU X.

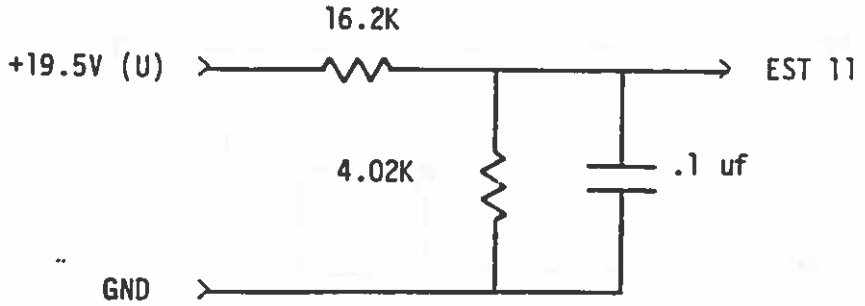
EST 10 (357) -19.3V (U) EST

DC analog proportional to the difference between -19.3V (U) and +12V (M). The nominal output is +2.322 volts. Since the unregulated supply varies greatly as a function of load, a ±6% variation of the unregulated supply is acceptable. This gives an EST voltage range of +1.961 to +2.686 volts. This voltage is present when OLS power enable is on. The off value is -1.0 to 1.0 volts.



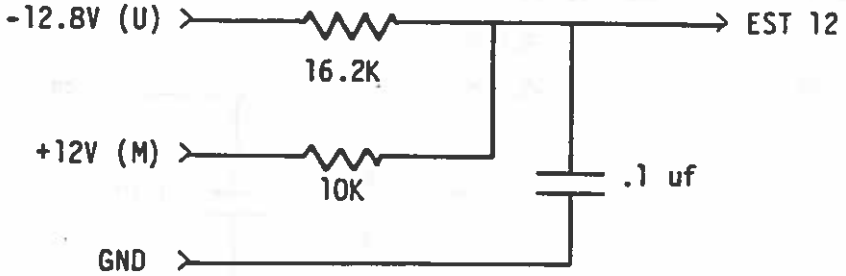
EST 11 (358) +19.5V (U) EST

DC analog proportional to 0.199 of the EST input. The nominal output is 3.877 volts. A ±6% variation of the unregulated voltage gives an acceptable range of 3.644 to 4.109 volts. This voltage is present when OLS power enable is on. The off value is -1.0 to 0.25 volts.



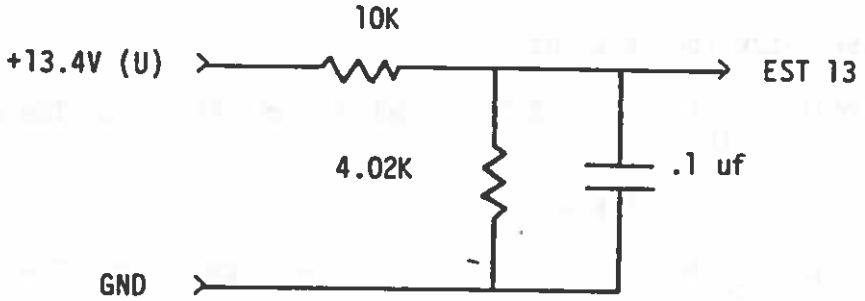
EST 12 (359) -12.8V (U) EST

DC analog proportional to the difference between -12.8V (U) and +12V (M). The nominal output is +2.324. A ±6% tolerance of the unregulated voltage gives an acceptable EST variation of +2.019 to +2.630 volts. This voltage is present when either PS is on. The off value is -1.0 to 1.0 volts.



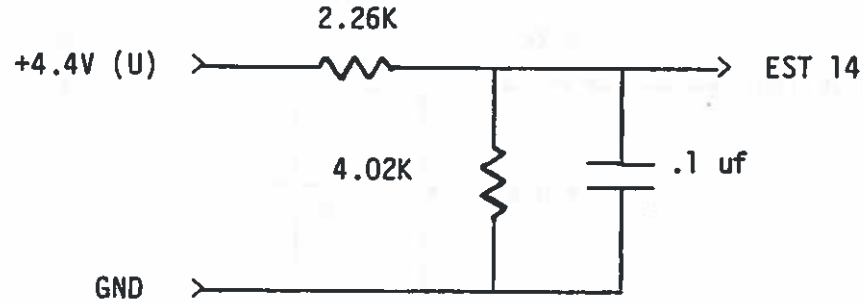
EST 13 (360) +13.4V (U) EST

DC analog proportional to 0.287 of the EST input. The nominal output is +3.842 volts. A ±6% tolerance gives an acceptable EST variation of +3.611 to +4.073 volts. This voltage is present when either PS in on. The off value is -1.0 to 0.25 volts.



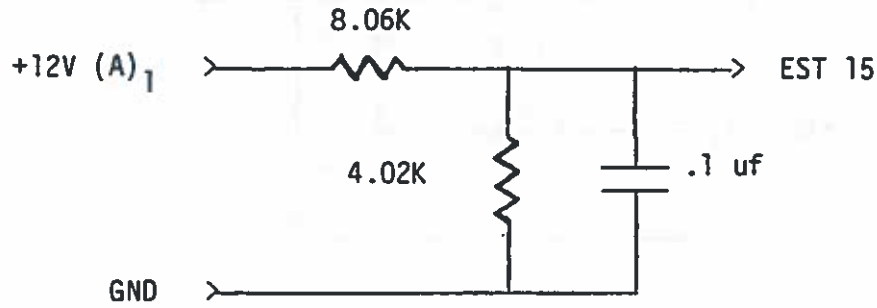
EST 14 (361) +4.4V (U) EST

DC analog proportional to 0.640 of the EST input. The nominal output is +2.880 volts. A +6% tolerance gives an acceptable EST variation of +2.708 to +3.053 volts. This voltage is present when either PS is on. The off value is -1.0 to 0.25 volts.



EST 15 (362) +12V (A)1 Reg EST

DC analog proportional to .333 of the regulator output. The input is 3.993 volts. A ±2% EST tolerance gives an acceptable variations of 3.913 to 4.073 volts. Valid when PS1 is on. The off value is -1.0 to 1.5 volts. The "A" in parenthesis indicates an analog supply and the 1 subscript identifies a P.S. 1 regulator.



EST 16 (363) +12V (A)2 Reg EST

Same circuit for P.S. 2 as EST 15. Valid when PS2 is on. The value is -1.0 to 1.5 volts.

EST 17 (364) +12V (D)1 Reg EST

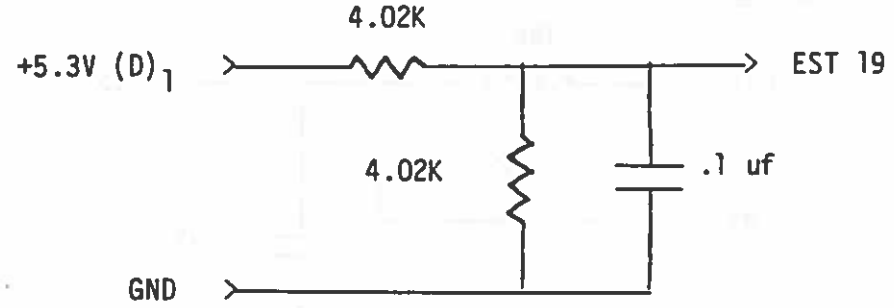
Same circuit for P.S. 1 as EST 15. Valid when PS1 is on. The off value is -1.0 to 1.9 volts.

EST 18 (365) +12V (D)2 Reg EST

Same circuit for P.S. 2 as EST 15. Valid when PS2 is on. The off value is -1.0 to 1.9 volts.

EST 19 (366) +5.3V (D)1 Reg EST

DC analog proportional to 0.5 of the regulator output. The nominal output is 2.650 volts. A ±2% EST tolerance gives an acceptable variation of 2.597 to 2.703 volts. Valid when PS1 is on. The off value is -1.0 to 1.2 volts.

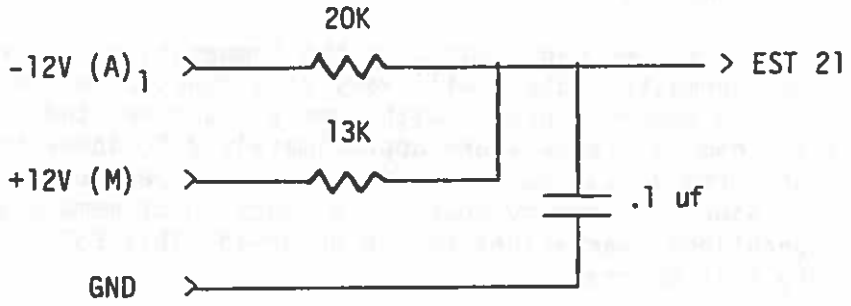


EST 20 (367) +5.3V (D)2 Reg EST

Same circuit for P.S. #2 as EST 19. Valid when PS2 is on. The off value is -1.0 to 1.2 volts.

EST 21 (368) -12V (A)1 Reg EST

DC analog proportional to the difference between the -12V (A) and +12V (M). The nominal output is 2.549 volts. A ±2% tolerance of the unregulated voltages gives an acceptable range of +2.451 to +2.640 volts. Valid when PS1 is on. The off value is -1.0 to 1.5 volts.



EST 22 (369) -12V (A)2 Reg EST

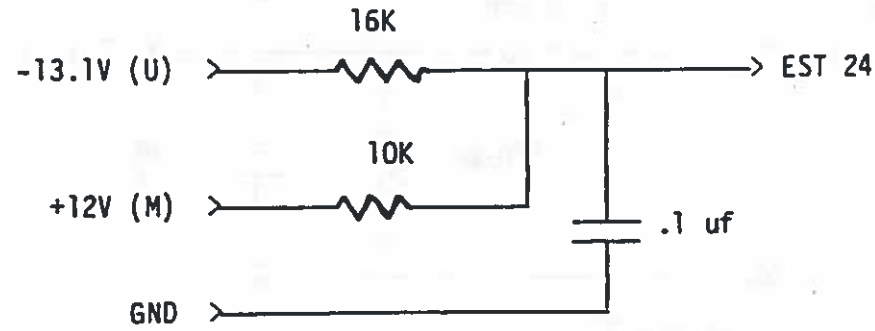
Same circuit for P.S. #2 as EST 21. Valid when PS2 is on. The off value is -1.0 to 1.5 volts.

EST 23 (370) +12V (M) Reg EST

Same circuit for +12V (M) as EST 15. Valid when either PS on. The off value is -1.0 to 0.5 volts.

EST 24 (371) -13.1V (U) To HVPS EST

DC analog proportional to the -13.1V (U) and +12V (M). The nominal output is +2.269 volts. A ±6% variance of the unregulated voltages gives an acceptable range of +1.962 to +2.576 volts. The EST is located on the HVPS side of a fuse set and should be present when either PS is on. The off value is -1.0 to 1.0 volts. A blown fuse will result in a full scale +5 volt saturation reading.



EST 25 (181) PSU Temp EST

DC analog voltage related nonlinearly to the temperature in the power supply section of the PSU. The thermistor is mounted on the chassis baseplate. The thermistor output will vary as a function of power supply configuration (i.e., PS1, PS2, or both activated) and PSU mount temperature. A nominal output is about 5°C warmer than the PSU mount. The curve of EST output vs thermistor temperature is shown in Figure 3.4.1-1. The EST is active when OLS power enable is on.

EST 26 (182) SPSE Temp EST

DC analog voltage related nonlinearly to the temperature of the "E" side core memory. The thermistor output will vary as a function of SPS mount temperature and core memory E power. With memory E active, the thermistor should indicate a nominal temperature approximately 25°C above the mount temperature. The curve of EST output vs thermistor temperature is shown in Figure 3.4.1-2. Since the memory power is a function of memory access rate, slight operational variations may be observed. This EST is valid only when Memory E is powered.

EST 27 (183) SPU Temp EST

DC analog voltage related nonlinearly to the temperature of the SPU. Since the SPU is a low power unit the SPU board temperature varies primarily as a function of mount temperature. The nominal thermistor reading is approximately 10°C to 15°C above the SPU mount. The curve of EST output vs thermistor temperature is shown in Figure 3.4.1-1. The EST is active when OLS power enable is ON.

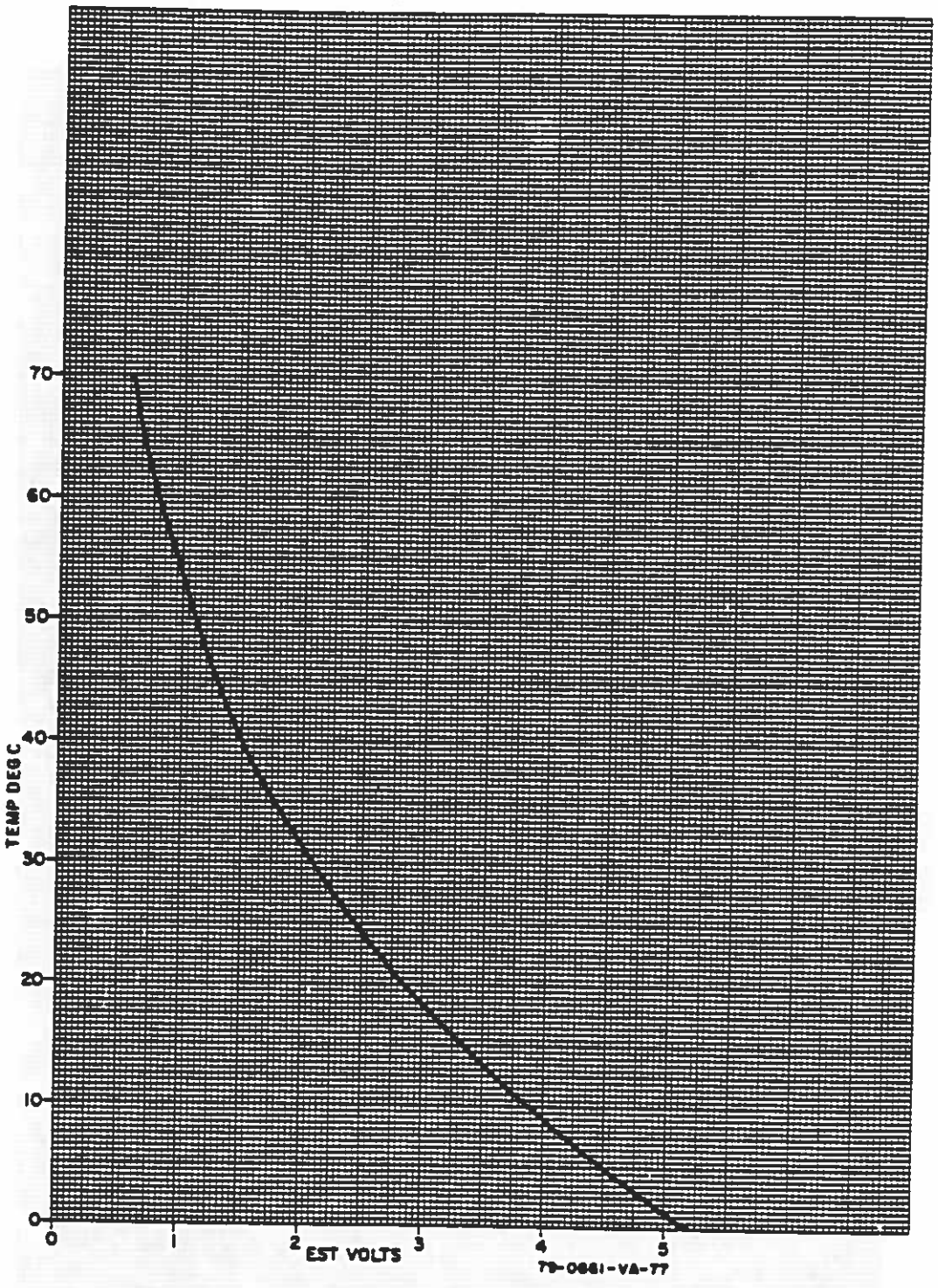


Figure 3.4.1-1. EST 25 PSU Temp EST
EST 27 SPU Temp EST

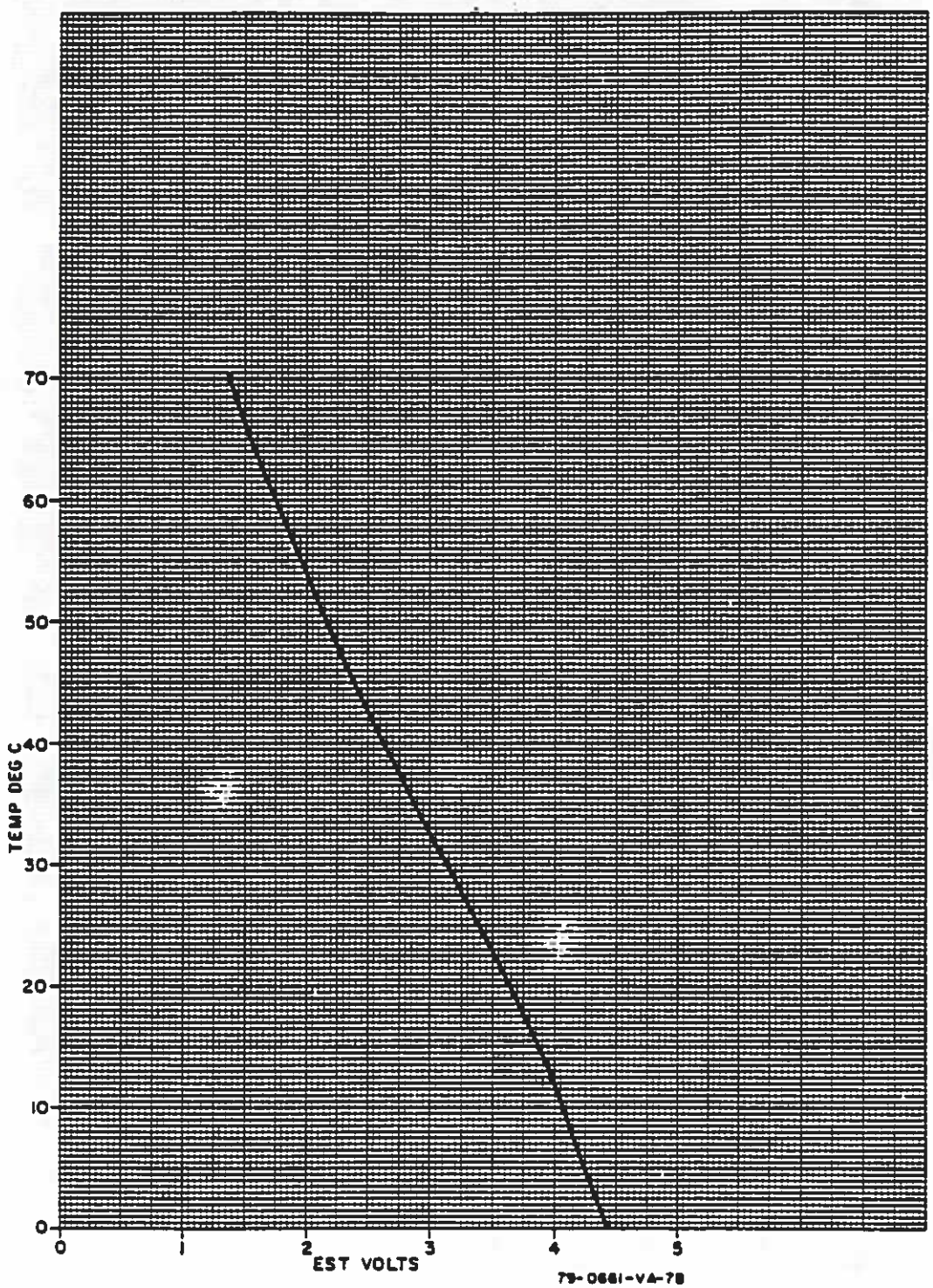


Figure 3.4.1-2. EST 26 SPSE Temp EST
EST 75 SPSF Temp EST

EST 28 (185) -Y SSS Temp EST

This EST monitors the SSS temperature at the -Y end. The EST signal has the calibration table given below. The normal operating range is ±5°C around the SSS temperature set point which is +5°. Thus, the expected maximum range of 0° to +10°C gives 3.6 to 2.4 volts EST signal when operating in the space environment. The room temperature EST should be approximately 1.6 to 1.3 volts out.

T, DEG. C	V-DC
-10	5.005
- 8	4.693
- 6	4.391
- 4	4.102
- 2	3.826
0	3.563
2	3.314
4	3.079
6	2.858
8	2.65
10	2.456
12	2.275
14	2.106
16	1.949
18	1.804
20	1.669
22	1.544
24	1.429
26	1.322
28	1.223
30	1.132
32	1.048
34	.9708
36	.8995
38	.8341
40	.7733

The curve of EST output vs temperature is shown in Figure 3.4.1-3.

EST 29 (186) +Y SSS Temp EST

This EST is the same as EST 28 except that it monitors the temperature of the +Y end of the SSS. Both ESTs are active when OLS power enable is on.

EST 30 (187) Relay Optics Temp EST

This EST signal has the same calibration curve as EST 28. The normal operating range is ±5°C around the SSS temperature set point which is 5°. Thus, the expected maximum range of 0° to +10°C gives 3.6 to 2.4 volts EST signal when operating in the space environment. The room temperature EST should be approximately 1.6 to 1.3 volts out.

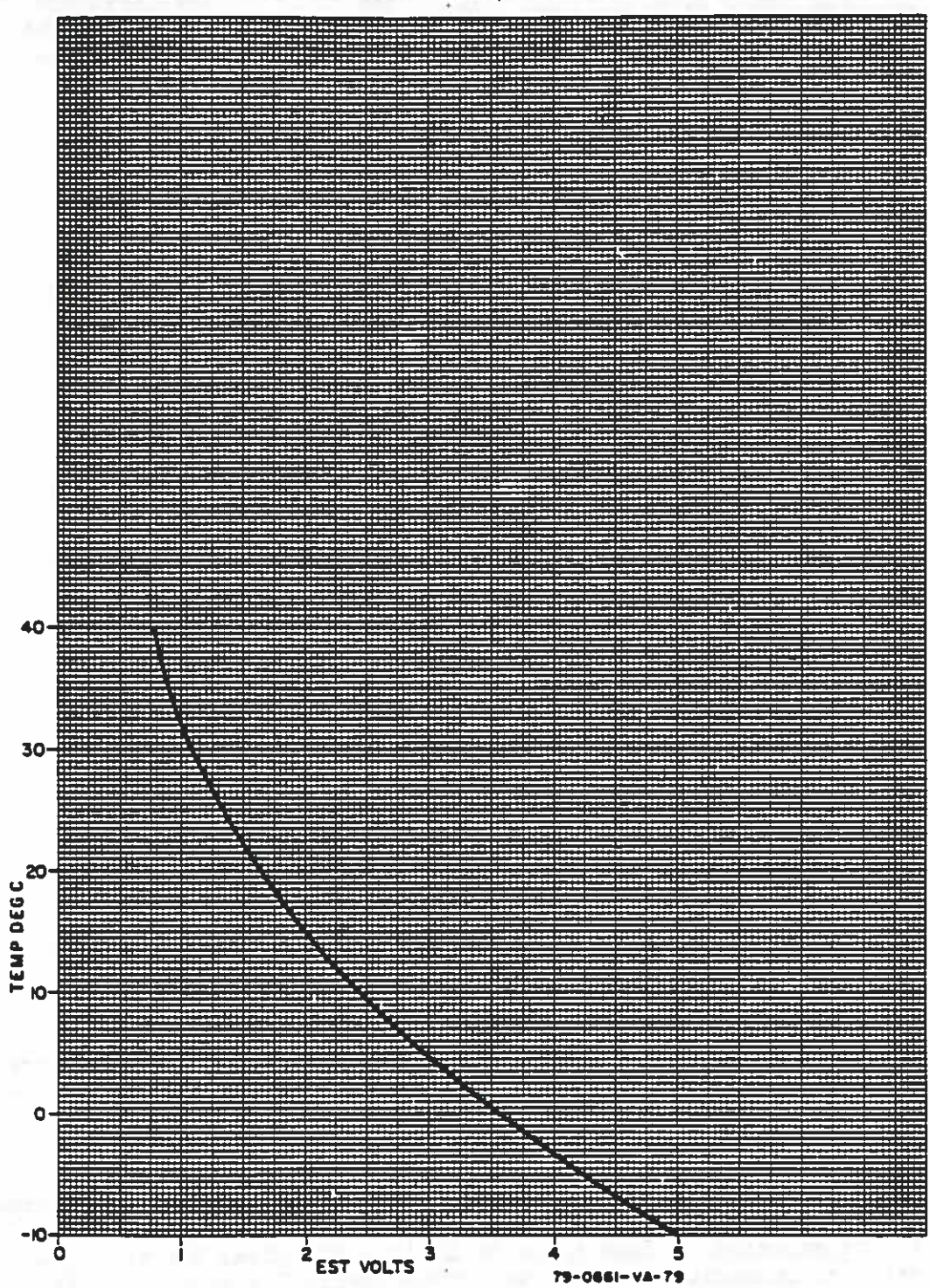


Figure 3.4.1-3. EST 28 -Y SSS Temp EST
EST 29 +Y SSS Temp EST
EST 30 Relay Optics Temp EST

EST 31 (188) M1 Temp EST

This EST monitors the first mirror temperature. The voltage versus temperature calibration is listed below.

The expected temperature varies with orbit angle and shade configurations, so an all encompassing normal temperature range is approximately -8° to +12°C. Therefore, the operating EST signal range is about 3.1 to 1.4 volts with about 0.8 volt at room temperature. The curve of output vs temperature is shown in Figure 3.4.1-4.

T, DEG. C	Output (V)
-20	4.883
-18	4.553
-16	4.238
-14	3.937
-12	3.651
-10	3.381
- 8	3.127
- 6	2.889
- 4	2.667
- 2	2.461
0	2.268
2	2.091
4	1.926
6	1.775
8	1.635
10	1.507
12	1.389
14	1.281
16	1.182
18	1.091
20	1.008
22	0.932
24	0.862
26	0.798
28	0.739
30	0.686

EST 32 (187) T Patch Temp EST (This EST is system unique)

This EST signal measures the temperature of the (inner stage) cold patch of the T channel Cone Cooler.

Typical operating temperature variation is very small, due to the active closed-loop control. Nominal range of the set point is approximately 103° to 113°K, so the output EST voltage equivalent is 1.9 to 3.6 volts dc typical. At room temperature the signal is nearly zero volts.

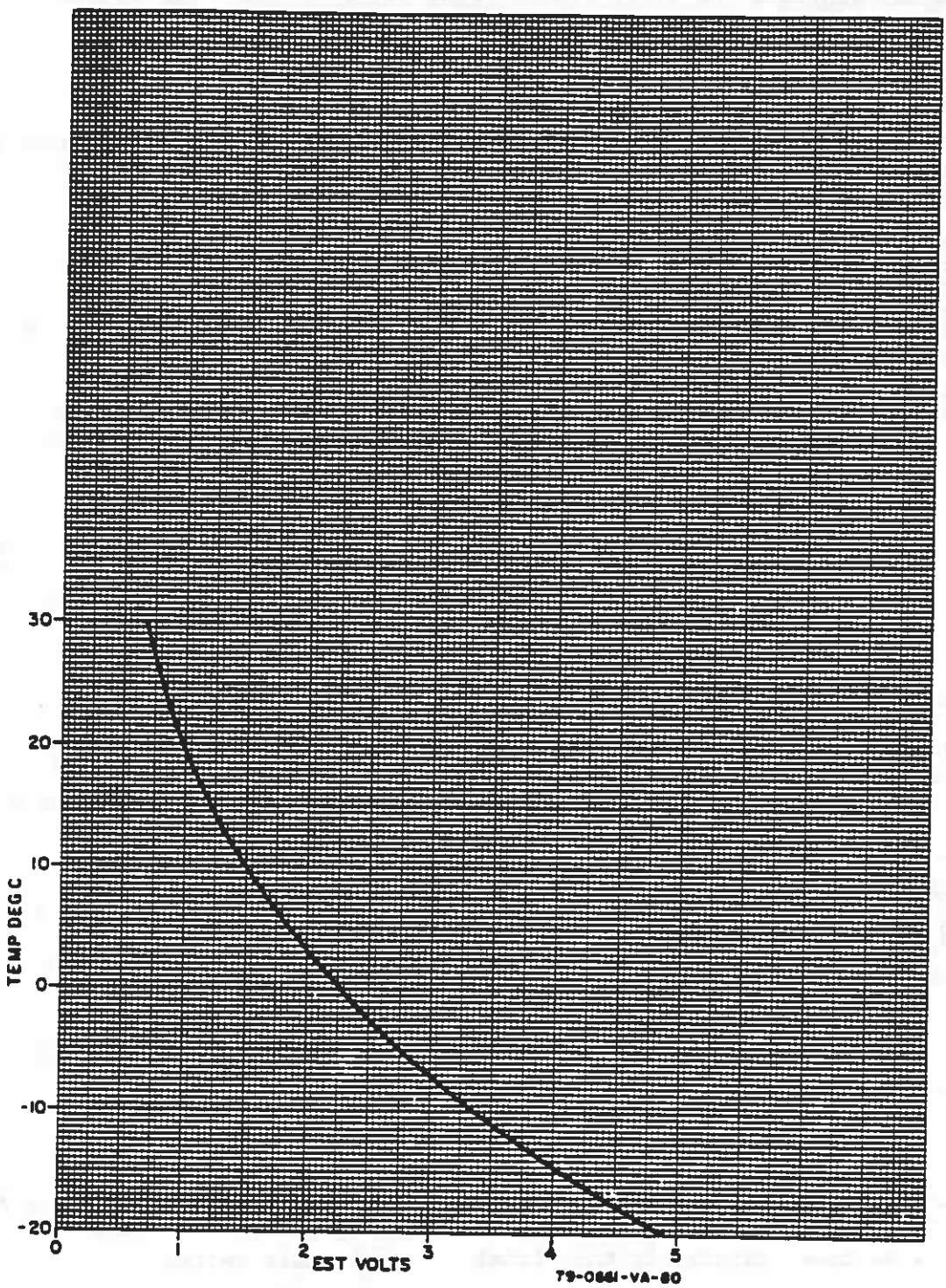


Figure 3.4.1-4. EST 31 M1 Temp EST

The temperature calibration relationship for a typical unit is given in the following table. This is the only temperature EST for which an individual calibration table for each serial number system is required, due to the variability in thermistors for this cryogenic region and the interest in good accuracy for the T Cold Patch Temperature. The actual calibrations will be included in the Acceptance Test Reports for individual OLS/AVE units.

The thermistor used to measure this EST is the same one used for temperature control of the T detector. The signal V1 is located and amplified to give the PATCH EST voltage. A typical curve of T Patch Temp EST output vs temperature is shown in Figure 3.4.1-5.

T (DEG K)	THERM. R	V1	PATCH EST, TYPICAL
95	6699	1.128	6.249
96	6194	1.051	5.822
97	5735	.9799	5.427
98	5315	.9141	5.063
99	4932	.8533	4.726
100	4581	.7971	4.415
101	4256	.7444	4.123
102	3963	.6965	3.858
103	3690	.6516	3.609
104	3440	.61	3.379
105	3210	.5616	3.166
106	3996	.5356	2.967
107	2802	.5029	2.785
108	2621	.4721	2.615
109	2455	.4436	2.457
110	2299	.4168	2.308
111	2155	.392	2.171
112	2023	.3691	2.044
113	1901	.3479	1.927
114	1786	.3279	1.816
115	1679	.309	1.711
116	1581	.2918	1.616
117	1489	.2756	1.527
118	1403	.2604	1.442
119	1323	.2462	1.363
120	1249	.233	1.291
121	1179	.2206	1.222
122	1114	.2091	1.158
123	1053	.1982	1.097
124	996.6	.188	1.041
125	943	.1784	.9881
126	893.3	.1695	.9387
127	846.3	.161	.8919
128	802.6	.1532	.8483
129	761.2	.1457	.807
130	722.8	.1388	.7686

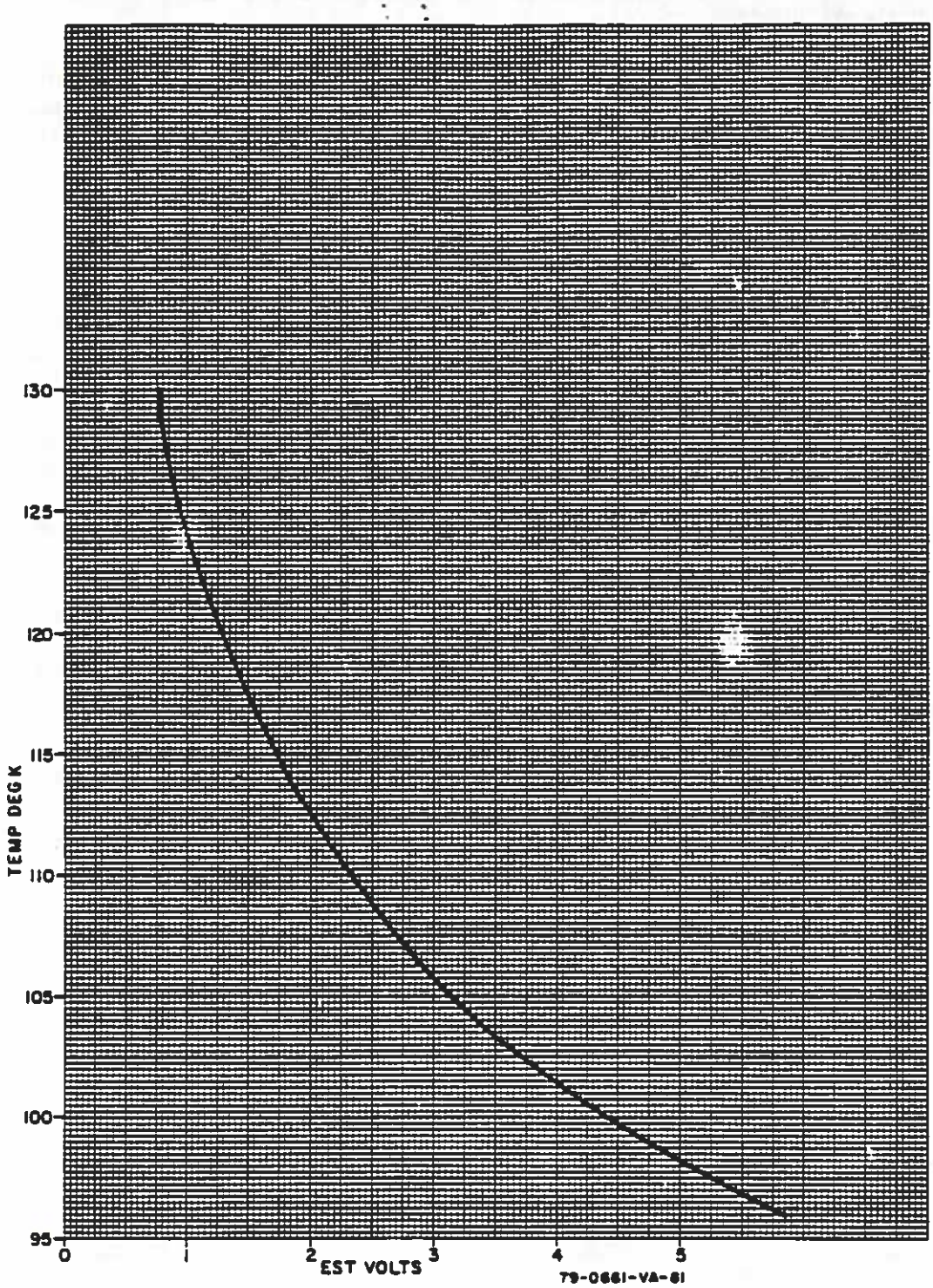


Figure 3.4.1-5. EST 32 T Patch Temp EST (Typical)

EST 33 (190) T Cone Temp EST

This EST measures the temperature of the cone cooler outer stage. The normal range of temperatures when operating is approximately 170° to 200° Kelvin.

The calibration table listed below gives the EST voltage versus temperature relationship; this table will serve for all coolers, as the precision thermistors are interchangeable.

The normal T Cone Temp EST range is approximately 3.8 to 4.9 volts, when cooled, and is approximately 0.16 volts when at room temperature. The curve of EST output vs temperature is shown in Figure 3.4.1-6.

TEMP (DEG K)	THERMISTOR RESISTANCE	EST VOLTAGE
170	4.0411E+5	4.741
175	2.6388E+5	4.678
180	1.7446E+5	4.587
185	1.1703E+5	4.462
190	79653	4.295
196	51227	4.033
200	38619	3.819
206	25692	3.447
210	19802	3.172
216	13608	2.739
220	10693	2.447
226	7559.6	2.030
230	6052	1.773
235	4622.7	1.483
240	3565.3	1.231
245	2774.6	1.016
250	2177.2	0.836
255	1722.7	0.687
260	1372.5	0.565
265	1101	0.4653
270	889.41	0.384
275	722.44	0.318
280	590.47	0.265
285	485.29	0.221
290	400.77	0.185
295	332.58	0.156
300	277.14	0.132
305	232.06	0.112

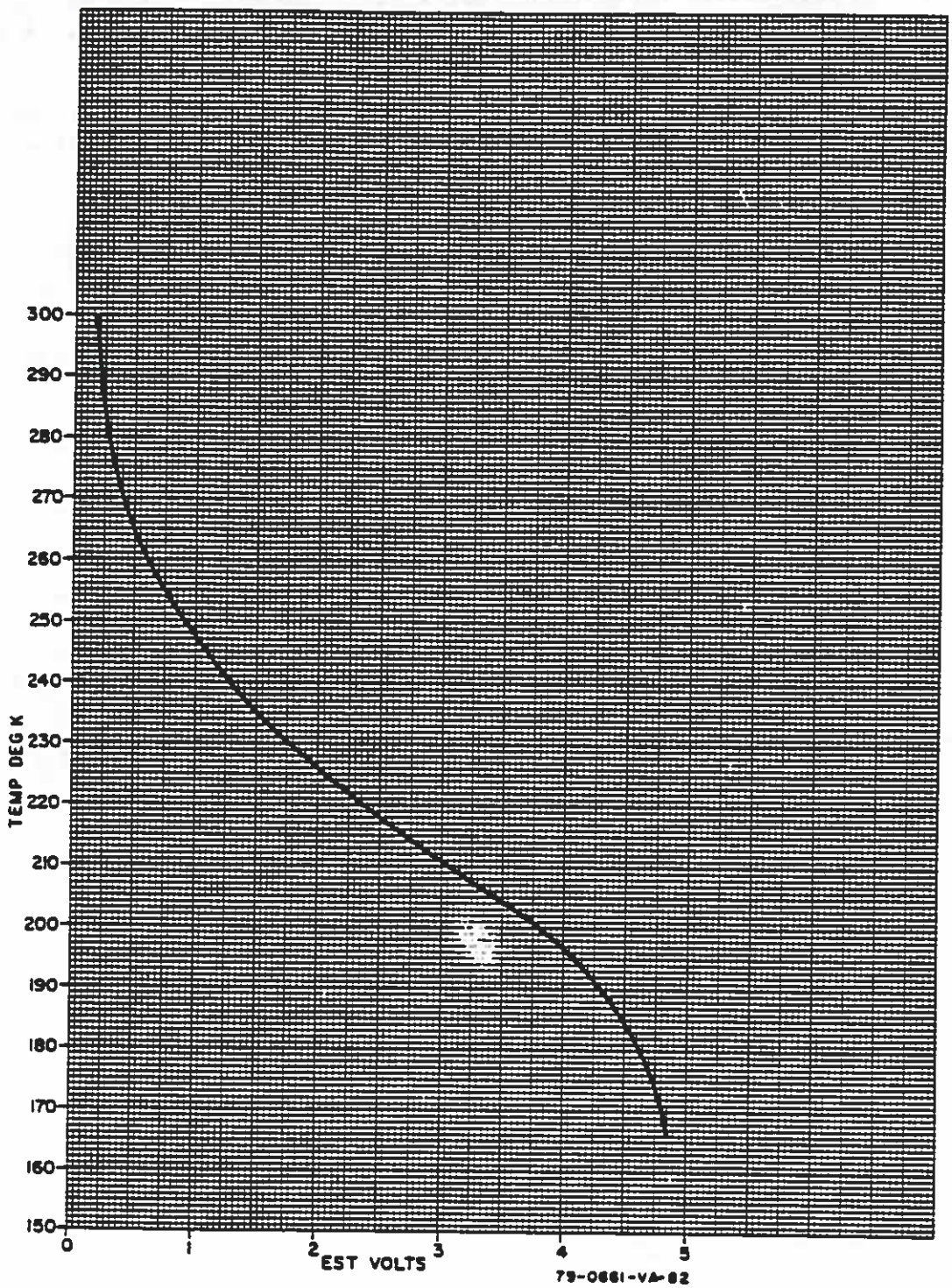


Figure 3.4.1-6. EST 33 T Cone Temp EST

EST 34 (191) T Clamp EST

This EST monitors the T Clamp cold reference blackbody temperature. This reference must stay in the 240° ±12°K range, or −45°C minimum to −21°C maximum for the T channel to operate properly The voltage versus temperature relationship is listed below. The normal operating range of this EST signal is 4.20 to 1.60 volts. The room temperature output should be approximately 0.32 to 0.24 volts out. The curve at EST output vs temperature is shown in Figure 3.4.1-7.

T, DEG. C	EST
-50	5.025
-48	4.69
-46	4 367
-44	4.058
-42	3.764
-40	3.486
-38	3.224
-36	2.976
-34	2.746
-32	2.531
-30	2.331
-28	2 146
-26	1.975
-24	1.816
-22	1.67
-20	1.536
-18	1.412
-16	1.299
-14	1.195
-12	1.099
-10	1.012
- 8	.9316
- 6	.8581
- 4	.7908
- 2	.7292
0	.6729
2	.6209
4	.5734
6	.53
8	.4899
10	.4535
12	.4198
14	.3891
16	.3607
18	.3348
20	.3107
22	.2888
24	.2686
26	.2499

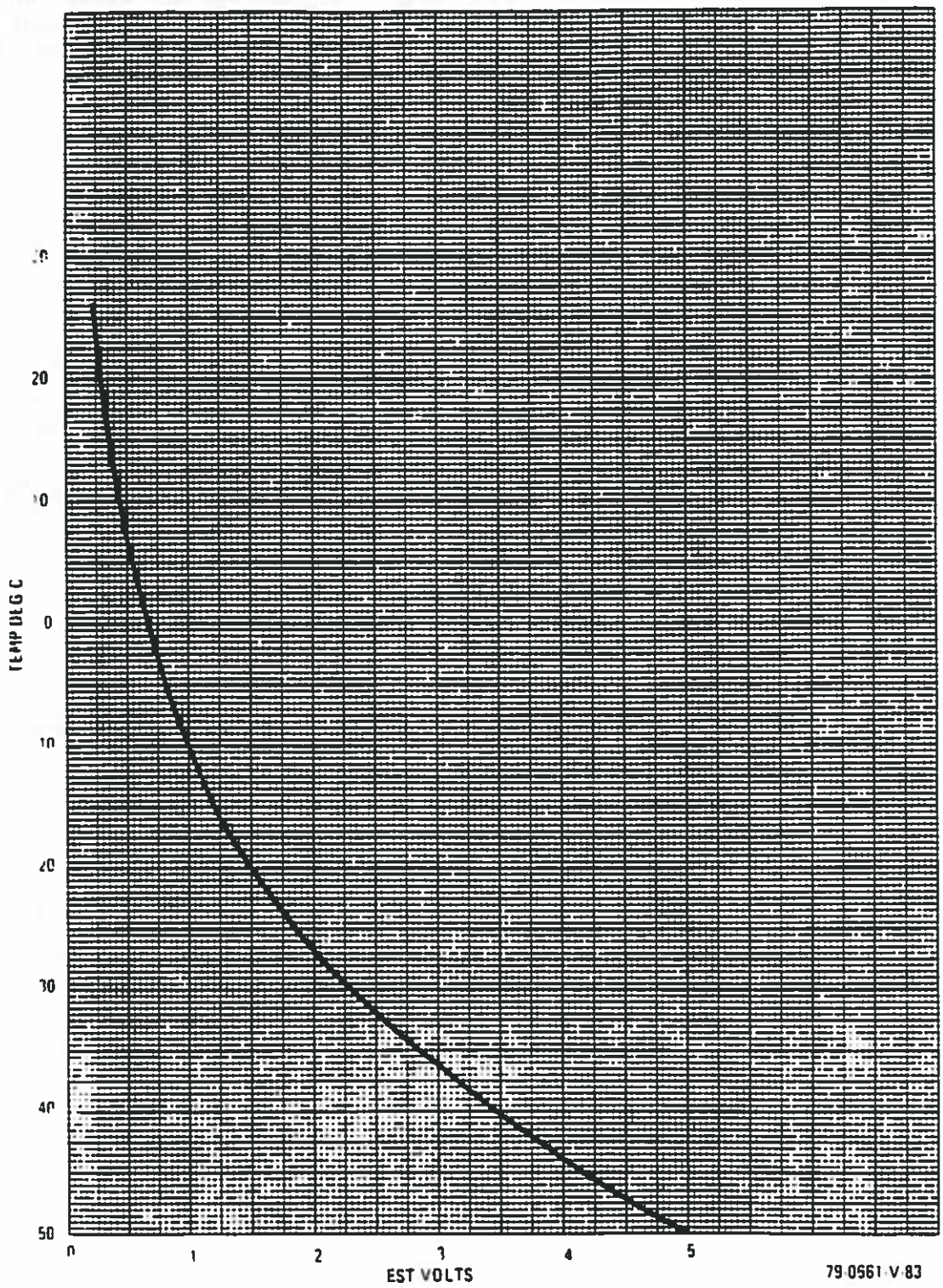


Figure 3.4.1-7. EST 34 T Clamp Temp EST

EST 35 (193) T Cal Temp EST

The EST monitors the temperature of the T calibration cavity viewed during +Z overscan by the T detector. The nominal operating range is + 5 C around the SSS temperature set point, which is +5°C. The expected maximum range of 0°C to +10°C gives 3.6 to 2.4 volts EST signal. The calibration of this EST is given below. The curve of EST vs temperature is shown in Figure 3.4.1-8.

T, DEG. C	V DC
-10	5.005
- 8	4.693
- 6	4.391
- 4	4.102
- 2	3.826
0	3.563
2	3.314
4	3.079
6	2.858
8	2.65
10	2.456
12	2.275
14	2.106
16	1.949
18	1.804
20	1.669
22	1 544
24	1.429
26	1.322
28	1.223
30	1.132
32	1.048
34	.9708
36	.8995
38	.8341
40	.7733

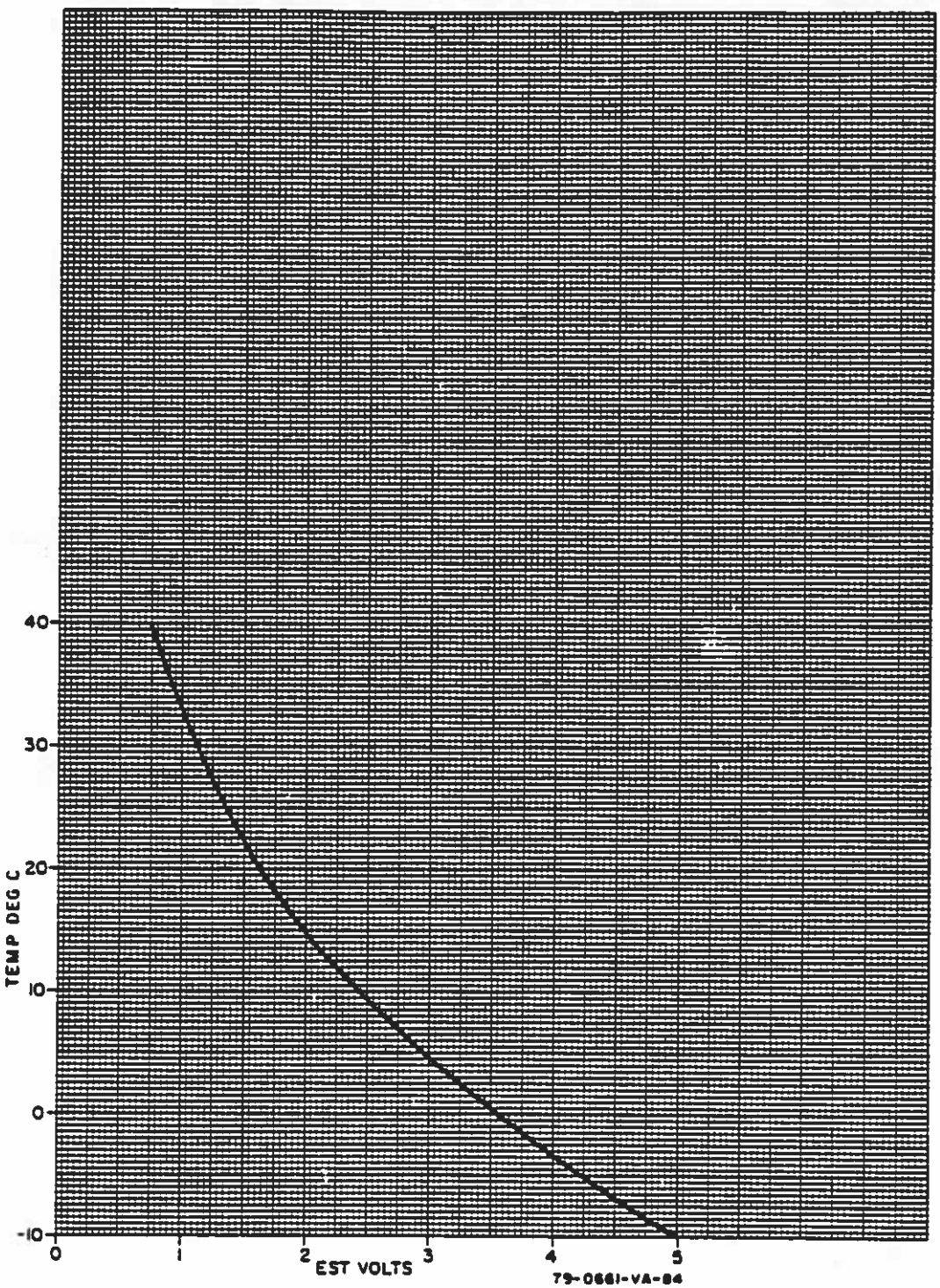


Figure 3.4.1-8. EST 35 T CAL Temp EST

EST 36 (194) T Cal/Clamp EST

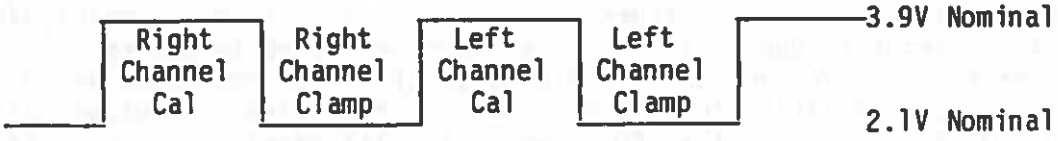
The multiplexed T Cal and T Clamp may be used to determine changes in T channel performance and to aid in "in-flight" calibration or failure analysis.

A standard sample and hold circuit is connected to the T analog filter output. This single circuit over a two scan cycle period sequentially samples during the end of scan time and holds, for approximately a half-scan line the following:

The left channel clamp output signal
The right channel calibration signal
The right channel clamp signal
The left channel calibration signal

This results in a square wave at 5.94 Hz. The T clamp temperature is typically 240°K, so this nominal EST level is 2.1 Vdc. T Cal temperature is typically 278°K, so this nominal EST level is 3.7 Vdc. The scale factor for this EST for 5D-3 is 41.7 mV/K. It is necessary to perform a single point dwell on this EST in order to have enough bandwidth to read out the channel.

This signal is presented as the following square wave:



At ambient, both T cal and T clamp are the same temperature and the T detector has very small response so the EST output will be a level of 1 to 4 volts.

EST 37 (195) T Cal/Clamp Backup EST

Same as EST 36 for the T backup filter output.

EST 38 (196) T Patch HTR EST

This EST voltage is a function of the power of the inner stage (patch) heater of the T Cone Cooler from the temperature control loop. The heater voltage is:

$V_{Htr} = 2\ V_T$ PATCH HTR -0.6 (volts dc)

The T Patch Heater power is:

$(V_{HTR})^2/2170$ (Watts).

The plot of T Patch Heater Power versus telemetry voltage is shown in Figure 3.4.1-9.

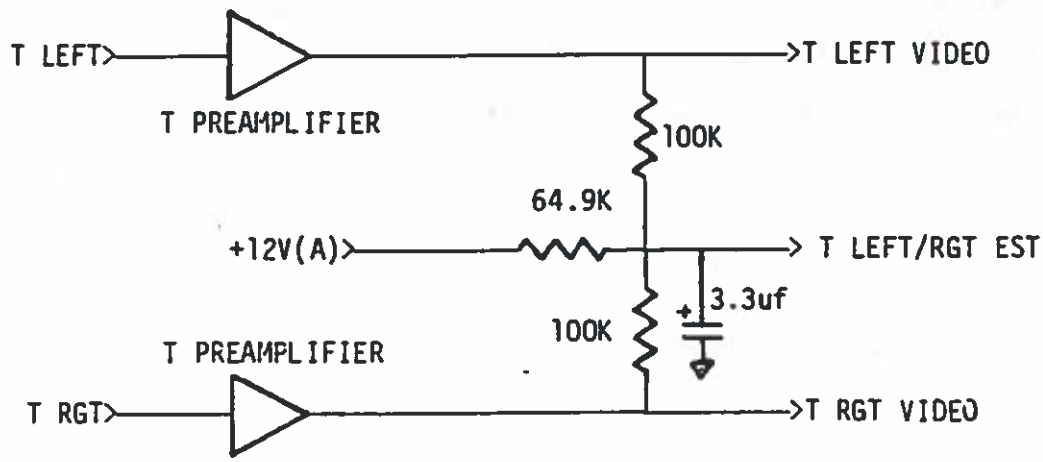
The normal range of this signal is approximately 2 to 4.5 volts dc when the T-Channel is cooled. At room temperature the normal voltage is zero volts.

EST 39 (197) T Left/T Right EST

The T Left/Right EST is used to troubleshoot or isolate possible problems with the T channel preamplifiers.

This telemetry channel monitors the dc operating levels of the left and right "T" channel preamplifiers. The nominal preamplifier outputs of -5.3 Vdc are coupled through a resistor divider which effectively sums the two signals and level shifts the nominal outputs to a voltage of +2.2 Vdc. Anticipated preamplifier variances due to time, temperature or system to system differences are ±1.0 Vdc and the dynamic range of linear operation is -5.3 ±2.5 Vdc. If one amplifier output shifts ±1 Vdc the telemetry output will shift ±0.282 Vdc. Note that this EST channel is also sensitive to +12V (A) variation since that is the bias supply.

The acceptable EST range for normal preamp operation is 0.16 to 4.64 Vdc. At ambient or with the scanner off the EST will be a level between 1.6 and 2.8 Vdc.



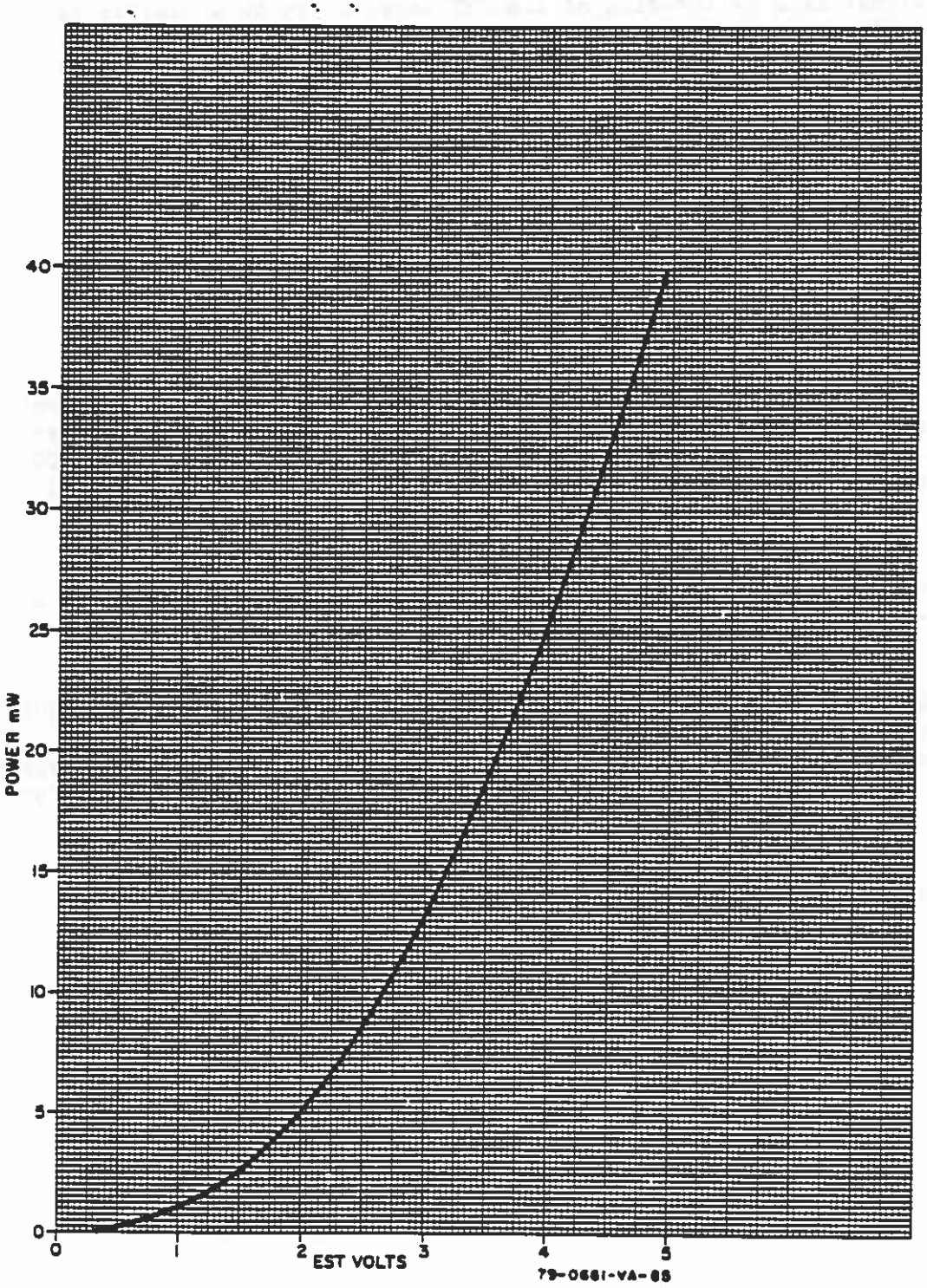
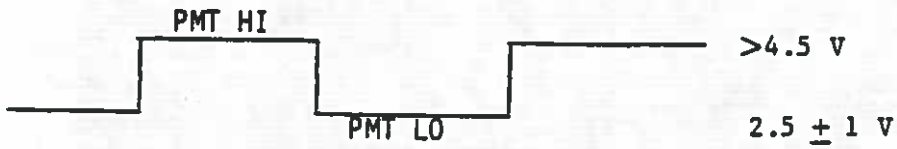


Figure 3.4.1-9. EST 38 T Patch HTR EST

EST 40 (198) PMT CAL EST

This signal is a calibration of the PMT sensitivity to a visible red (660 nm wavelength) light pulse from a calibration source LED. It is sampled on alternate scan lines in PMT HI gain and PMT LO gain during the (-)Z ends of scan, resulting in the square wave shown. The frequency = 2.97 Hz.



The PMT CAL V EST is taken only if the PMT is to be used on the upcoming scan. Samples are taken after a 5.09 kHz single pole lowpass noise filter so the Noise Bandwidth is the same as the actual 8 kHz LS PMT channel. A VDGA gain command word for the PMT CAL gain value, different for each OLS, is stored in constants memory.

The average value of the EST output for PMT LO Gain is 2.5 Vdc with an acceptable range of 1.9 to 3.1 volts dc.

The EST is meaningful only when the PMT high voltage is on and the PMT use mode is selected. If the PMT is off the EST output is indeterminate. Calibrations are also only valid on the dark side of an orbit and with scenes of less than full moon, as there is no mechanical optical path shutter for the PMT field of view to adequately darken this sensitive detector.

EST 41 (199) PMT CAL Backup EST

This EST monitors the PMT performance through the redundant VDGA and filters. The EST description is identical with EST 40.

EST 42 (201) VCO Error EST

This is an analog signal proportional to the voltage on the varactor in the voltage controlled oscillator (VCXO) circuit. The VCXO circuit is used in a phase lock loop that generates the 40/39 tape recorder gapper clock.

If the phase lock loop fails to acquire lock the loop would drive the varactor voltage to an upper or lower limit. Loop failure in the upper stop would yield an EST voltage of approximately 4.5 Vdc (+11.3 Vdc on the varactor). Lower stop failure yields an EST voltage of approximately 0.78 Vdc (-11.3 Vdc on the varactor).

The VCO EST output may vary from unit to unit between 1.2 and 2.9 volts. The variance of a particular unit around its nominal should be less than $\pm$ 0.5 volts.

EST 43 (376) DME A Current EST

This telemetry channel monitors the average dc motor current, smoothed over several full scan cycles. A 1.82 ohm current sampling resistor and a low-pass filter amplifier stage having a gain of 4.016 provides the output for this EST. The scale factor is 0.1368 amp/volt EST.

A limiter circuit in the DME prevents the drive pulse width from exceeding 29 msec for vacuum, so the typical maximum EST voltage is 0.92 volts (vacuum). The limiter is switched by command to be 59 msec maximum pulse width for air, so the typical maximum EST voltage is 1.92 volts (air).

The nominal EST voltages expected are 300 to 550 mV for vacuum and 0.8 to 1.3 volts for air.

This EST is valid only when DME A is selected and scan enable A is commanded. The OFF state is 0 $\pm$ 0.1 volts.

EST 44 (377) DME B Current EST

Same as EST 43 for DME B. This EST is valid when DME B is selected and scan enable B is commanded.

EST 45 (202) SENSEL

Describes selected sensor per the following:

EST Voltage	HRD SEL	PMT SEL	PMT 1/9	PMT PGS	Sensor Selected	Voltage Limits
+3.33V	1	0	0	0	PMT 1/9	3.180 to 3.480
+5V	1	0	0	1	Not Used	
+1.66V	1	0	1	0	PMT LO	1.510 to 1.810
0V	1	0	1	1	PMT HI	-.150 to +.150
+5V	0	1	X	X	HRD	4.850 to 5.150

The SENSELEST is derived from an output word from the SPS processor. The tolerance for all readings is nominal output ± 150 mV. This EST is accurate only when the processor is active.

EST 46 (203) DOC SQB EST

Monitors deployable optics cover fusible link actuators.

Fusible Link Actuated	EST Volts
None	0
S1 Only	2.51
S2 Only	0.90
S1 & S2	3.76

NOTE: The cover has two actuators, S1 and S2.

This EST is accurate only when the actuators or the actuator simulator box is installed.

EST 47 (204) DCC SQB EST

Monitors cone cooler cover fusible link actuators.

Fusible Link Actuated	EST Volts
None	0
S1 Only	2.51
S2 Only	0.90
S1 & S2	3.76

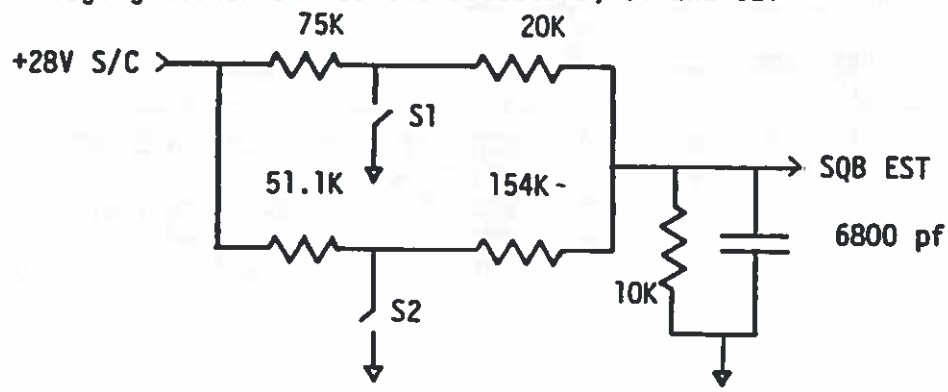
NOTE: The cover has two actuators, S1 and S2.

EST 48 (205) SCNR Cage SQB EST

Monitors scanner caging mechanism release fusible link actuators.

Fusible Link Actuated	EST Volts
None	0
S1 Only	2.51
S2 Only	0.90
S1 & S2	3.76

NOTE: The caging mechanism has two actuators, S1 and S2.



EST 49 (206) PMT HV EST (This EST is system unique)

A Telemetry voltage of 0 Vdc corresponds to a supply voltage of -1292 Vdc, and +5V reading indicates a supply voltage of -766.4 Vdc. The sensitivity of the signal is 9.52 mV/V. The nominal supply voltage is -1050 Vdc yielding a telemetry output of 2.30 Vdc. This voltage will vary from system to system as a function of the desired element voltages required for each PMT. The system to system nominal may vary from 1.5 to 4.0 Vdc, but EST variance for any one system should not exceed + 250 mV. If the HVPS is OFF, the telemetry channel output will be approximately +5.6 Vdc, yielding a full-scale EST output voltage.

EST 50 (209) PR1 RDY EST

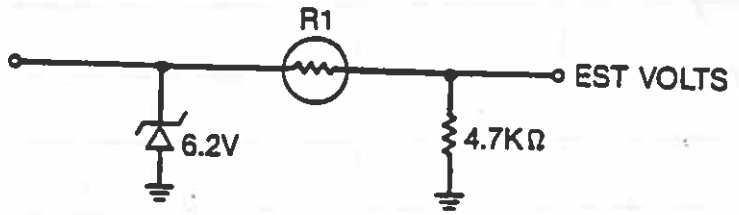
A +3.0 to +5.0V indicates recorder up to speed and ready to accept or output data. Signal shall be stable within 5 sec after power enable signal goes high and a proper operating mode has been selected. A 0.2 to +-/2V indicates either:

(a) Power enable not sent to recorder.
(b) If power enable has been sent, recorder is not running. May be due to incorrect command relative to tape position; i.e., record command when already at end of tape.
(c) Degapper buffer not locked to playback data (in playback modes only).

The signal is derived from a voltage divider on the telemetry board of the tape recorder.

EST 51 (21) PR1 Temp EST

A dc analog voltage proportional to the temperature at the recorder head-to-tape interface. The thermistor is physically located in close proximity to the head assembly and is thus associated with the temperature of the heads. The temperature vs EST voltage is shown in figure 3.4.1-10. This curve is for nominal values and will vary as a function of Zener voltage and component tolerances. There is a ±5% tolerance on the Zener voltage and ±3% on the thermistor.



$$V_{EST} = V_Z \frac{4.7K/\Omega}{R1 + 4.7K\Omega}$$

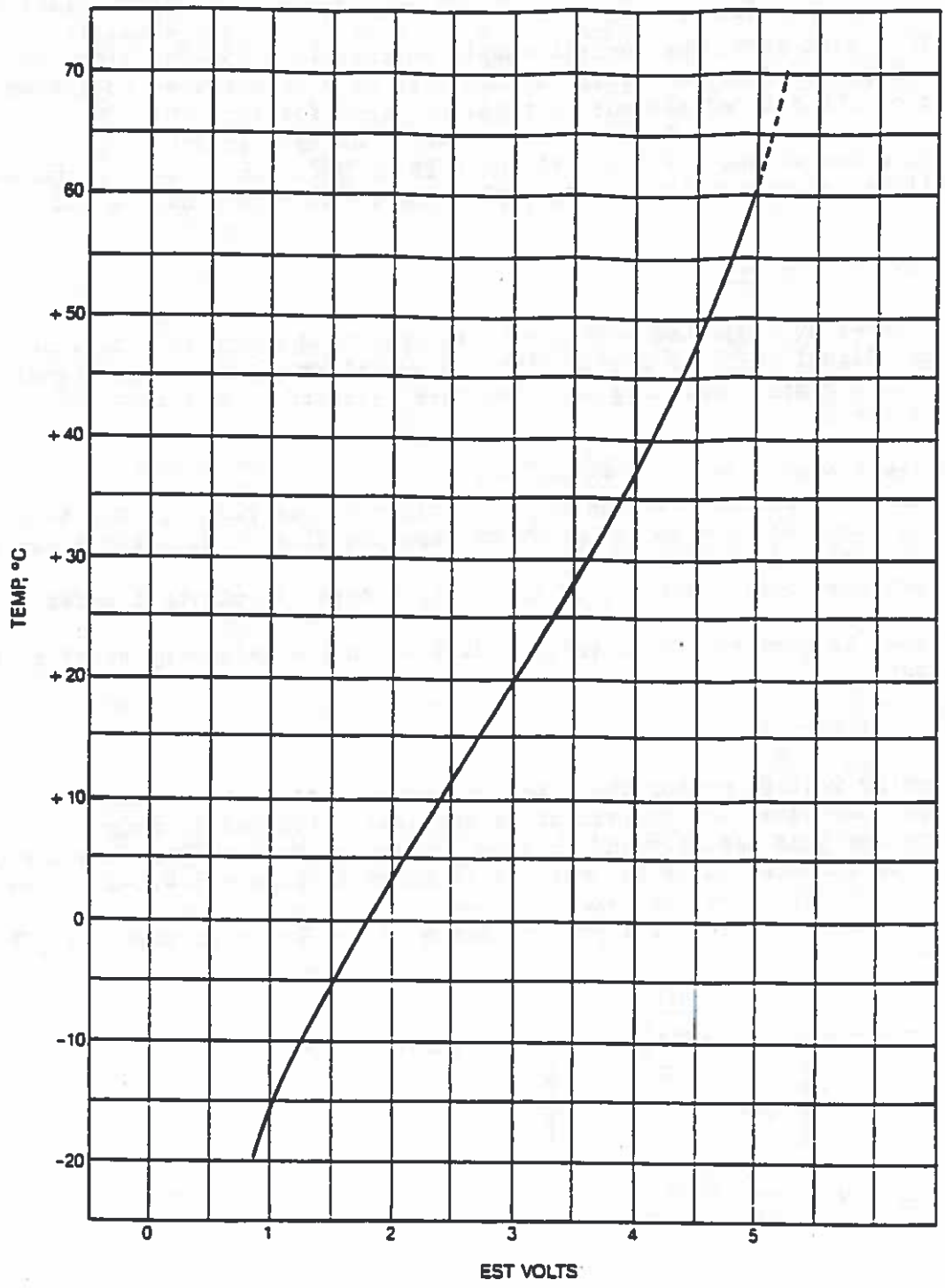


Figure 3.4.1-10. EST 51 PR1 Temp EST
EST 57 PR2 Temp EST
EST 63 PR3 Temp EST
EST 69 PR4 Temp EST

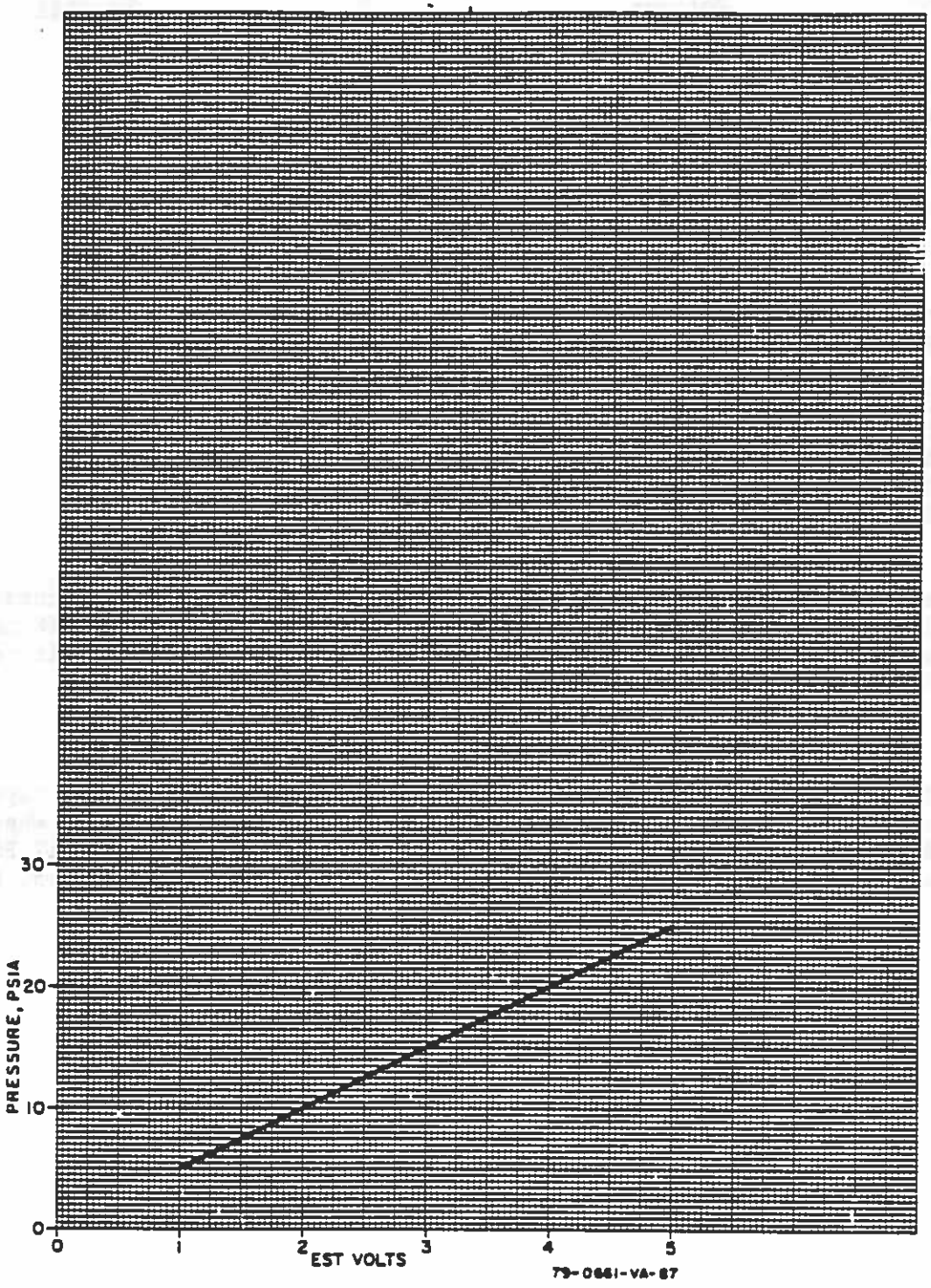


Figure 3.4.1-11. EST 52 PR1 Pressure EST
EST 58 PR2 Pressure EST
EST 64 PR3 Pressure EST
EST 70 PR4 Pressure EST

A tabulation of the nominal temperature vs EST volts data is given below.

°C	Voltage	°C	Voltage
-17.8	.93	+35.00	3.92
-12.2	1.17	37.78	4.06
-6.67	1.45	40.56	4.20
-1.11	1.75	3.33	4.32
+1.67	1.90	46.11	4.44
+4.44	2.08	48.89	4.57
7.22	2.24	54.44	4.78
10.04	2.42	60.00	4.97
12.78	2.59	65.56	5.12
15.56	2.77	71.11	5.28
18.33	2.93	82.22	5.50
21.11	3.12		
23.89	3.29		
25.00	3.35		
26.67	3.44		
29.44	3.60		
32.22	3.76		

The signal is valid whenever S/C +28V power is applied to the recorder. The tolerance for the tape recorder temperature is the base plate (ESM panel) temperature ±5°C, when not recording or playing back. At ambient, this results in an EST range of 2.8 to 3.3 volts.

EST 52 (211) PR1 PRES EST

A DC analog voltage proportional to the internal pressure of the tape recorder. The curve is shown in Figure 3.4.1-11. The signal is valid whenever S/C +28V power is applied to the recorder. The nominal pressure of +17 PSI gives an EST output of 3.4V DC. The acceptable tolerance is 2.5 to 4.5V DC.

EST 53 (024) PR1 Motor Current EST

A dc analog voltage proportional to a motor current error signal, generated at the output of the scaling amplifier on the tape recorder servo/logic board. The typical nominal value is:

Mode	Voltage Range
SDS REC	0.00 - 0.50
SDFNI REC	0.25 - 0.75
SDFI REC	0.60 - 1.20
1.33 PBK	0.90 - 1.50
2.66 PBK	1.20 - 1.80
FAST FORWARD	1.20 - 1.80

A 5V output represents a motor stall condition. This EST is valid only when power enable is sent to the recorder via the SPS.

EST 54 (032) PR1 Servo Error EST

A dc analog voltage proportional to the tape recorder motor control servo-loop time lag. The operational range is +2 to +4V. "Hunting" from 0 to +5V is a typical malfunction. This EST is valid only when power enable is sent to the recorder via SPS.

EST 55 (212) PR1 EOT/BOT EST

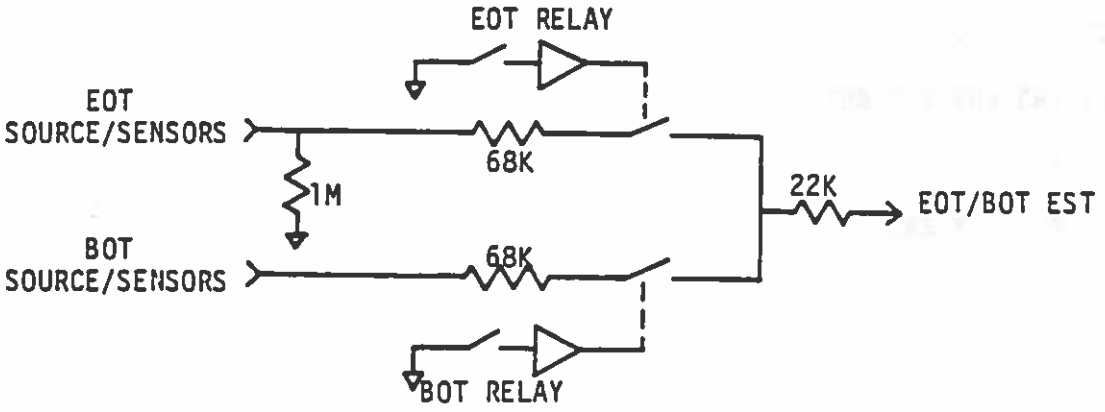
This signal is operative only when tape recorder has received a power enable. The EST will read:

(a) 2.5 ±0.5V when tape recorder in normal record or repro modes.

(b) 4V ±0.5V to 2.5 +0.5V waveform; pulsewidth 30 ms; period 80 ms when at End of Tape (EOT)

(c) 0 ±0.5V to 2.5 ±0.5V waveform, pulsewidth 30 ms, period 80 ms when at Beginning of Tape (BOT).

NOTE: The SPS may turn off power enable very soon after reaching EOT or BOT, so condition (b) and (c) may not last long.



EST 56 (215) PR2 RDY EST

Same as EST 50.

EST 57 (217) PR2 Temp EST

Same as EST 51.

EST 58 (218) PR2 Pres EST

Same as EST 52.

EST 59 (056) PR2 Motor Current EST

Same as EST 53.

EST 60 (064) PR2 Servo Error EST

Same as EST 54.

EST 61 (219) PR2 EOT/BOT EST

Same as EST 55.

EST 62 (222) PR3 RDY EST

Same as EST 50.

EST 63 (223) PR3 Temp EST

Same as EST 51.

EST 64 (225) PR3 Pres EST

Same as EST 52.

EST 65 (072) PR3 Motor Current EST

Same as EST 53.

EST 66 (080) PR3 Servo Error EST

Same as EST 54.

EST 67 (226) PR3 EOT/BOT EST

Same as EST 55.

EST 68 (229) PR4 RDY EST

Same as EST 50.

EST 69 (230) PR4 Temp EST

Same as EST 51.

EST 70 (231) PR4 Pres EST

Same as EST 52.

EST 71 (088) PR4 Motor Current EST

Same as EST 53.

EST 72 (096) PR4 Servo Error EST

Same as EST 54.

EST 73 (233) PR4 EOT/BOT EST

Same as EST 55.

EST 74 (383) PSTATE EST

PSTATE is a dynamic EST which provides information on the processor operation. The signal has eight levels, with each level representing the time the processor is in a particular program module. The states are arranged according to priority. PSTATE 1 has the highest priority and PSTATE 7 has the lowest priority.

PSTATE 1 - Sensor switching processing.
2 - Sensor calibration and segmenting.
3 - Formatting pulses.
4 - Initiate special sensor sampling.
5 - Telemetry processing.
6 - Real time command processing.
7 - Location data processing.
0 - Other processing as required.

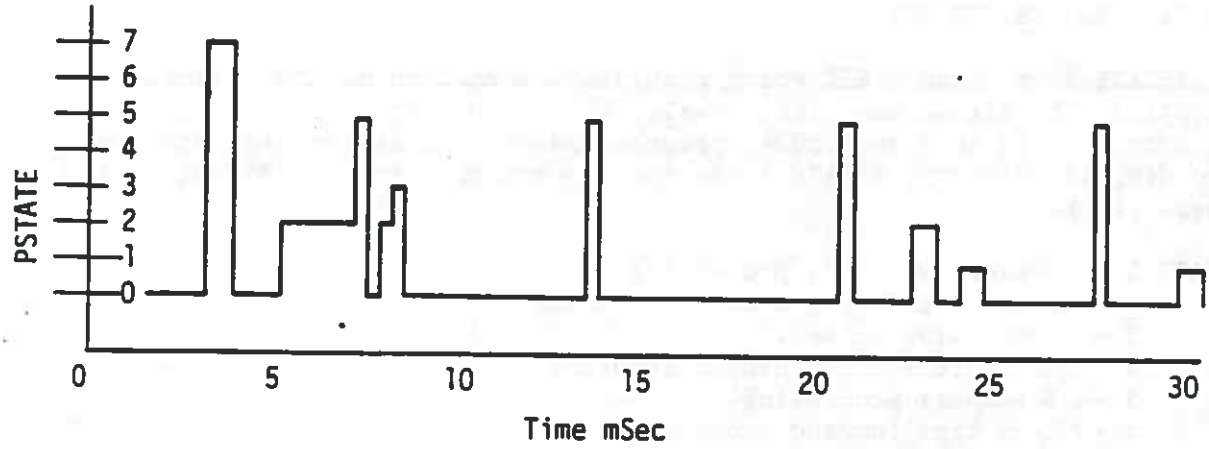
PSTATE 0 is entered if none of the priority states 1-7 demand attention.

PSTATE 0 performs the following functions:

Orbit clock updating
Orbit memory control
Main memory control
Along scan gain control
Direct mode data processing
Command timing
EST processing
Checksum calculation
Processor diagnostic
Command verification
Scanner amplitude calculation

A typical PSTATE representation is shown below. Time 0 represents the peak of the -Z overscan.

PSTATE	DC VOLTS ± 0.4 V
1	0.5
2	0.95
3	1.4
4	1.8
5	2.2
6	2.7
7	3.1



Due to spacecraft bandwidth limitations the on-orbit use of this EST will be limited to verifying that the processor is not stuck in any particular program.

EST 75 (207) SPSF Temp EST

Same as EST 26 for the "F" side core memory. This EST is valid only when Memory F is powered.

EST 76 (241) Scan Enable B EST

A high level (4V + 0.5V) indicates that the SCAN ENABLE B control is selected. A-low level (0V ±0.5V) indicates that this control is not selected. This control will perform its enable function only if DME B is connected to the scanner motor.

EST 77 (213) Cold Patch 1 W Heater EST

This configuration EST monitors the on/off status of the 1 watt decontamination heater on the cone cooler (inner stage) cold patch. For the ASH Heater Command off this EST will read zero to about 1.1 Vdc due to the variable control loop heater power when in space. For the ASH Heater on this EST will read approximately +4.2 to 5.0 volts.

EST 78 (235) Power Supply #1 Temp EST

DC analog voltage related nonlinearly to the internal temperature of power supply #1. The nominal thermistor reading is expected to be between +20°C and +40°C. The curve of EST output versus thermistor temperature is shown in figure 3.4.1-12. The EST is active only when power supply #1 is selected. A list of power supply temperatures and the corresponding EST voltages is provided below.

EST 78 and 148 Power Supply #1 and #2 EST

Voltage	Temperature-°C	Voltage	Temperature-°C
0.05	166.05	1.50	39.29
0.10	134.49	1.60	37.32
0.15	117.79	1.70	35.46
0.20	106.61	1.80	33.72
0.25	98.29	1.90	32.06
0.30	91.69	2.00	30.49
0.35	86.25	2.10	28.99
0.40	81.63	2.20	27.56
0.45	77.62	2.30	26.19
0.50	74.08	2.40	24.88
0.55	70.92	2.50	23.61
0.60	68.06	2.75	20.63
0.65	65.46	3.00	17.88
0.70	63.07	3.25	15.32
0.75	60.86	3.50	12.91
0.80	58.81	3.75	10.63
0.85	56.89	4.00	8.46
0.90	55.09	4.50	4.38
0.95	53.59	4.75	2.45
1.00	51.79	5.00	0.57
1.10	48.53	5.25	-1.27
1.20	46.14	5.50	-3.06
1.30	43.68	5.75	-4.83
1.40	41.40		

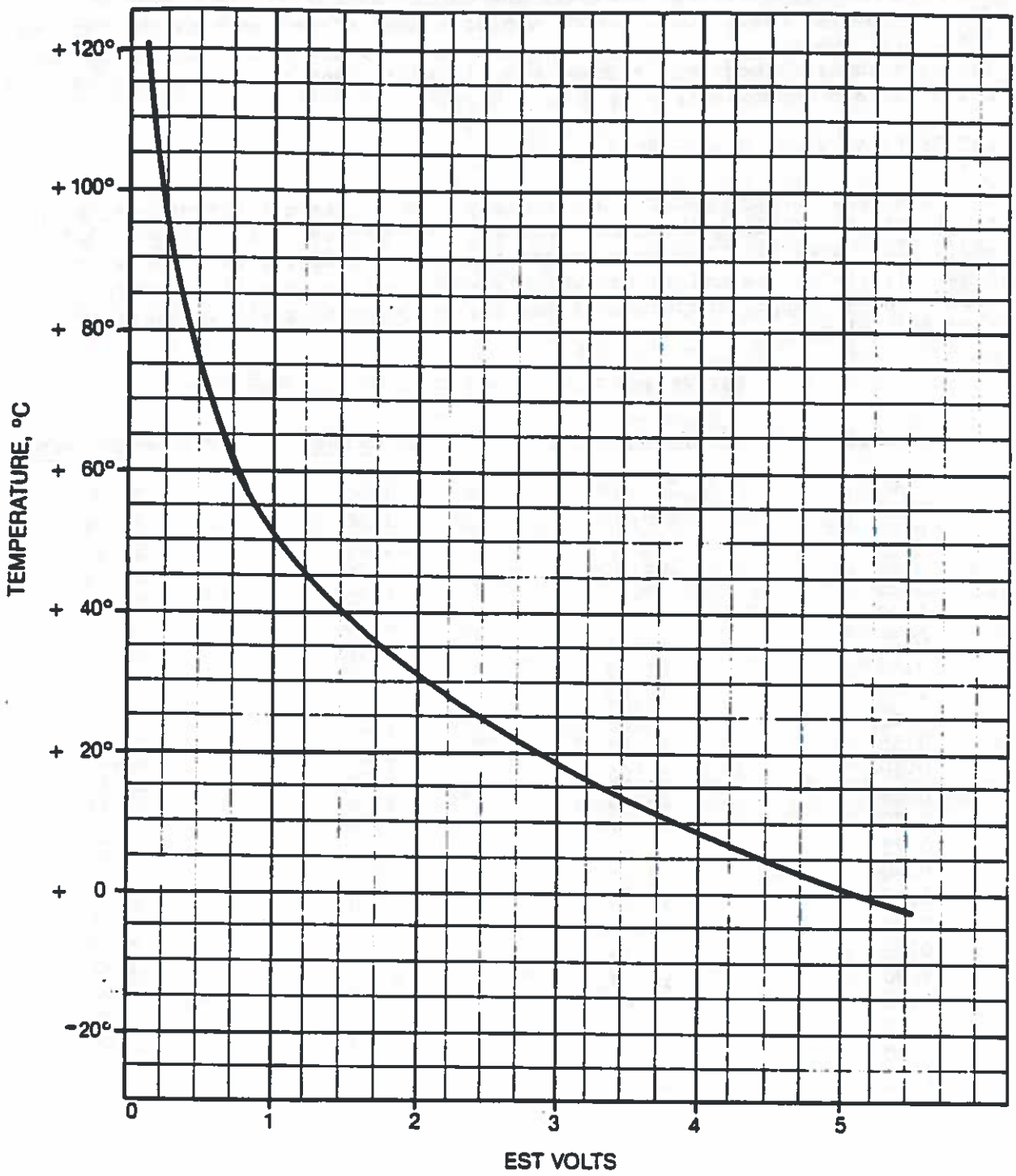
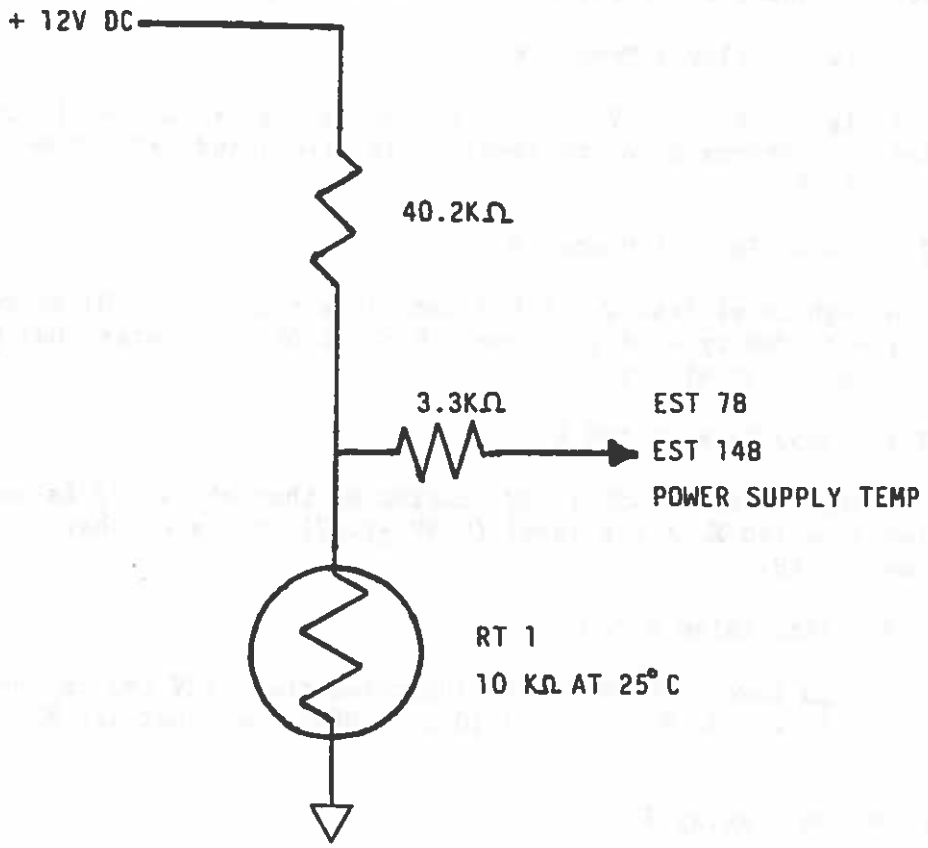


Figure 3.4.1-12. EST 78 Power Supply #1 Temperature
EST 148 Power Supply #2 Temperature

EST 78



EST 78 AND 148 POWER SUPPLY #1 AND #2 TEMP EST

NOTE: The spacecraft PIP uses negative logic (5 volts represents logic zero; and zero volts represents logic one).

The OLS discrete EST threshold for bit transfer from logic zero to logic 1 (or vice versa) is 2.5 volts. However, from 1.5V to 3.5V the state is undefined.

The following discrete EST signal levels are described in terms of their representation within the OLS AVE.

EST 79 (242) Relay 2 Processor C

This digital EST verifies the correct operation of Relay #2. A high level (+4.5V ±1.0V) indicates that +5.3V (D) has been switched through the relay to Processor C. The EST is tapped off the secondary side of the relay. A low level indicates Processor C is connected to an off PS.

EST 80 (243) Relay 3 Memory E

A high level (+4.5V + 1.0V) indicates that +5.3V (D) is connected through relay 3 to Memory E. A low level (0.5V ±1.0V) indicates Memory E is connected to an off PS.

EST 81 (244) Relay 4 Memory F

A high level (+4.5V + 1.0V) indicates that +5.3V (D) is connected through relay 4 to Memory F. A low level (0.5V ±1.0V) indicates that Memory F is connected to an off PS.

EST 82 (245) Relay 5 I/O X

A high level (+4.5V +1.0V) indicates that +5.3V (D) is connected through relay 5 to I/O X. A low level (0.5V ±1.0V) indicates that I/O X is connected to an off PS.

EST 83 (246) Relay 6 I/O X

A high level (+4.5V +1.0V) indicates that +12V (A) is connected through relay 6 to I/O X. A low level (0.5 ±1.0V) means that I/O X is connected to an off PS.

EST 84 (247) Relay 7 I/O Y

A high level (+4.5V +1.0V) indicates that +5.3V (D) is connected through relay 7 to I/O Y. A low level (0.5 ±1.0V) indicates that I/O Y is connected to an off PS.

EST 85 (248) Relay 8 I/O Y

A high level (+4.5V +1.0V) indicates that +12V (A) is connected through relay 8 to I/O Y. A low level (0.5V ±1.0V) indicates that I/O Y is connected to an off PS.

EST 86 (251) Relay 9 Analog

A high level (+4.5V +1.0V) indicates that +12V (A) is connected through relay 9 to the analog section circuit blocks. A low level (0.5V ±1.0V) indicates that the analog loads are connected to an off PS.

EST 87 (252) Relay 10 Formatter G

A high level (+4.5V +1.0V) indicates that +5.3V (D) is connected through relay 10 to Formatter G. A low level (0.5 ±1.0V) indicates that Formatter G is connected to an off PS.

EST 88 (253) Relay 11 Formatter G

A high level (+4.5V ±1.0V) indicates that +12V (A) is connected through relay 11 to Formatter G. A low level (0.5 ±1.0V) indicates that Formatter G is connected to an off PS.

EST 89 (254) Relay 12 Formatter H

A high level (+4.5V ±1.0V) indicates that +5.3V (D) is connected through relay 12 to Formatter H. A low level (0.5V ±1.0V) indicates that Formatter H is connected to an off PS.

EST 90 (255) Relay 13 Formatter H

A high level (+4.5V +1.0V) indicates that +12V (A) is connected through relay 13 to Formatter H. A low level (0.5V ±1.0V) indicates that Formatter H is connected to an off PS.

EST 91 (256) Processor Bus Select

A low level (0V ±0.5V) indicates that Processor C is connected to signal bus A and Processor D is connected to signal bus B. A high level (4V + 0.5V) indicates that Processor D is connected to signal bus A and processor C to signal bus B.

EST 92 (257) Memory Bus Select EST

A low level (0V ±0.5V) indicates that Memory E is connected to signal bus A and Memory F is connected to signal bus B. A high level (4V ±0.5V) indicates that Memory F is connected to signal bus A and Memory E to signal bus B.

EST 93 (258) IF Select EST

A low level (0V +0.5V) indicates that the OLS is accepting and transmitting instructions from the spacecraft using Red/Black X and the Spacecraft Interface block of I/O X. A high level (4V ±0.5V) indicates communication using Red/Black Y and the Spacecraft Interface block of I/O Y.

EST 94 (261) Gain Control Select EST

A low level (0V ±0.5V) indicates that bits from I/O X are controlling the OLS gain control lines. A high level (4V ±0.5V) indicates that I/O Y is controlling the lines.

EST 95 (262) Sensor Control Select EST

A low level (0V ±0.5V) indicates that bits from I/O X are controlling the OLS sensor control lines. A high level (4V ±0.5V) indicates that I/O Y is controlling the lines.

EST 96 (263) Output Data Mux Select EST

A low level (0V +0.5V indicates that the ODM in I/O X is controlling the output data switching and is controlling the data, clocks, sync and controls for the tape recorders. A high level (4V ±0.5V) indicates that ODM Y is performing these functions.

EST 97 (264) Encoder Processor (WF) Select EST

A low level (0V ±0.5V) indicates that the Encoder Processor in I/O X is processing the center detected DELPHI train from the encoder and a high level (4V ±0.5V) indicates that the Encoder Processor in I/O Y is active.

EST 98 (265) CLR/CLK Select EST

A low level (0V ±0.5V) indicates that the clock oscillators and drivers in OSU X have been selected. A high level (4V ±0.5V) indicates that clocks from OSU Y are used.

EST 99 (266) RTD Formatter Select EST

A low level (0V ±0.5V) indicates that RTD data from Formatter G is. selected. A high level (4V ±0.5V) indicates (4V ±0.5V) indicates that data from Formatter H is selected.

EST 100 (267) SDF Formatter Select EST

A low level (0V ±0.5V) indicates that SDF data from Formatter G is selected. A high-level (4V ±0.5V) indicates that data from Formatter H is selected.

EST 101 (268) SDS Formatter Select EST

A low level (0V ±0.5V) indicates that SDS data from Formatter G is selected. A high-level (4V ±00.5V) indicates that data from Formatter H is selected.

EST 102 (271) SSP Formatter Select EST

A low level (0V ±0.5V) indicates that special sensor processing is performed in Formatter G. A high level (4V ±0.5V) indicates that SSP processing is performed by Formatter H.

EST 103 (272) T Analog Select EST

This digital EST identifies whether output data has been derived from the primary or redundant set of T analog filters, both of which are active at all times. A low level (0V ±0.5V) indicates that data is selected from the primary TF and TS filters and a high level (4V ±0.5V) indicates that data is selected from the redundant TF and TS filters. The EST is derived from the SPS output control line.

EST 104 (273) L Analog Select EST

This digital EST identifies whether output data has been derived from the primary or redundant set of L analog filters, both of which are active at all times. A low level (0V ±0.5) indicates that data is selected from the primary LF and LS filters and a high level (4V +0.5V) indicates that data is selected from the redundant LF and LS filters. The EST is derived from the SPS output control line.

EST 105 (274) HRD Backup Select EST

A high level (4V ±0.5V) indicates that the output of the HRD backup postamp is connected to both the primary VDGA and redundant VDGA. A low level (0V ±0.5V) indicates that normal HRD postamp is connected.

EST 106-117 Time Multiplexed EST

A series of twelve time multiplexed EST lines, derived from processor output words, are used to provide configuration information. Of the total 72 bits available, those assigned provide a total of 61 bits of time-multiplexed telemetry which are grouped into 31 functional telemetry elements (see table below). These EST's are updated once per PIP frame. The EST - time slot matrix is depicted in Figure 3.4.1-13.

where: a high level, high state is 4.0V ±0.5V and a low level, low state is 0.0V ±0.5V.

EST 109 [D1] and EST 110 [D2] are exceptions to this. Their high level, high state is 5.15 ± 0.5V. IMCEN, which is one of the multiplexed states of EST 109 [D1], also has a high level, high state of 4.0 ± 0.5V.

Note: In the discussion below, the interpretation of "1" means high value at the input to the PIP and a "0" means a low value at the input to the PIP. The PIP output will be the complemented value. A description of the configuration matrix is as follows:

The SDFPRx discrete (x=1-6) gates the SDFDATA to primary recorder X. A high state shall be an enable and a low state shall be a disable. Software provides logic interlock so that SDFDATA and SQSDATA are not selected simultaneously to the same recorder. This applies to the Record mode only.

The DATCHx discretes (x=1-4) are encoded to select the data source to channel X. Software shall ensure that any particular recorder will be selected to only one channel; however, the RTD formatter may be connected to any number of available channels.

Time Slots	S0	S1	S2	D1	D2	D3	D4	D5	D6	D7	D8	D9
0	0	0	0	SDFPR1	SDSPR1	DT1PRE	BB1PRE	CHADT1	PR1PWR	PR3PWR	BRDF RS	$\overline{TG1}$ (LSB)
1	1	0	0	SDFPR2	SDSPR2	DT2PRE	BB2PRE	CHBDT1	PR1DR2	PR3DR2	BRDF RV	TG2
2	0	1	0	SDFPR3	SDSPR3	DT3PRE	BB3PRE	CHADT2	PR1DR1	PR3DR1	0	$\overline{TG3}$
3	1	1	0	SDFPR4	SDSPR4	DT4PRE	BB4PRE	CHBDT2	PR1WR	PR3WR	0	TG4 (MSB)
4	0	0	1	DATCH1 2^0	DATCH2 2^0	DATCH3 2^0	DATCH4 2^0	CHADT3	PR2PWR	PR4PWR	0	$\overline{TL1}$ (LSB)
5	1	0	1	DATCH1 2^1	DATCH2 2^1	DATCH3 2^1	DATCH4 2^1	CHBDT3	PR2DR2	PR4DR2	0	$\overline{TL2}$
6	0	1	1	DATCH1 2^2	DATCH2 2^2	DATCH3 2^2	DATCH4 2^2	CHADT4	PR2DR1	PR4DR1	0	$\overline{TL3}$
7	1	1	1	IMC EN	0	0	0	CHBDT4	PR2WR	PR4WR	0	$\overline{TL4}$ (MSB)

*NOTE: Some TG and TL bits are formatted in complemented form. TG values are not valid when T RGT and T LFT gains are different; CPU telemetry contains valid T gains.

Figures 3.4.1-13. EST - Time Slot Matrix

The time-multiplexed telemetry bits are groupable into 31 functional telemetry words of follows:

	Time Slot	D[#]	Telemetry Point
1.	0	1	DSDFPR1
2.	1	1	DSDFPR2
3.	2	1	DSDFPR3
4.	3	1	DSDFPR4
5.	4,5,6	1,1,1	ADATCH1
6.	4,5,6	2,2,2	ADATCH2
7.	4,5,6	3,3,3	ADATCH3
8.	4,5,6	4,4,4	ADATCH4
9.	7	1	DIMCEN
10.	0	2	DSDSPR1
11.	1	2	DSDSPR2
12.	2	2	DSDSPR3
13.	3	2	DSDSPR4
14.	0	3	DDT1PRE
15.	1	3	DDT2PRE
16.	2	3	DDT3PRE
17.	3	3	DDT4PRE
18.	0	4	DBB1PRE
19.	1	4	DBBEPE
20.	2	4	DBB4PRE
21.	3	4	DBB4PRE
22.	0,1	5	ACHDT1
23.	2,3	5	ACHDT2
24.	4,5	5	ACHDT3
25.	6,7	5	ACHDT4
26.	0,1,2,3	6	APR1STAT
27.	4,5,6,7	6	APR2STAT
28.	0,1,2,3	7	APR3STAT
29.	4,5,6,7	7	APR4STAT
29.	0	8	ABRDFRS*
29.	1	8	ABRDFRV*
30.	0,1,2,3	9	ATGAIN
31.	4,5,6,7	9	ATLEVEL

*Not processed by PIP.

The encoding of DATCHX is shown below:

	2^2	2^1	2^0
Disconnect Channel	0	0	0
PR1	0	0	1
PR2	0	1	0
PR3	0	1	1
PR4	1	0	0
Not Used	1	0	1
Not Used	1	1	0
RTD	1	1	1

The DTxPRE (x=1-4) discretes are used to indicate that power is applied to the data transmitters. A high state is an enable and low state is a disable. A DT should be enabled 10 sec prior to its use either for playback or RTD transmission. This period is referred to as the warm-up period. Only one DT at a time undergoes warm-up.

The BBXPRE (x=1-4) discretes indicate that the encrypters are commanded on (1) and that the data is sent encrypted. A high state is an enable and low state is a disable. The OLS can control four BBs, even though the present plans call for an operational complement of three.

The CHADTX and CHBDTX (x=1-4) presents the data channel to transmitter interconnection. Any channel (1 through 4) may be connected to any transmitter; however, software will ensure that a transmitter is fed by only one data channel at a time. Encoding is shown below.

DTx Source	Ch1	Ch2	Ch3	Ch4
CHADTx	0	1	0	1
CHBDTx	0	0	1	1

The PR1 - PR4 ESTs indicate tape recorder operating mode and speed. Encoding is shown below:

	PRxPWR	PRxDR2	PRxDR1	1PRxWR
Off	0	0	0	0
Fast Forward	1	0	0	0
Not Used	1	0	0	1
Rec. Fast (SDFI)	1	0	1	0
Not Used	1	0	1	1
Rec. Med. (SDFNI)	1	1	0	0
Playback Slow (SDFNI)	1	1	0	1
Rec Slow SDS	1	1	1	0
Playback Fast (SDFI or SDS)	1	1	1	1

The IMC Enable bit reads a "1" when the IMC is on and a "0" when IMC is commanded off. The normal state is IMC on.

A binary coded output will be generated to indicate the commanded gain of the T-Channel. The EST (TGEST) will have 16 discrete levels representing 16 gain stages. Note the position of the LSB and the fact that TG1 and TG3 are inverted when interpreting the following table.

T GAIN CMD	GAIN, DB
0000	0
0001	0.2313
0010	0.4626
0011	0.6939
0100	0.9252
0101	1.1565
0110	1.3878
0111	1.6191
1000	1.8504
1001	2.0817
1010	2.3130
1011	2.5443
1100	2.7756
1101	3.0069
1110	3.2382
1111	3.4695

A binary coded output (TL1-4) is generated to indicate the commanded offset of the T-channel. The EST point (TL EST) will have discrete levels representing 16 offset stages between 0°C and 15.3°C. Note the position of the LSB and the fact that all bits are inverted.

Decimal	TL Cmd	Level, °C @ 210°K
0	0000	0
1	0001	1.02
2	0010	2.05
3	0011	3.07
4	0100	4.09
5	0101	5.11
6	0110	6.11
7	0111	7.16
8	1000	8.18
9	1001	9.21
10	1010	10.23
11	1011	11.25
12	1100	12.27
13	1101	13.30
14	1110	14.32
15	1111	15.34

The BRDF Rx discretes are used to indicate which BRDF algorithm is enabled. A high state for BRDF RS indicates that the specular component of the BRDF algorithm is enabled. A high state for BRDF RV indicates that the diffuse component of the BRDF algorithm is enabled. These two points (as well as the other EST 116[D8] points) are not processed by the PIP and are not available in the PIP telemetry format. BRDF RS and BRDF RV are brought out via OLS CPU telemetry.

EST 118 (291) Scan Enable A EST

A high level (4V ±0.5V) indicates that the SCAN ENABLE A control is selected. A low level (0V ±0.5V) indicates that this control is not selected. This control will perform its enable function only if DME A is connected to the Scanner Motor.

EST 119 (292) RTD ENABLE EST

A high level (4V ±0.5V) indicates that the RTD mode is enabled. A low (0V ±0.5V) indicates that RTD is off.

EST 120 (293) RTD TF/LS EST

A high level (4V ±0.5V) indicates that the last commanded RTD configuration was TF/LS. A low (0V ±0.5V) indicates that the last commanded RTD mode was LF/TS.

EST 121 (294) SDF Enable LF EST

A high level (4V ±0.5V) indicates that the SDF LF mode is enabled. A low level (0V ±0.5V) indicates that the mode is off.

EST 122 (295) SDF Enable TF EST

A high level (4V ±0.5V) indicates that the SDF TF mode is enabled. A low level (0V ±0.5V) indicates that the mode is off.

EST 123 (296) SDS Enable EST

A high level (4V ±0.5V) indicates that the SDS mode is enabled. A low level (0V ±0.5V) that the mode is off.

EST 124 (214) PMT Blank EST

This SSS output indicates the status of the PMT blanker. A high level (4.8V ±0.48V) indicates that the blanker is ON and low level (0V ±0.5V) indicates that it is OFF.

When the HRD mode is selected, the blanker is on. When the PMT mode is selected, the blanker is off except during the turnaround, or when the light energy into the HRD detector exceeds the blanker threshold.

EST 125 (297) Scan Offset EST

The scanner offset correction feature is not automatic in the 5D-3 system. This EST will indicate by a high level (4V ±0.5V) that the scanner offset needs to be changed. An uplink command will enable the OLS to initiate the offset correction which will then be displayed by an offset calibration word in the primary data subsync frame.

EST 126 (298) COM EST

The Command link is in use when both of the following conditions exist:

(a) The OLS is receiving a 16 bit comm word from the S/C.
(b) S/C DVALID = On (0V ±0.5V @ OLS/SC INTERFACE).

The EST will indicate the above conditions as a high level (4.0V ±0.5V) and the lack of any of the above conditions will be indicated as low level (0.0 ±0.5V).

EST 127 (301) LOG EST

This point (LOGEST) will be a high level (4.0 +0.5V) when L-channel is in the LOG mode and a low (0V ±0.5V) when L-channel is in the LIN mode. The EST originates from a processor register output. Note that even when the LIN mode is commanded, the sensor is automatically switched to LOG for 13 ms during the -Z overscan region for calibration purposes.

EST 128 (220) Scanner Ready EST

This analog EST, with its four levels, indicates when the scanner has reached an amplitude greater than 1018 Delphi pulses at both ends of scan, and also indicates which of two drive Motor Electronics boards is in use. Output voltage limits are as follows:

Status	Output, Vdc
Scanner below 1018	4.20 to 5.00
Scanner above 1018, DME A	2.75 to 3.35
Scanner above 1018, DME B	1.40 to 1.75
Unpowered or Both Scan Enables OFF	zero

EST 129 (302) MAC LOAD EST

A high level (4V ±0.5V) indicates that the OLS is conditioned to perform a memory load using the MAC command and any COMDAT received will be stored in memory. A low level (0V ±0.5V) indicates that the OLS is not in a MAC load sequence and COMDATs received will be interpreted as real time commands.

EST 130 (303) Processor Status EST

A high level (4V ±0.5V) on this EST indicates that a software routine has detected an error in the OLSP program. OLSP is the main operating program in the OLS processor. The error may be a checksum error, diagnostic error, or the result of an OLS load shedding command and is stored in memory as part of the processor status word. The EST will remain high until cleared by uplink command. When an error is detected, the error table should be dumped and analyzed to determine the cause of the problem.

EST 131 (221) +Z HTR CTR EST (1A16)

This EST signal reads 5.04V ± 0.5V when the SSS heater is off and 0V ±0.5V when the SSS heater is on. This EST will normally cycle on and off as the temperature is being controlled. The duty cycle will depend on SSS temperature set point and orbit configuration. The EST originates at the SSS heater. The EST is valid whenever the S/C +28V is present.

EST 132 (227) +X, -Z HTR CTR EST (1A19)

Same as EST 131.

EST 133 (228) -X, +Z HTR CTR EST (1A18)
Same as EST 131.

EST 134 (234) -X, -Z HTR CTR EST (1A17)
Same as EST 131.

EST 135 (304) PC Run EST

A high level (4V ±0.5V) indicates that processor C has left the loader and is executing some program. A low level (0V ±0.5V) indicates that processor C has returned to the loader.

EST 136 (305) PD Run EST

A high level (4V ±0.5V) indicates that processor D has left the loader and is executing some program. A low level (0V ±0.5V) indicates that processor D has returned to the loader.

EST 137 (306) RELENC EST

A high level (4V ±0.5V) indicates that the SPS is deriving encoder information from the real encoder. A low level (0V ±0.5V) indicates that the SPS is using its encoder simulator to provide encoder information.

EST 138 (307) DOCMD EST

A high level (4V ±0.5V) indicates that the operational program (OLSP) is conditioned not to receive commands. A low level (0V ±0.5V) indicates that the OLSP can accept commands. This discrete is set during program loads and also by the other processor if the diagnostic program is being commanded.

EST 139 (311) REDENC EST

A high level (4V ±0.5V) indicates that the redundant fiducial and auxiliary encoder (mirror) are selected. A low level (0V ±0.5V) indicates that the primary fiducial and auxiliary encoder (vane) are selected.

EST 140 (312) VAC EST

A high level (4V ±0.5V) indicates that the DME pulse drive switch is selected for the vacuum environment. (The operational program initializes to this state.) A low level (0V ±0.5V) indicates that the DME pulse drive switch is selected for the atmospheric environment.

EST 141 PSU Spare EST (OLS 12) or EST 141 (313) Solenoid Command State (OLS 13 and up)

This EST is presently a spare digital EST from the PSU. The telemetry point will be solenoid command state on OLS 13 and up. The EST will have the following states:

The EST has the following states:
Low voltage state (~0v to 0.7v) represents "Solenoid commanded to activate".
High voltage state (~4.7v) represents "Solenoid not commanded to activate".

EST 142 PSU Spare EST

This EST is presently a spare analog EST.

EST 143 PSU Spare EST

This EST is presently a spare analog EST.

EST 144 (308) Freerun EST

A high level (4V ±0.5V) indicates that the encoder simulator is in the freerun mode. A low level (0V ±0.5V) indicates that the encoder simulator is locked to the real encoder control track.

EST 145 PSU Spare EST (OLS 12) or EST 145 (314) Solenoid State (OLS 13 and Up)

The EST has the following states:

Low voltage state (~0 to 0.7v) represents "Solenoid fully activated."
High voltage state (~4.7v) represents "Solenoid not fully activated."

EST 146 (236) PS1 Status EST

Independent of the state of the override command when the OLS power enable to side 1 is OFF the input to the EST channel should be approximately +6.0 Vdc yielding a full scale EST output voltage. If the power enable to side 1 is ON, the EST should indicate +3.25 Vdc ±6%. If both the override command and the power enable to side 2 are ON, the EST should indicate +2.10 ±6%.

EST 148 (241) Power Supply #2 Temp EST

DC analog voltage related nonlinearly to the internal temperature of power supply #2. The nominal thermistor reading is expected to be between +20°C and +40°C. The curve of EST output versus thermistor temperature is shown in figure 3.4.1-12. The EST is active only when power supply #2 is selected.

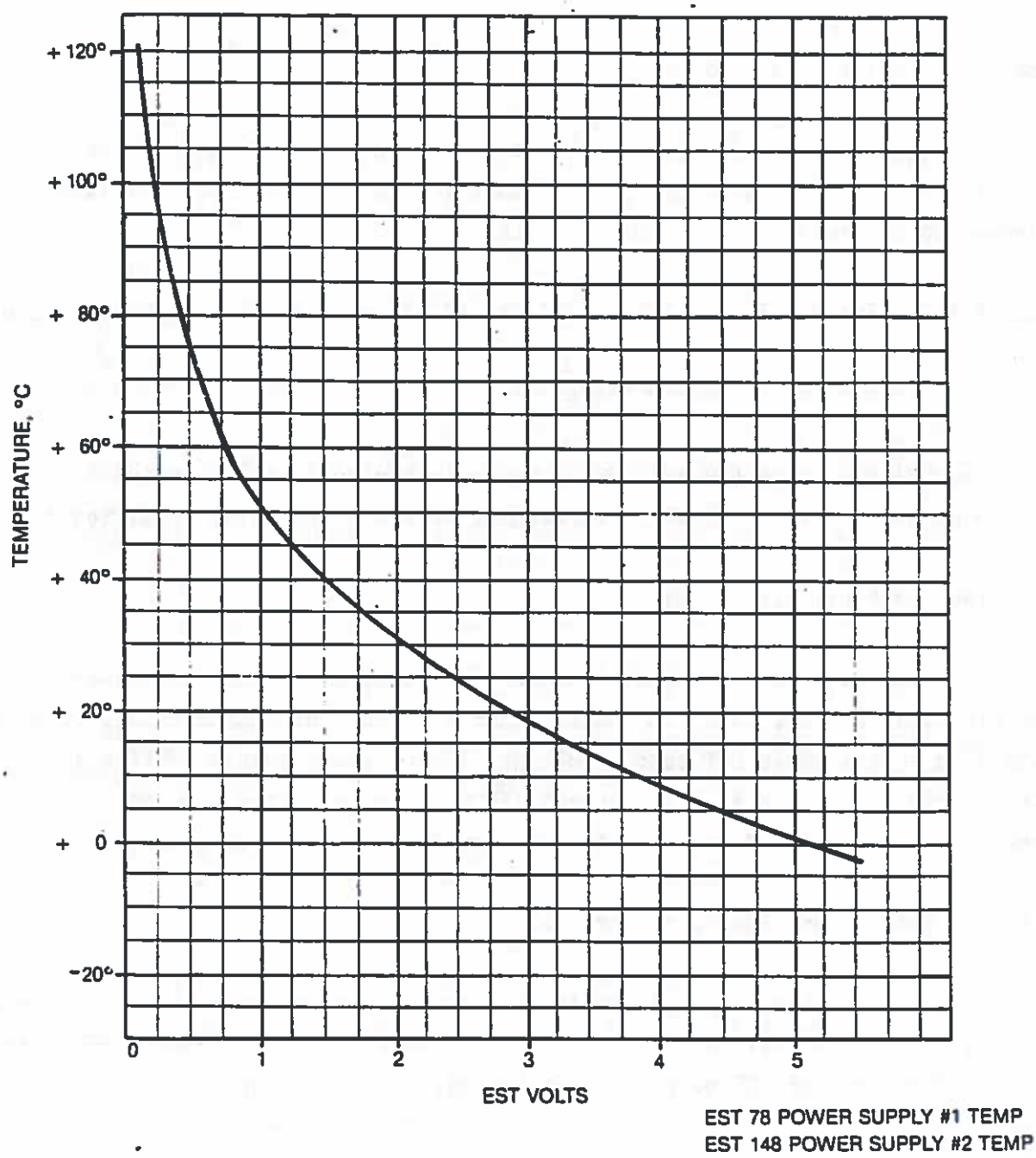


Figure 3.4.1-12. EST 78 Power Supply #1 Temperature
EST 148 Power Supply #2 Temperature

3.4.2 Processor Telemetry

3.4.2.1 General Description

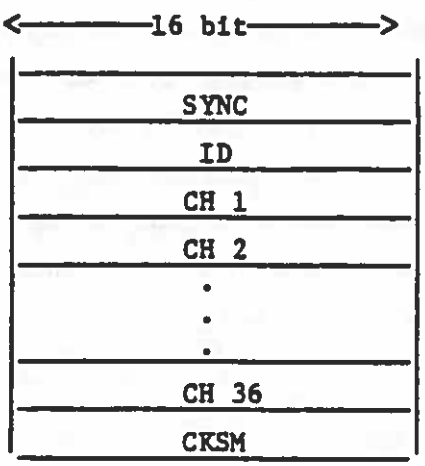
A 40-word OLS CPU telemetry frame is continuously output on the OLS-S/C interface MDDATA except when interrupted by a memory load, memory dump, program load, or mission sensor load. The interruptions can also occur by the redundant processor performing a program load or special diagnostic dump. After interruption, the telemetry output is reset to the beginning of the frame. Sync words differentiate between telemetry and dump/load data. In addition, an ID word following the sync further defines the type of load/dump, identifies the processor using MDDATA, and presents other information defining the telemetry table in use.

3.4.2.2 Data Rate

The CPU telemetry data rate varies as a function of program loading. When the program is first initialized the rate can go up to almost 140 16-bit words per second. When the program is running a normal load with ASGC on, the maximum rate is about 80 words per second. These rates can only be accomplished with the S/C PIP in the 10 kilobit OLS dump mode, which provides a 220 words per second channel. Data words not supplied by the OLS in this case will be supplied as filler code (Hex AAAA) by the PIP. The maximum data rate will be limited (by the PIP) in other PIP modes to either 4 or 40 words per second.

3.4.2.3 Frame Format

The telemetry frame format is shown below:



The value of SYNC is octal 123456. The ID word contains the processor ID, a TAG field of zero, an a TBLID according to the following format:

16	15 10	9 1
I	TAG	TBLID

I = 1, processor D

1 = 0, processor C

TAG = 0 defines CPU telemetry

TBLID = 0 defines the baseline telemetry supplied with the flight program OLSP ---

CH 1 through CH 36 contain the data associated with the parameters as defined in the telemetry address table. CKSM is the checksum of the 40 word telemetry address table and will remain constant for any given CPU telemetry address table.

3.4.2.4 Reprogramming Processor Telemetry

The CPU telemetry table can be reprogrammed by a simple MAC load sequence to include the contents of any memory location which can be accessed by the processor. When reprogramming, the TBLID field should be changed to identify the new parameter formats. As an example, suppose it is desired to include the scanner amplitude limit in channel 32. This parameter has the label C7EMLM and is located in address 036 of block 017 (absolute address 07436) in program OLSPO2J. The command sequence is:

```
100115  ; MAC word count 2 (count includes ID word)
010035  ; MAC TLM CH 32
000575  ; MAC TLM LOAD
P00XXX  ; ID (P=parity bit, XXX identifies new table)
107436  ; +C7EMLM (absolute address including parity bit of parameter
          C7EMLM)
```

Reprogramming the telemetry table can be useful for selecting other parameters of interest or to increase the effective sampling rate of one or more parameters by listing their occurrence more than once in the table.

3.4.2.5 Channel Parameter Formats

The following defines the channel parameters for the baseline program load. Unless otherwise specified, names will be defined for the logic "1" state. Negative numbers are represented in two's complement form.

CH 1 +E6STATUS OLSP Status Word

16	15 12	11 8	7 4	3	2	1
0	INIT	VER	REV	E3	E2	E1

E1 = Checksum error table entry — Can only be cleared with SPC command

E2 = Shed OLS loads

E3 = System error table entry

Rev = Program Revision (10 for OLSPO2J)

Ver = Program Version (2 for OLSPO2J)

Init = Number of times program was initiated since memory power was turned on.

CH 2 +M1ON Main Memory Status

16		2	1
Wait		ON	TTT

TTT = Time Tag Test in Progress
ON = Main Memory Program On
WAIT = Main Memory In Standby

CH 3 +M1ADR Main Memory Address

16	11	1
	2^{10} ADR	2^{0}

ADR = Address in Main Memory relative to uplink memory start. If TTT=0, then CH3 represents the address of the next command to be executed, if TTT=1, then CH3 represents the address of the command following the one awaiting execution.

CH 4 +M4ETC Main memory Clock

16		1
2^{16}	SEC	2^{1}

Represents the current state of the Main Memory clock (LSB = 2 sec). Actually the sampled ETC.

CH 5 +M2ON Orbit Memory Status

16		2	1
		ON	TTT

TTT = Time Tag Test in Progress
ON = Orbit memory Program is ON

CH 6 +M2ADR Orbit Memory Address

16	11	1
	2^{10} ADR	2^{0}

ADR = Address in Orbit Memory relative to uplink memory start. If TTT=0, then CH6 represents the address of the next command to be executed, if TTT=1, then CH6 represents the address of the command following the one awaiting execution.

CH7 +M4OC Orbit Memory Clock

16		1
2^{14}	SEC	2^{-1}

Represents the current state of the orbit clock (LSB = 1/2 sec). This clock is updated every 2 sec in sync with the ETC. Command execution is interpolated between 2 second marks using the processor's real time clock.

CH8 +S1PT Scanner Period

16		1
2^{15}	SIPT	2^{0}

Represents the scanner period in seconds averaged over 16 scan cycles.

Period = (SIPT + 2^{17}) 1.06496 x 10^{6}
Nominal value for SIPT is 48214

CH 9 +E2EM SCANNER AMPLITUDE

16		1
2^{11}	ENCODER COUNT	2^{-4}

Represents the scanner amplitude in number of delphi pulses from Nadir. This number is computed about once every 30 milliseconds and has a nominal value of 1024.5.

CH 10 +V1CMD Last Executed Command

16	15	11
CV	CMD	

Represents the last command executed. This could either be a real time, main memory, orbit memory or S/C LOCDAT command. If the last command was a MAC load, this value represents the last data word of the load. Other data words of the load may show-up if the sample rate is high enough. CV is the command verification bit (used internally by the program). A logic "1" indicates even (bad) parity received.

CH 11 +F2RRQ PR0 STATUS

CH 12 +F2RRQ+5 PR5 STATUS

16	15	14	13	12	11	10	9	8	7 6	5 4	3 2 1
R	ON	ONP	INT	CV			B	A	S/D	SUB	PR

PR represents the recorder number. PR0 and 5 are for record mode testing only in that the formatters are producing prerecorded data but no recorder is on. The SUB field indicates the type of command.

SUB	TYPE
0	off
1	record
2	playback
3	fast forward

S/D represents source/destination

SUB	RECORD	PLAYBACK
0	SDF	Channel 1
1	SDS	Channel 2
2	N/A	Channel 3
3	N/A	Channel 4

The A and B field further define command configuration.

B	A	
LF	TF	SDF Record
Low Speed	Clear	Playback

CV is the Command Verification bit. A logic "1" indicates the command was received with incorrect parity.

INT is set while the recorder is undergoing a 5 second interlock. This bit is set when the recorder is turned off and should remain on for 5 seconds.

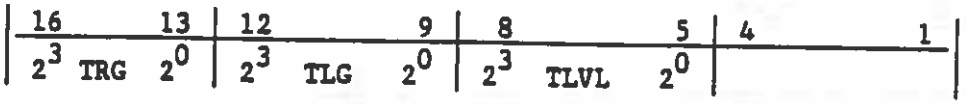
ONP is set when the recorder is initially turned on. This bit remains on for 10 milliseconds and is followed by the ON bit. ON remains on as long as the recorder is in use.

R is the recorder request bit which is set when a record command is received. This bit remains on until the request has been acknowledged and executed.

CH 13	+F3RLOC	PR1	Location
CH 14	+F3RLOC+1	PR2	Location
CH 15	+F3RLOC+2	PR3	Location
CH 16	+F3RLOC+3	PR4	Location

Primary recorder location. Reset to zero at BOT. Computed from elapsed time since turn on and commanded speed. Each ON/OFF sequence can have an inaccuracy of ±2 seconds times the recorder speed. The inaccuracies will accumulate until they are removed at BOT.

CH 17 +NOTCHA T CHANNEL



TRG represents the gain of the right T-Channel and TLG represents the gain of the left T-Channel. TLVL is the value of the T-Level setting.

CH 18 +S1PAB +Z OVERSCAN TIME

$$\left| \frac{16}{2^{15}} \quad S1PAB \quad \frac{1}{2^{0}} \right|$$

+Z overscan time between encoder counts 1018 leading edges.

T (seconds) = S1PAB/CLK

where CLK = 1064960. Hz

CH 19 +S1PBC DOS 0 ACTIVE TIME

$$\left| \frac{16}{2^{15}} \quad S1PBC \quad \frac{1}{2^{0}} \right|$$

DOS 0 active time between encoder counts ±101% leading edges.

T (seconds) = (S1PBC $+2^{16}$)/CLK

where CLK = 1064960. Hz

CH 20 +S1PCD -Z OVERSCAN TIME

$$\left| \frac{16}{2^{15}} \quad S1PCD \quad \frac{1}{2^{0}} \right|$$

Z overscan time between encoder counts -1018 leading edges.

T (seconds) = S1PCD/CLK, CLK = 1064960. Hz

CH 21 +S1PDA DOS 1 ACTIVE TIME

$$\left| \frac{16}{2^{15}} \quad S1PDA \quad \frac{1}{2^{0}} \right|$$

DOS 1 active time between encoder counts ±1018 leading edges.

T (seconds) = (S1PDA + 2^{16})/CLK, CLK=1064960 Hz.

CH 22 +C6LOCK DT Status

16	15	14	4	3	2	1
F5	F6	C6	DT4	DT3	DT2	DT1
WU	WU	RQ	I	I	I	I

Bits 1-4 define the data transmitters which are interlocked against turning on. F5WU indicates that an RTD or playback command has placed a DT in warm-up. C6WU indicates a DT warm-up as controlled by the TBC command (CMD06). Additional TBC commands waiting in a que are indicated by a command 06 request, C6RQ=1.

CH 23 +G2BIAS BIAS

16	15 1
S	2^{7} BIAS 2^{-7}

Bias adjustment in degrees for the scene solar elevation, SSE, where

GAMMA = SSE + BIAS

CH 24 +G2MODE GAIN MODE

16 1
MODE

where MODE = 0 defines preset gain control
MODE = 1 defines along scan gain control
MODE = -1 defines along track gain control

CH 25 +S4CSAZ COSINE SOLAR AZIMUTH

16	15 1
S	2^{-1} COSAZ 2^{-15}

Used as a multiplying factor to the earth geocentric angle, THETA, for the computation of scene solar elevation,

SSE = EL + COS(AZ) *THETA

CH 26 +S4ELVT SOLAR ELEVATION

16	15 1
S	2^{7} EL 2^{-7}

Solar elevation in degrees used in computation of scene solar elevation (see CH 25).

CH 27 +S4RRH1 1 + ALT/EARTH RADIUS

16	15 1
0	2^{0} (1+h/R) 2^{-14}

(R+h)/R=1+(S/C altitude/earth radius) which is used for the calculation of the earth geocentric angle, THETA, at the scene.

THETA = $\sin^{-1}$ [(1+h/r) sin Ø] - Ø
where Ø is the scan angle of the scene

CH 28 +S4LONG LONGITUDE

16	15 1
S	2^{-1} LONG 2^{-15}

Represents the S/C longitude in radians.

CH 29 +S4LAT LATITUDE

16	15 1
S	2^{-1} LAT 2^{-15}

Represents S/C latitude in π radians.

CH 30 +F1ZBFA+9 LUNAR Z1-Z16

16 9	8 1
$S2^{-1}$ COS(AZL) 2^{-7}	$S2^{6}$ ELL 2^{0}

COS(AZL) is used as a multiplicative factor to the scene geocentric angle, THETA, in the computation of scene lunar elevation. ELL is the lunar elevation in degrees used in the computation of scene lunar elevation,

SLE = ELL + COS(AZL) *THETA

CH 31 +F1ZBFA+8 LUNAR Z17-Z32

16 12	11 4	3 1
2^{-1} ELL 2^{-5}	2^{7} ABS(LUN PHASE) 2^{0}	1 0 1

ELL - See CH 30.
ABS(LUN PHASE) is the absolute value of lunar phase in degrees and is used as a gain adjustment under moonlit conditions. Full moon is zero degrees.

CH 32 +NOMSK3 SEGMENT OVERRIDE

16 10	9	8	7	6	5	4	3	2	1
	R	M	L	R	M	L	R	M	L
	T			HRD			PMT		

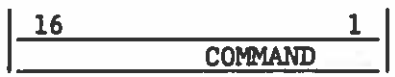
This parameter indicates when any segments, left, mid, or right of any of the sensors have been commanded to an override state during active video.

CH 33 +V30W01 VDGA BASE GAIN

16 1
2^{5} BASE 2^{-10}

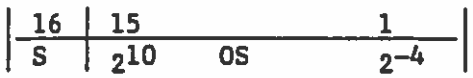
Represents the gain in dB of the VDGA at start of active data (encoder count $\pm$996).

CH 34 +S4CMD S/C LOCDAT COMMAND



Represents the lost command received on the S/C LOCDAT interface. Only PSC commands will be executed.

CH 35 +S1OS SCANNER OFFSET



The scanner offset, in number of delphi's, is computed oncer per scan cycle. If the encoder simulator has been commanded to free-run this number is the value at the time of the command execution.

CH 36 +S1SWOS OLSP OFFSET

Represents the software offset in delphi's. This number is zero if the encoder simulator is in use. The software corrects to the software offset by an integer number of delphi's according to:

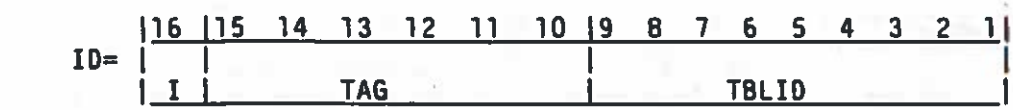
Software offset correction = INT [SWOS + 0.5].

If the scanner offset (SIOS) averaged over 1024 scan cycles exceeds the software offset by 0.5 delphi hysteresis, the software offset is updated to the new average offset and a new integer correction is applied. This update does not take place if the inhibit offset correction bit in uplink memory is set.

3.4.2.6 MDDATA Formats

As previously described, other types of data besides processor telemetry appear in MDDATA. The frame formats for this data are of variable length and are defined below.

SYNC1 = 0123456
SYNC2 = 0137465



I (PROCESSOR NO.): PROC C = 0, PROC D = 1

TAG	FUNCTION
0	OLS CPU TELEMETRY
1	MAC LOAD PAGE
2	MAC DUMP PAGE
3	MAC LOAD BLOCK
4	MAC DUMP BLOCK
5	MAC LOAD TLM ADDRESSES
6	MAC DUMP TLM ADDRESSES
7	MAC LOAD MISSION SENSOR
010	SPC DUMP CONSTANTS MEMORY
011	SPC DUMP GVVSSE
012	SPC DUMP MAIN PROGRAM
013	SPC DUMP ORBIT PROGRAM
014	SPC DUMP DMDM
015-017	SPARE
020	SPC DUMP PROCESSOR STATUS WORD
021	SPC DUMP CKSM ERROR TABLE
022	SPC DUMP SYSTEM ERROR TABLE
023	SPC DUMP MAIN PROGRAM STATUS
024	SPC DUMP ORBIT PROGRAM STATUS
025	SPC DUMP ELAPSED TIME COUNT
026	SPC DUMP ERROR TIME CODE
027	SPC DUMP OLS CPU TELEMETRY TABLE
030	SPC DUMP PROCESSOR I/O INPUT SELECT
031	SPC DUMP PROCESSOR I/O OUTPUT SELECT
032	SPC DUMP BLOCK
033-037	SPARE
040-075	RESERVED FOR OTHER PROCESSOR/PROGRAMS
076	DIAGNOSTIC DUMPS
077	PROGRAM LOAD/VERIFY/GO TO

For TAG 0-037, TBLID = telemetry address table number which is zero for base line telemetry table loaded on a normal program load. For TAG = 040-075, TBLID = 0.

For TAG = 077, TBLID indicates the value uplinked from the ground which, for program loads, will be program version in bits 5-8, program revision in bits 1-4, and zero in bit 9.

For TAG = 076, TBLID indicates the block number for a scratch block dump, 0376 for the checksums dump, and 0377 for an OLS 16K memory dump.

CPU telemetry can be interrupted by either processor at any word of its 40-word frame. After the interrupting program is finished using MDDATA the CPU telemetry will restart with word 1 of its frame. Figure 3.4.2-1 represents the different data formats appearing on MDDATA.

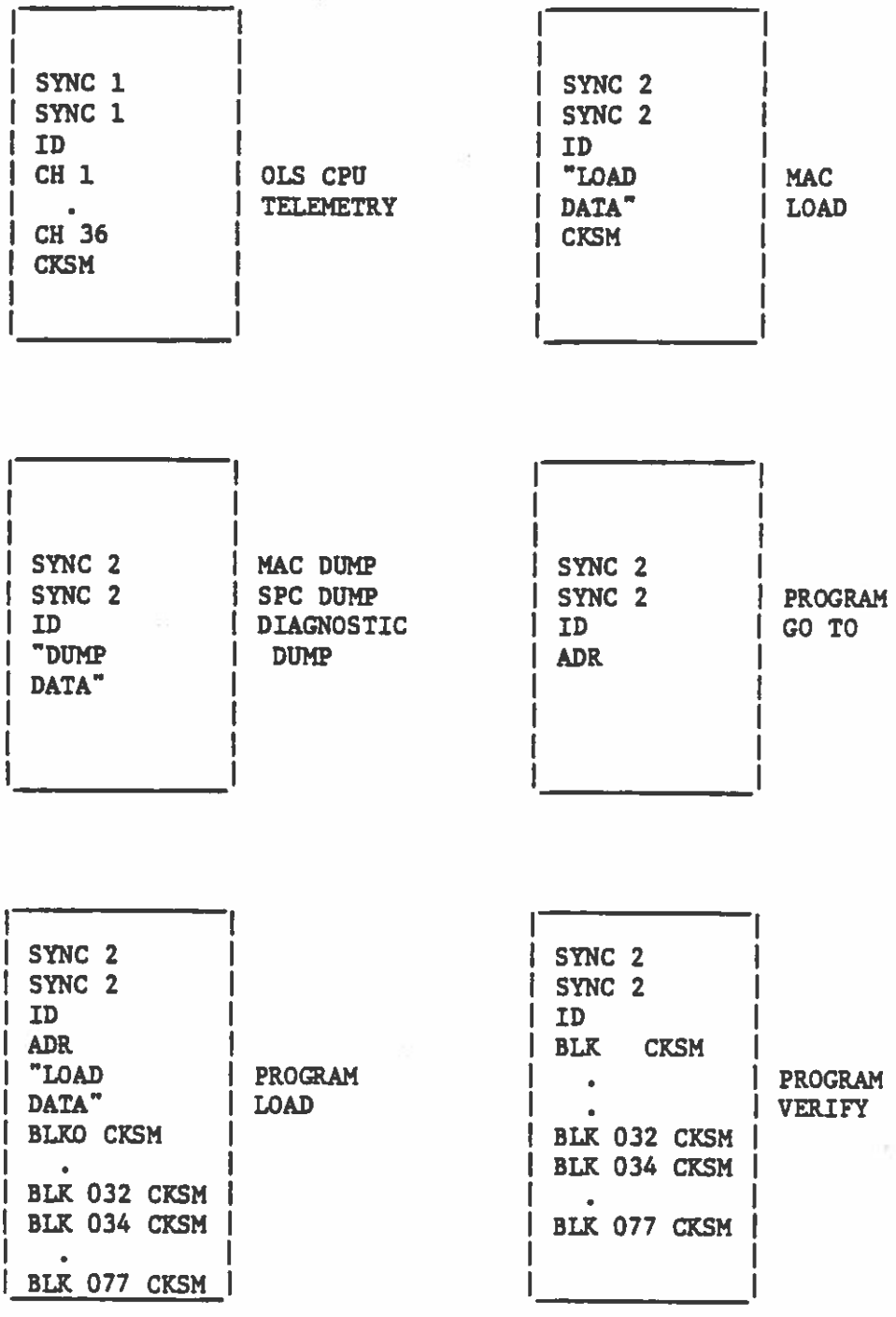


Figure 3.4.2-1. MDDATA Data Formats

APPENDIX I
OPERATORS MANUAL

Dwg. No. MN315R808P01 Rev R
Code Ident. 97942

BVS 0630

DATE June 11, 1975

ORIGINATOR Kenneth R. Martin

REVISED August 10, 1989

OLS 5D

OPERATIONAL COMMANDING MANUAL

Contract F04701-86-C-0078

(Task 86-01)

Prepared For

UNITED STATES AIR FORCE
Headquarters, Space Division
Los Angeles, California

Prepared By

WESTINGHOUSE ELECTRIC CORPORATION
Defense and Electronics Center
Baltimore, Maryland

BVS No. 0630

REVISION SHEET & NOTES PAGE

REVISION LETTER	REVISION DATE	AFFECTED PAGES	REVISION MADE BY
P	6/13/85	Complete re-write	SCN 098
P1	2/13/86	5, 6, 10, 12, 30, 35, 41, A-3, A-5, A-7, A-11, A-12, B-3, B-4 & B-5(typo corrections)	-
Q	10/30/86	9, 11-14, 20, 23-25, 31, 34-36, 39-41, A-2, A-3, A-5, A-7, A-13, B-4, B-5, D-2	SCN 108 CR OL-2084
R	8/10/89	i, 6, 14-21, 24, 27, 28, 30, 34-36, 38-43, A-2, A-7, A-9, A-11, A-12, A-13, B-3, B-4	SCN 124

(* INDICATES PAGE # IS ONLY CHANGE TO THAT PAGE)

Notes:

WANG Doc. #(s): gp/1032B

TABLE OF CONTENTS

1. INTRODUCTION

This document contains information relating to uplink commanding which will be of use to those who must program the OLS 5D system. An attempt has been made to structure the discussion such that one section leads into the next. A complete listing of the uplink command formats and uplink memory formats appear at the end of this report.

The discussion starts with a description of the initial loading of the operational program OLSP. This is followed by a description of the uplink commands and uplink memory. A complete definition of the uplink memory constants is included. This leads to sections on how to send real time commands and how to program with stored commands.

Sections are included which discuss Mission Sensor Programming. In addition, the system interlocks provided by the software are described.

Finally, a section on error analysis is presented. This may be of particular interest since OLS 5D-1 does not have this capability. The various error indications and their use is presented.

2. LOADING THE OPERATIONAL PROGRAM

2.1 Program Memory

The OLS 5D contains two independent memories which are loaded by two processors. Processor C or Processor D can load either memory and the one loaded is determined by the way the system is configured via S/C interface lines and also which load processor pulse is received from the S/C. Only one processor is loaded at a time using the COMDAT uplink S/C interface line.

Each memory consists of 3K words of ROM and 13K words of read/write memory. The ROM contains the loader program, checksum and diagnostic programs, tables, and other programs which probably will not be changed in the future. The read/write memory contains the remainder of the operational program (11K) and the uplink memory (2K).

The memories are segmented into blocks of 256 words each. There are 0100 blocks per memory (in this report all numbers with a leading 0 are written in octal notation). The ROM program is contained in blocks 0-013. The operational program is in blocks 014-067. The uplink program, page 0-7, is contained in blocks 070-077.

The program can be loaded in one continuous piece or any number of patches may be made to any address. The starting address of the read/write memory is location 000 of block 014. The program start address is location 000 of Block 020 which represents an absolute address of 010000. This is also the address to which control should be transferred after completion of the program load. Absolute addresses for any part of memory can be computed as shown below where the address within the block (000-0377) is in bits 1-8 and the block number (0-077) is in bits 9-14.

ABSOLUTE ADDRESS

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
		M_S					L_S	M_S							L_S
0	0	B	--BLK--				B	B	--ADR--						B

2.2 Load Format

The program load format consists of three parts -HEADER, ADDRESS, and DATA. The first words recognized by the loader will be the header. All words preceding the header will not be recognized but will be echoed via MDDATA. Bit 16 will always represent the MSB and will be the first bit transmitted.

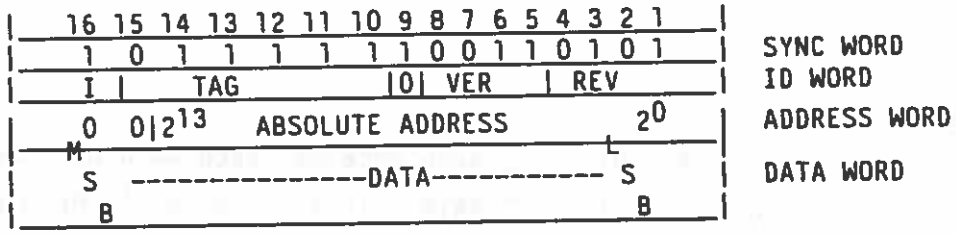
In order to reduce program load time, the program load, excluding S/C load controls, should be sent in the S/C data mode (not encrypt mode).

The header consists of 2 consecutive sync words followed by an ID word. The ID word contains 4 fields. When the ID word is echoed the loader sets the TAG field to 077 and the I field to 1 for processor D and 0 for processor C. VER contains the version and REV contains the revision of the OLSP.

The first word received after the header is an address word. This word defines the address in which to place the next word (data) which follows. The address in this word represents the absolute address in memory.

The first word received after the address word is the data word to be placed in the specified address. This data word could represent an operational program instruction or data or uplink program constant, command, time tag, or data.

Any number of data words can follow until the load is complete. Each data word will be stored in suceeding locations in memory.



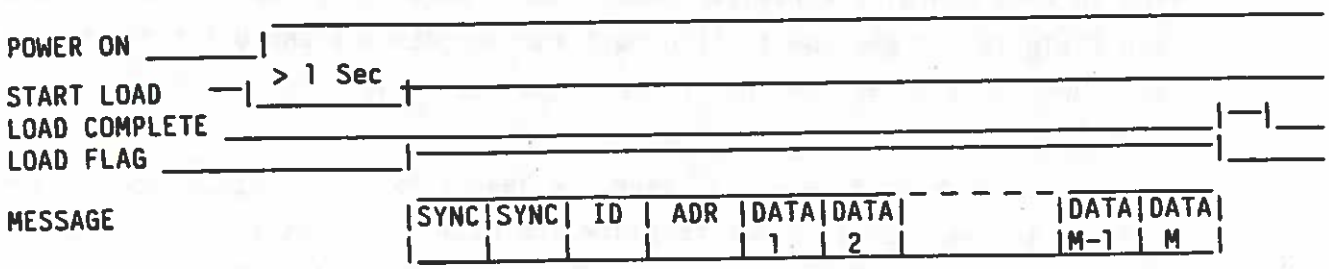
2.3 Load Controls

The controls used to activate the loader sequence are derived from S/C interface signals. A LOAD PROCESSOR "X" pulse will force that processor to the loader program where "X" represents either processor C or D. Since the load processor interface to the OLS is a level type, two S/C commands are required to generate this pulse (LOAD PROCESSOR "X" LOW - LOAD PROCESSOR "X" HIGH).

The START LOAD processor "X" pulse sets a flag which can be tested by the 2 processors so that the data to follow can be input by the correct processor. Only one processor can be loaded at a time, therfore before the other START LOAD pulse is received, a LOAD "X" COMPLETE Command must be transmitted. The LOAD COMPLETE resets the flag described above.

The correct sequence for loading would be to send the START LOAD pulse immediately followed by the header, address word, and any number of data words. The LOAD COMPLETE command should be sent after the last data word has been sent. The following figure shows the sequence along with critical timing.

PROGRAM LOAD TIMING



The START LOAD pulse should last for 1 second following a power on in order for supply voltages to settle and for the system to reach a clear or intial state.

The LOAD COMPLETE command can occur anytime 50 us after the last bit of the last data word was transmitted. It must occur prior to sending the first uplink command or prior to sending the START LOAD pulse for the other processor.

2.4 Downlinking

After the START LOAD pulse has been received each word uplinked will be downlinked via S/C interface line MD DATA. These words will include the HEADER, address word, all data words, and any data which may have preceded the HEADER. After the LOAD COMPLETE command occurs, the program enters the VERIFY section of the LOADER. Any additional uplinks will be ignored.

2.5 Program Verify

Locations 000-077 of block 033 data are reserved for precomputed checksums (at program assembly time) of the memory blocks from 000 to 077. Space for block 033 is reserved although it is not checksummed. The CHECKSUM part of the LOADER will compute a new checksum on each block starting with block 000 and continuing up through block 077, skipping block 033, and downlinking each checksum via MDDATA after it is computed. The ground can then verify the downlinked values of the blocks loaded against the checksum data base in block 033.

After the checksum for block 077 is downlinked, the IDLE part of the LOADER is re-entered and the program awaits a START LOAD pulse as before. Several options are then available.

1) From the downlinked checksums, a determination of which blocks were bad can be made and these blocks can be individually uplinked until all blocks pass the test.

2) Perhaps the failed blocks were not needed and, therefore, not uplinked. In this case, a START LOAD followed by a LOAD COMPLETE will transfer control to the operational program at location 010000.

3) Uplink the entire program again if time permits.

4) Start the operational program by sending a START LOAD followed by a LOAD COMPLETE.

Checksums are computed according to the algorithm shown below.

$$CKSM = [CKSM + MEM(X)]_{SRC,1}$$

where SRC,1 is a 1-bit circular right shift on the 16 bit sum, ignoring any carry bit. MEM(X) is location X of a particular blocks where X starts at 0377 and ends at 0.

A Program Verify can be performed at any time by the sequence: START LOAD, HEADER, LOAD COMPLETE .

2.6 Operational Program Start

The Operational Program (OLSP) is started by sending a START LOAD pulse followed by a LOAD COMPLETE. Program control transfers to location 010000.

NOTE: START LOAD is the S/C commands LOAD PROCESSOR LOW - LOAD PROCESSOR HIGH

LOAD COMPLETE is the S/C command LOAD PROCESSOR COMPLETE.

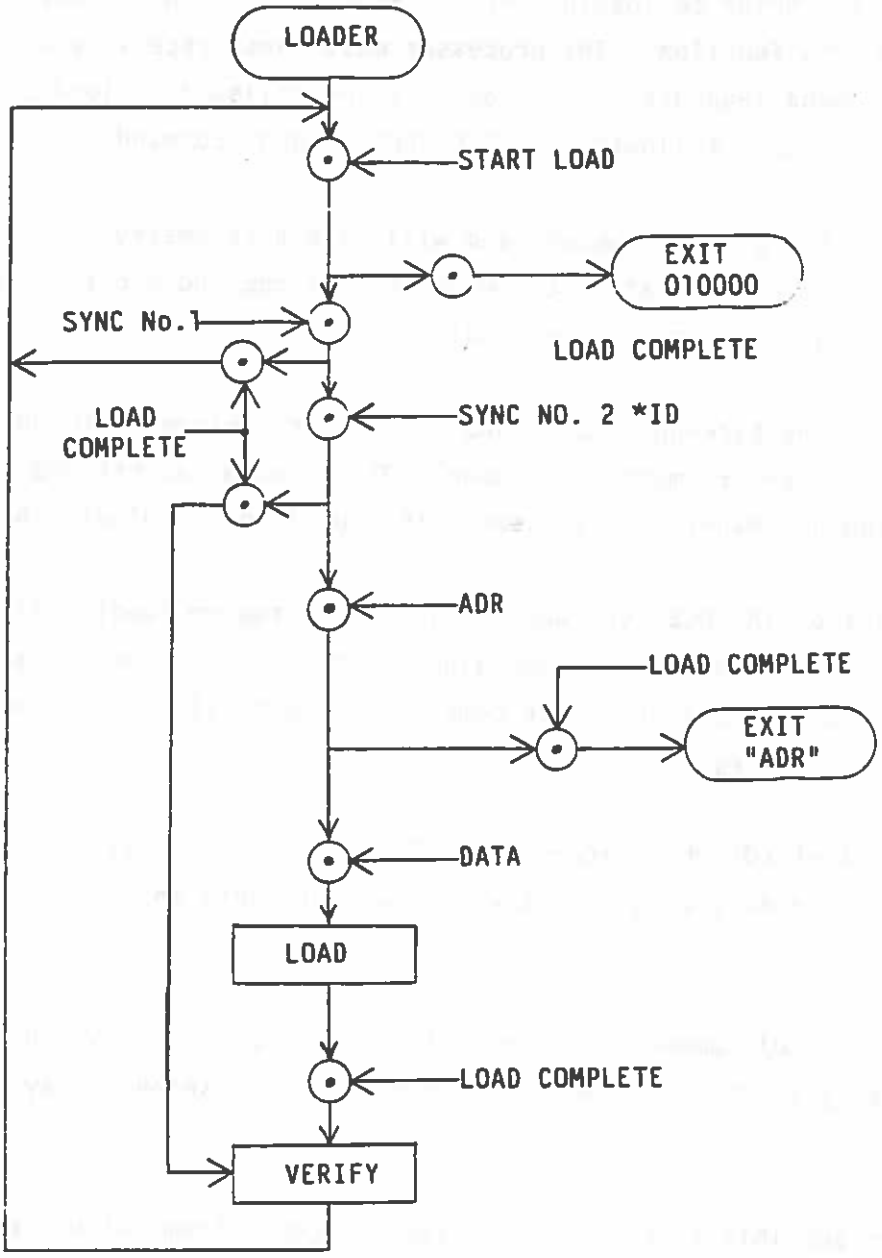
The program can also be started at any desired location "ADR" by sending the sequence: START LOAD, HEADER, ADR, LOAD COMPLETE. The following starting addresses may at times be useful. Refer to the correct program listing for the address associated with the labels.

I3INIT	Initialize OLS to primary side and start OLSP
I3IRED	Initialize OLS to redundant side and start OLSP
I3BYPS	Restart OLSP without re-initialization
E6CALC	Recompute stored checksums
L1LOAD	Idle
L1DUMP	16K reverse dump. Header supplied by uplink

2.7 Loader Flow Diagram

The LOADER exit is made to absolute address 010000 (location 000 of block 020) or location ADR. What has been loaded into this location would normally be the operational program initialization routine. It could also be a special program to perform some unanticipated function or diagnostic program. There are many kinds of diagnostic programs which could be written to test out all or any portion of the OLS system (i.e., processor, memory, I/O, formatters SSS, SPS, PR's, DT's, etc.). Because the loader requires exclusive use of COMDAT and MDDATA, commands to, and OLS CPU telemetry from, the other processor will be disabled during a load and/or verify sequence. A simplified block diagram of the LOADER appears below.

Simplified Loader Flow Diagram



3. FIRST ORBIT TELEMETRY

The capability exists for recording telemetry during the first orbit after handover (prior to loading the OLS Program). Either processor C or D can perform this function. The processor must first receive a S/C load processor command sequence (load processor low followed by load processor high). This is then followed by a S/C PFOT or BFOT command.

PFOT is the primary command and will record telemetry in SDS format on PR 1 using I/O X and formatter G. When PFOT is commanded off PR1 will playback at high speed on channel 1 DT1 clear.

BFOT is the back-up command and will record telemetry in SDS format on PR3 using I/O Y and formatter H. When BFOT is commanded off PR3 will playback at high speed on channel 2 DT2 clear. If PFOT is on, BFOT will be ignored.

Receipt of the OLS sync word (prior to a program load) will terminate the first orbit telemetry by commanding off PR's, DT's, and formatters. Receipt of the S/C load processor complete command will also terminate the first orbit telemetry.

Receipt of EOT when recording or BOT in playback will not terminate the first orbit telemetry program but will power off PR's and DT's to conserve power.

Multiple FOT commands can be sent for multiple records and playbacks. A 5 second delay exists prior to each record and a 10 second delay prior to each playback.

It is possible to enter an OLS load sequence from FOT by sending the header, address, and program data without a new S/C load processor command sequence.

The following table lists the commanding possiblities.

CMD1 -FOT-	CMD2-4	CMD5	CMD6	CMD N	Function
LP	HDR	ADR	DATA	LPC	Load & verify
LP	HDR	LPC			Verify
LP	LPC				Start loaded program @ 010000
LP	HDR	ADR	LPC		Start program at "ADR"

where LP = S/C load processor command sequence, will always reset processor to location 0.
LPC = S/C load processor complete command.
HDR = OLS SYNC SYNC ID
ADR = OLS Address word
DATA = OLS Program data words

CMD1 will always reset the OLS to the loader.
CMD2 will terminate first orbit telemetry function if it was on.

Multiple S/C PFOT (BFOT) ON/OFF Commands can be sent at any time between CMD1 and CMD2 in the table. FOT Commands will be ignored by the OLS at all other times. The exception to this is that a PFOT ON/OFF sequence will reset a MAC load sequence (see section on Real Time commanding).

4. UPLINK COMMAND DESCRIPTION

Appendix A contains the formats for all 16 uplink commands (000-017). The general format for these commands appear below.

BIT POSITION

16	15 14 13 12 11 10 9 8	7 6 5	4 3 2 1
P	DATA	SUB	CMD

Bit 16 is the MSB and is the first bit transmitted. Bit 1 is the LSB and is the last bit transmitted. the basic command number (000-017) is placed in bits 1-4. Bits 5-7 usually define a sub-command of the basic command. Bits 8-15 are used for data or for further definition of the sub-command. Bit 16 is the parity bit and is set to a state such as to provide an odd number of set bits (logic "1") in the entire 16 bit word.

When a function is named in the command formats, the name applies when the corresponding bit is set to a logic "1". For function names of the type A/B, function A applies when the corresponding bit is set to a logic "1" and function B applies when the corresponding bit is set to a logic "0".

CMD00-GNC-Gain Control

The command is used for controlling the gain of the L and T sensors. Bits 5-8 (4 bits for this command) define a particular sub-command of the GNC command.

Sub-command 0 itself has sub-commands 0-7. Sub sub-commands 0, 6 & 7 select a gain for the T sensor, the gain value being defined in bits 12-15 with the LSB in bit 12 representing 0.16 dB. Sub sub-command 1 selects a level shift at 210°K for the T sensor, the shift being defined in bits 12-15 with the LSB in bit 12 representing 1.02°K shift. Sub sub-command 3, 4 and 5 are segment selects for the T, HRD, and PMT sensors respectively. The segment mode is specified in bits 12-15 where "A" represents automatic mode in which the segments are automatically selected by the operational program. If "A" is set, the remaining mode bits are ignored. If "A" is not set, the segments are selected according to the L, M, and R bits for left, mid, and right segments. These bits can be set in any combination; however, they have an effect only during active scan (|scan angle| < 56.25°). During overscan (|scan angle| $\geq$ 56.25°), the operational program always uses the pre-programmed segment selects. Sub sub-command 2 is a spare. Sub-command 0 becomes effective at the time the command is executed.

Sub-commands 1-7 command the gain mode of the L sensor (Along Scan Gain Control, Along Track Gain Control, Preset Gain Control). Bit 9 selects the state of the LOG/LIN amplifier where a "1" selects log state. For the preset gain modes, bits 10-15 select the gain of the VDGA. These sub-commands do not become effective until positive End of Scan (EOS).

Sub-command 010 commands slope and bias adjustments to the GVVSSE curve. These adjustments do not become effective until positive EOS. The slope command is not implemented in OLSP Rev K and up.

Sub-command 011 enables/disables the BRDF computation (OLSP Rev K and up). The OLSP initializes the BRDF to enable both specular (R_s) and diffuse (R_v) components.

Sub-commands 012-017 are spares.

CMD01-RTR-Real Time Readout

This command controls the readout of real time data. Sub-command 0 puts the Real Time Data Formatter (RTDF) into operation and connects the data stream for transmission of real time data. Sub-commands 1-7 are spares.

Bit 8 defines the ON or OFF status of the command and bits 10-11 select which channel to turn on or off. Bit 12 selects the text of the data to be clear or encrypted. Bit 13 selects the data type to be TF/LS data or LF/TS data. Bit 14 specifies whether or not to enable the Direct Mode Data Message.

Consecutive ON commands may be given in order to connect the RTDF to any number of channels. Consecutive ON commands may also be given to change the data type, state of the DMDM bit, or the clear/encrypt state of the text.

An OFF commmand will turn off only the channel specified. If the RTDF is still connected to another channel, that channel will remain in operation and if DMDM had been specified by another channel command, the DMDM would remain active.

If a command is given to use a channel that is already in use by a recorder, that command will be rejected. If a command is given to turn off a channel that is not connected to the RTDF, that command will be ignored.

When an ON command is received and the particular transmitter connected to the channel if off, it is turned on for a 10 second warm-up prior to enabling the RTDF. During a transmitter warm-up, no other transmitters are turned on. Any commands received during this warm-up period are therfore delayed if they command a transmitter on.

CMD02 - Spare

CMD03 - SDC - Stored Data Control

This command is used for control of the stored data modes. Bits 5-7 equal to 0 or 5 are for test of the record mode without specifying a recorder. Bits 5-7 equal to 1-4 specify recorder 1-4. Bits 8-9 specify whether the command is OFF, RECORD, PLAYBACK or FAST FORWARD. For record commands, the source of the data is specified in bits 10-11 as either the SDF or SDS formatter. For playback commands, bits 10-11 define the channel destination of the data. Bits 12-13 define the data type for SDF record commands. For playback commands, these bits define the text of the data to be clear or encrypted and define the tape playback speed.

The tape playback speed should be selected according to the bit rate desired.

Tape Speed	Bit Rate
High	2.66 MBITS/SEC
LOW	1.33 MBITS/SEC

The action taken by a record command is to connect a formatter to a recorder. That formatter may be specified by another record command selecting another recorder. In this case, the one formatter will supply data to any number of recorders specified. Once a connection has been made to a recorder, the speed of the recorder is fixed even if another record command changes the formatter's data type.

A playback command will first insure that the selected transmitter has been on for 10 seconds, turning it on if required, then connect and playback the recorder.

A fast forward command will advance it to end of tape at high speed.

Off commands will turn off the recorder and the channel it was connected to for playback. For record, the recorder is turned off and also the formatter if the formatter is not in use by another recorder. An automatic off command will be performed when encountering EOT during Record or Fast Forward and BOT during playback.

If either the recorder or channel is already in use, the command will be rejected. If the recorder has not been off for at least five seconds, the command is delayed until it has been off for five seconds.

CMD04 - RLC - Recorder Location Counter

The RLC command is used to set the primary recorder (1-4) location counter specified in bits 13-15 to the value specified in bits 5-12. A range of 0-2048 in steps of 8 feet can be specified.

CMD05 - Spare

CMD06-TBC-Transmitter/BBT Control

The TBC command is a back-up command and need not normally be used. It may become useful for getting around some of the failure modes of the system.

Sub-command 0 selects the channel to DT connection. Normally channel 1 connects to DT1, channel 2 connects to DT2, etc. Interlocks are provided so that one channel connects to only 1 DT.

Sub-command 1 turns ON or OFF the selected DT. Sub-command 2 sets or resets the selected DT interlock. If the interlock is set, the selected DT is turned off (the data and channel using that DT are unaffected). Once the DT is interlocked, it cannot be turned on by this or any other command until the interlock is reset.

Sub-command 3 selects the power to the selected BBT, thus once a channel has been set up by the RTR or SDC commands, this command may be used to change the text of the data. Sub-commands 4-7 are spares.

The usual 10 second DT warm-up interlocks are used where applicable.

CMD07-PSC-Primary Sensor Control

The PSC command is for miscellaneous primary sensor functions which are normally commanded a few times.

The PMT power, T channel cone cooler heater, scanner, IMC and encoder pulse simulator can be enabled or disabled. Scanner A should be used if DMEA is selected. Scanner B should be used if DMEB is selected.

The encoder pulse simulator command is useful to provide pulses for formatting the telemetry and mission sensor data if a problem develops in the encoder or scanner. The simulator can be locked to the scanner or commanded to free-run.

The scanner protect command will enable or disable scanner protection. If scanner protection is enabled, bit 9-14 of the command define the number of delphi counts above 1024.5 at which the scanner should be turned off if its amplitude equals or exceeds this value. The program initializes to scanner protect enabled with an amplitude limit of 1050.5 delphis.

The SPU controls command is used to control the solenoid mechansim.

CMD010 - LDC - Location Data Command

The LDC command normally comes from the spacecraft location data interface although it can be executed as a normal OLS command.

Subcommand 0 is the Phase 2 Load Shed command and will turn off the scanner and PMT unless the OLS is operating in the autonomous mode in which case the command is ignored.

Subcommand 2 contains two commands depending on the bit configuration of bits 8-15. The Phase 1 Load Shed will turn off both main and orbit stored programs, mission sensors, data transmitters, encryptors, T-channel cone cooler heaters, and all recorders except SDS record. The processor status word E2 bit will be set. During autonomy, the Phase 1 Load Shed will instead turn off all recorders and mission sensors and set the E2 bit. RTD will continue encrypted on DT1 and DT3 and the orbit memory continues.

The remaining subcommand 2 is the autonomous mode command. It will turn off main memory, T-channel heater, all records and playbacks except SDS record, all transmitters and encrypters except RTD DT1 & DT3. It will switch on the autonomous mode DMDM, command the mission sensors according to the preferred state table, and enter the autonomous mode.

CMD011-SSC-Mission Sensor Control

The SSC command provides control over the mission sensors. Subcommand 0 defines the on/off state of a sensor. Sub-command 1 and 2 define the state of the mode 1 and mode 2 control lines. A logic "1" for the sensor defines ON state for 2 state sensors and step to next state for 3 or more state sensors. A logic "0" for the sensor defines OFF state for 2 state sensors and hold current state for 3 or more state sensors. The type of sensor is specified in page 0 of the uplink memory (the uplink memory is discussed in a later section). Sub-command 3 transmits an 8-bit control word to a selected sensor. Sub-command 4 defines the 8-bit control word. The control word must be established by sub-command 4 before sub-command 3 is executed. Multiple sub-command 3's can be executed without intervening sub-command 4's to send the same control word to different sensors.

CMD012-SGN-System Generator

The function of the SGN command is to connect up the various primary and redundant functions.

Sub-command 0 is used for redundant function control. A logic "1" in bit 8 selects the redundant function and a logic "0" selects the primary function. The exception is select code 5, Vacuum/Air DME pulse width.

Sub-command 1-7 are spares.

CMD013-OCP-Orbit Clock Preset

The OCP command is used for setting a value into the orbit clock. The clock is preset when the command is executed. Three sub-commands are defined.

Sub-command 0 causes the orbit clock to be set to 0.

Sub-command 1 defines an address in page 0 of the uplink memory which contains the value to which the orbit clock should be set.

Sub-command 2 contains the value the orbit clock should be set to.

Sub-command 3 defines the number of half second increments to be added to the orbit clock from -64.0 to +63.5 seconds.

Sub-command 4 defines the number of minutes to be added to the orbit clock from -128 to 127 minutes in steps of one minute.

CMD014-UPC-Uplink Program Control

The function of the UPC command is to turn on or off the stored uplink programs or to put the main program in STANDBY.

Sub-command 0 is used to turn off the Main and/or Orbit Memories. Subcommand 1 specifies the starting address within a page. This sub-command must be sent prior to the page command. Sub-command 2 specifies the starting page and also turns on the memory (Main or Orbit) in which the uplink address lies. Sub-command 3 puts the Main Memory in STANDBY until either a Main Program on command is received or the Elapsed Time Count decreases in value by at least 2 seconds. Sub-commands 4-7 are spares.

CMD015-MAC-Memory Access Control

The purpose of the MAC command is to load or dump memory. Either the uplink memory, the operational program memory, the OLS telemetry channel assignments, mission sensor preferred state table, autonomous mode DMDM table, special ancillary data table, or a mission sensor program memory can be specified.

There are always three types of MAC commands required for load or dump operations. The first type is the MAC word count command. This command specifies the number of 16 bit words to load or dump. The word count field can contain any number from 0 to 1023. For uplink memory page or OLS memory block, a count of zero will be interpreted as a 1024 word load or dump. For OLS CPU telemetry table loads or dumps word counts in the range of 2 to 37 (for up to 36 channels plus the ID word) are valid. For mission sensor memory loads (dump are not available except via primary data formats) the valid range is 0 - 1023 specifying the lower order 10 bits on the mission sensor load length.

The second type of MAC command is the MAC address for uplink memory page or OLS memory block loads or dumps. The valid range of address is 0-255. For CPU telemetry table loads or dumps, this command is interpreted as a MAC channel number command where the channel number has a valid range of 1-36.

For mission sensor memory loads the command is interpreted as a MAC word count extended command where the word count extended = load length/1024. The maximum load length is 32767 words. For other tables the address is referenced to the start of the table.

Command types one and two can be sent in any order and can be repeated as often as desired; however, they must both be executed prior to sending the third MAC command type.

The third type of MAC command is the MAC load or dump and is the command which starts the indicated action. For uplink memory page load or dump the page (0-7) must be specified. For OLS memory block load or dump the block (0-63) must be specified. For mission sensor memory loads the mission sensor ID (1-12) must be specified. The field specifier for other loads or dumps defines the table (CPU telemetry, mission sensor preferred state, autonomous mode DMDM, special ancillary data).

For MAC dump command sequences the dump data will appear on the S/C MDDATA interface preceded by a header identifying the type of dump data.

The MDDATA interface is also used to echo the load file, preceded by a header defining load type, for MAC load command sequences. For most load types an odd parity bit must be supplied in bit 16 of the load file. For the load file echo this bit (bit 16) will indicate zero for odd parity received and one for even parity received. For block loads and mission sensor memory loads bit 16 is an information bit and not a parity bit and will be echoed as uplinked.

The load file for page and block loads consist of the load data destined for the page or block. For CPU telemetry table loads the load file consists of the new channel addresses preceded by the new CPU telemetry table ID. Bits 1-9 of the ID word can be specified to any value desired for configuration management puposes. The load file for mission sensor memory words consists of the following:

Word 1 Configuration number
2 Address of Data 1
3 Number of Data words (N)
4 Control Checksum

```
  5   Data 1
  6   Data 2
  |
  |
N+4   Data N
N+5   Block Checksum
```

where the load length = N+5, the control checksum is over words 1-3, and the block checksum is over words 1 through N+4. The checksums are computed using the algorithm defined in the next paragraph.

A checksum will be computed on each load file (for all MAC load types) and downlinked via MDDATA after the load is complete. The algorithm for checksum computation is as follows

```
    CKSM = 0
10  INPUT COMDAT
    WORD COUNT = WORD COUNT-1
    IF(PAGE OR CPU TLM LOAD)
       Then
           COMDAT B16 = 1 FOR EVEN PARITY
           COMDAT B16 = 0 FOR ODD PARITY
       Else CONTINUE
    DOWNLINK COMDAT VIA MDDATA
    CKSM = CKSM + COMDAT
    CKSM = CKSM SHIFTED RIGHT CYCLIC ONE BIT
    IF(WORD COUNT NOT EQUAL TO ZERO) GO TO 10
    DOWNLINK CKSM VIA MDDATA
```

For mission sensor loads, the OLSP also compares the checksum for the first N+4 words against the N+5th word (block checksum) and initiates a system error message if not in agreement.

CMD016-AIS-Auxiliary Instruction Set

The purpose of the AIS command is to give the uplink program decision capability and to allow it to be changed dynamically. Two 3 bit page registers and 15 bit accumulators are provided. One set for orbit memory and one set for main memory usage. The page register is used to form the effective address for memory reference instructions. Operations are performed on the 15 bit accumulator using two's complement arithmetic with the sign bit in bit 15. Fifteen commands have been defined and there are three spares as listed below:

Sub-Command	Name	Description
0	CLEAR	Clears the Page Register and/or Accumulator to zero.
1	LOAD	Loads the contents of the effective address into the Accumulator. The effective address is defined by the address field of the instruction and the current value of the Page Register.
2	STORE	Stores contents of Accumulator into the effective address.
3	ADD	Adds contents of the effective address to the Accumulator.
4	SUBTRACT	Subtracts contents of the effective address from the Accumulator using two's complement arithmetic.
5	JUMP	Jumps to the specified address within the page where the jump command is located.
6	NO-OP	No operation.
	TLZ	Skip next instruction if Accumulator (AC) is less than zero.
	TEZ	Skip next instruction if AC equals zero.
	TLEZ	Skip next instruction if AC less than or equal to zero.
	TGZ	Skip next instruction if AC greater than zero.
	TNZ	Skip next instruction if AC not equal to zero.
	TGEZ	Skip next instruction if AC greater than or equal to zero.
	SKIP	Unconditionally skip next instruction.
7	SETP	Set Page Register to value specified.

Sub-commands 5 and 6 cannot be executed as real time commands.

CMD017-SPC-Special Purpose Commands

This command contains a set of special purpose commands which are used for real time commanding and real time trouble shooting purposes. Many of the sub-commands call for a dump of a certain functional area of memory without having to compute address and word count. The MDDATA interface is used for dumps. All dumps are preceded by a header defining dump type.

Sub-command 0 is a NO-OP, performing no operation.

Sub-command 1 calls for a dump or dumps of various uplink areas. Included are the operational constants and GVVSSE table in page 0, the Main memory, Orbit memory, DMDM memory, mission sensor preferred state table, autonomous mode DMDM, and special ancillary data.

Sub-command 2 calls for a dump of a processor memory block.

Sub-command 3 calls for dumping the status of the input or output selects of the processor. A close knowledge of the software is required for best use of this command as some of the output selects are not available exactly as output to the system. Also certain inputs may cause a slight effect in the system (i.e., inputting the real time clock may cause the loss of up to 5 milliseconds in time).

Sub-command 4 calls for various status dumps from the program. Included are the processor status word, checksum error table, system error table, main program address counter and status, orbit program address counter and status, sampled elapsed time count, processor status error time code, and OLS telemetry table.

Sub-command 5 is a spare.

Sub-command 6 clears out the selected status word, error tables, or initialization count in the processor status word.

Sub-command 7 is an Execute. This command is required for non-command authenticate real time command execution which will be discussed in a later section. The Execute command has a bit associated with it which overrides the effects of command parity errors.

5. UPLINK MEMORY DESCRIPTION

Appendix B contains a diagram of the uplink memory. The memory is composed of 2048 words which is broken into 8 pages (page 0-7) of 256 words (000-0377) each. The memory consists of four main sections, operational constants, GVVSSE memory, stored program, and Direct Mode Data Message (DMDM). The operational constants contain constants and variables required by the operational program. The stored program consists of the Main program and the Orbit program.

5.1 Operational Constants

The operational constants are located in addresses 000-0110 of page 0. Addresses 000-064 are reserved for DMCC element usage. Addresses 065-0110 are used by PSCC program elements. Bit 16 of each location in page 0 is always forced to a 0 when stored.

The OLS processor status word is located in address 000. This word can be set to zero from the ground. Bits 12-15 contain a count of the number of times the processor was intitilized since the last time of memory power loss. This number will count modulo 16. The error bits E1-E3 are defined below. Once set, they stay set until reset by the ground.

E1 - memory checksum error
E2 - shed OLS power command
E3 - system error table entry

Bits 8-11 identify the program version. The revision of the program is located in bits 4-7.

Location 001 is used to indicate recorders which should be excluded from the autonomous mode PR cycling. Bit 1 marks PR1 as bad ... bit 4 marks PR4 as bad.

Locations 010-012 contain information to define the boundaries of the dynamic memory in pages 1-7. The addresses are absolute addresses in the range 0400-03776. The Orbit Memory starting address and DMDM starting address must be an even address. The DMDM length refers to the number of words in memory which means the number of DMDM characters divided by 2.

Locations 013-036 are reserved to hold preset values for the Orbit Memory reference clock.

Locations 037-040 define the type of the mission sensors A-L mode 1 and mode 2 control lines. A logic "1" defines the sensor as a pulsed type and a logic "0" defines a two-level type.

Locations 041-054 define the sampling format and order for the mission sensors A-L (select codes 001-014). Any sensor can be specified in any slot. The sensor selected in slot 041 will be sampled first. The T/L bit defines in which data stream the sampled data is to be placed. The sensors dedicated to the L data stream (there must be at least one even if its an all zero dummy word) should be specified prior to the T data stream sensors and they should not be intermixed. Bits 6-13 define the number of bits divided by 36 which are to be sampled by the specified sensor.

Location 066 bit 1 is the inhibit bit for correcting data sampling for scanner offset. If this bit is a logic "1" there will be no new corrections for the scanner offset. When the bit is set to a "0" continuous offset corrections will be allowed.

Location 067 contains the 4-bit vehicle identifier and the direction bit. If the direction bit is a logic "1", the S/C is traveling in the -Y direction. If the direction bit is a logic "0", the S/C is traveling in the +Y direction. This bit is used to apply the correct phase to the Image Motion Compensation.

Locations 071-077 define the VDGA points at which the L sensors are to be switched and to define the VDGA offset in each region. Appendix C contains a curve of Sensor Gains and Switch Points showing the four regions of operation, i.e., HRD, PMT 1/9, PMT LOW, and PMT HIGH.

The region of operation is determined by the 3 switch point parameters SWPT1-SWPT3 (S1-S3). The gain represented by the sensor to be switched in is represented by the 3 gain parameters GAIN1-GAIN3 (P1-P3).

VDGA zero offset is represented by the HRD offset (PO) parameter.

Sensor switching will take place at the defined switch points ± SWPT DELTA. The SWPT DELTA is defined in location 0100 and has a nominal value of 1.5 dB.

Location 0103 is reserved to hold the gain to be placed in the VDGA during calibration of the PMT in -Z overscan.

Location 0101 is reserved for PDELBS which is used for centering the encoder simulator about NADIR. Location 0102 contains PDELSP which is used to reduce the encoder simulator DOS spread. The values stored are 15 bit two's complement numbers with the LSB representing 1.878 microseconds.

Location 0104 contains the maximum allowable GVVSSE gain to be used in ASGC and ATGC modes.

Location 0105 contains a lunar gain bias value which is added to the lunar portion of the GVVSSE/GVVSLE gain value only, whereas the HRD offset is added to both portions of the GVVSSE/GVVSLE gain.

Location 0106 contains a multiplicative factor on the specular component of the BRDF when the HRD detector is selected.

Location 0107 contains a multiplicative factor on the specular component of the BRDF when the PMT detector is selected.

Location 0110 contains a multiplicative factor on the X^2 term in the specular component of the BRDF.

All locations not discussed through location 0110 are spares and can be used for any purpose desired.

5.2 GVVSSE Memory

Gain Value VS Scene Solar Elevation (GVVSSE) is located in uplink memory page 0 addresses 0237-0376. Gain values are stored for each angle from -15° to +80° with the 0376 value duplicated in location 0377. Gain Value vs Scene Lunar Elevation (GVVSLE) is located in uplink memory page 0 addresses 0112-0237. Gain values are stored for each angle from +80° to -5° with the 0112 value duplicated in address 0111. Bit 16 is always forced to a 0 when stored.

5.3 Stored Program

The stored program area of the uplink memory is located in pages 1-7 (absolute address 0400-03777) and can be divided into 2 sections, Main Memory and Orbit Memory. The boundary between the two sections is flexible since it can be defined in locations 010 of page 0.

5.3.1 Main Memory

The Main Memory always starts at address 000 of page 1 (absolute address 0400) and contains the Main Program. The Main Program contains commands in the even address locations and time tags in the odd locations. These commands are executed when the associated time tag equals the Elapsed Time Clock (ETC). The ETC is reset at least once per day. If either the command or time tag was received from the ground with incorrect parity, bit 16 will be set equal to "1"

5.3.2 Orbit Memory

The Orbit Memory contains the Orbit Program and always starts with a command in an even location. Time tags are stored in odd locations. The commands are executed when the time tag equals the Orbit Clock (OC). The OC can be changed via real time or stored commands and is usually reset once per orbit. In this way the Orbit Program is cyclic on an orbital basis. Bit 16 is used to hold the parity correctness of the commands and time tags.

5.4 DMDM Memory

The DMDM is stored in the memory following the Orbit Memory and always starts in an even address as defined in location 011 of page 0. It is composed of 2, 6-bit ASCII characters per word where D1 is the first character, D2 is the second character, etc. The word length of the DMDM is defined in location 012 of page 0.

There is a separate 46 word table for holding a message which will be used when the OLS swtiches to the autonomous mode. The format of the Autonomous Mode DMDM is identical to the normal DMDM except that it is a fixed length of 92 characters. The table is loaded via the MAC commands.

6. REAL TIME COMMANDING

Real time commands are received via the COMDAT S/C interface line. There are two OLS modes associated with uplink commanding, 1) command mode, 2) data mode. Command mode is used for executing commands. Data mode is used for storing information into memory as a result of executing a MAC LOAD command.

6.1 Command Mode

If the S/C ACCEPT pulse is received the previous COMDAT will be executed if it was received with odd parity, if it was an EXECUTE command, or if the PARITY OVERRIDE was on; otherwise it will be rejected and placed in the system error table. If the S/C ACCEPT pulse is not received but the S/C REJECT pulse is received, the command will be rejected.

Following command execution or rejection, the command will be placed in the 20 word CV buffer with the processor ID (1=D, 0=C) in bit 16. If the command was rejected bits 1-15 of the CV will be complemented. This buffer will be downlinked CVDATA as the S/C permits. If the buffer is full, COMDAT is placed in the system error table uncomplemented and bit 16=1 indicates a rejection due to parity or REJECT.

6.2 Data Mode

If COMDAT was received with even parity, bit 16 will be set prior to downlinking via MDDATA and storing COMDAT in memory unless the data mode was the result of a MAC LOAD BLOCK or MAC LOAD Mission Sensor command in which case there is no parity associated with COMDAT.

There are no S/C ACCEPT or REJECT pulses in data mode since all the data loads are non-authenticated. Data loads will still be accepted in the authenticate mode; however, in this case an unsolicited NO-OP CV (000017) will be produced at the end of the load.

Data mode is terminated normally by satisfying the word count of a MAC load command sequence. If there are problems in the uplink such that the word count is not satisfied, a PFOT record, PFDT playback command sequence will terminate the MAC load and cause the OLSP to go back to command mode.

6.3 Systems Not Using Command Authenticate

There are no ACCEPT or REJECT pulses. Commanding in both OLS modes require that CAP be set. In order to execute in command mode each COMDAT must be followed by an EXECUTE command. Both COMDAT and EXECUTE must have been received with odd parity or the parity override command must be on in order to execute COMDAT. The EXECUTE will set the state of the parity override even if it was received with even parity. If the command is not executed it is placed in the system error table with bit 16=1. CVDATA will always contain both the command and the execute with bits 1-15 complemented for bad parity received and the processor ID in bit 16.

7. STORED PROGRAM COMMANDING

Commands may be stored in the Main Memory or Orbit Memory for delayed execution. Each command must be stored with a time tag (TTG). Commands must be stored in even addresses and time tags must be stored in odd addresses. Main Memory time tags have a 4 second LSB. Orbit Memory time tags have a 1/2 second LSB. The command will be executed when the reference clock equals the time tag.

The Elapsed Time Clock (ETC) is the reference clock for the Main Memory TTG's and is reset by the S/C once per day near 2400 hours ZULU. The Orbit Clock (set by an OCP command) is the reference clock for the Orbit Memory.

Both the command and its TTG must have been loaded with correct parity for it to be executed unless the parity error override is on. The state of the parity error override is set by the last execute uplinked.

Up to 10 commands may be executed having the same TTG value. Commands with bad TTG's will not be executed where a bad TTG is one which has a value less than the reference clock when retrieved from memory.

Some commands do not execute or are executed differently from memory. The following commands will not execute from memory:

CMD015	MAC	Memory Access Command

The only action of an execute command in memory is to set the state of the parity error override.

8. SOFTWARE INTERLOCKS

The following interlocks are provided by the operational program:

1. Power to a DT will be enabled for 10 seconds before data to the DT is enabled.

2. DT's will not be enabled within 10 seconds of each other.

3. The priority for enabling waiting DT's will be DT1-DT4 for the TBC command followed by CH1-CH4 for the RTR and SDC commands.

4. A single channel will be connected to a single DT.

5. If a DT has been interlocked (disabled) it will not be enabled, however, data may still be connected to the channel.

6. A channel or PR will be connected to only one data source.

7. A formatter may be connected to any number of PR's or channels.

8. A PR will be connected to only one channel.

9. Ir a PR is commanded on, it will not be turned on until 5 seconds have elapsed from the time it was turned off.

10. After a PR has been turned on, it will not respond to anything other than an OFF command,

11. If a command and/or its associated execute (or time tag) had a parity error when it was originally uplinked it will not be executed unless the parity error override is on.

12. If a stored command has a bad time tag it will be skipped (not executed).

13. Memory access commands will not be executed from memory.

14. Real time AIS (CMD016) Jump of Skip commands will not be executed.

15. Main Memory Standby (CMD014) will only be executed from main memory.

16. The LDC (CMD010) and SSC (CMD011) commands are the only commands which will be executed via the S/C LOCDAT interface.

9. MISSION SENSOR PROGRAMMING

Mission sensor (MS) data is placed in the RTD and SDS line formats. In order to properly control the sampled data there are uplink constants in uplink memory page 0 required and there is a real time command available.

Provisions have been made for up to 12 mission sensors. These sensors are sampled at the rate of 1 sample per second per sensor. The number and ordering of sensors sampled along with how many bits to sample from each sensor is defined in the MS format control words in uplink memory page 0. The destination of the data, L or T data stream, is also contained in the MS format control words. MS FMT WD #1 contains the sampling information for the first sensor sampled and must specify the L data stream. MS FMT WD #2 contains the sampling information for the second sensor sampled, etc. The sensor data to be directed to the L data stream must be sampled prior to the sensor data to be directed to the T data stream and should therefore be programmed first (lower number MS FMT words) in uplink memory. The two types should not be intermixed.

Two other words in uplink memory must be specified in order to define which sensors are of the pulsed type. These are the MS type words. The formats of these words in uplink memory have been described in an earlier section and can also be found in Appendix B. The type words should be set up prior to use of any sensor mode commands. If the type words are changed for any reason, the mode lines should be set to hold for all sensors to be defined as pulse before the type word is changed.

The SSC command (CMD 011) will turn on or off the sensors. The command will also select the state of the mode 1 and mode 2 control lines and 8 bit data going to each sensor.

The RTR command (CMD01) or the SDC SDS record command (CMD03) will initiate MS processing. The processing will continue until both commands are turned off.

The MAC command (CMD015) can be used to load a mission sensor memory. The OLS commanding (a particular mission sensor may have additional protocol) and load format is described in section 4.

The minimum bit capacity of the various formats for special sensor data including 288 bits of overhead are:

SDS L 2088 bits per second

SDS T 3816 bits per second

RTD 5252 bits per second

Provisions have been made to command mission sensors to a preferred state when the autonomous mode is entered. For this to take place the mission sensor preferred state table must have been previously loaded via MAC commands. The table can contain up to 50 entries containing SSC commands and an end of table flag (80FF).

10. ERROR ANALYSIS

In addition to the telemetry there is software supplied information which can be used for analysis of vehicle performance.

10.1 Command Verification

Each real time command received is placed in a 20 word CV buffer and downlinked via the CVDATA S/C interface at one word per PIP frame for command verification purposes. If the CV buffer becomes full, the excess commands are placed in the error table where they can be examined if desired. CVDATA is also flagged to indicate the parity correctness of the received command and to indicate processor ID.

10.2 Memory Load Verification

Memory loads are downlinked via the MDDATA S/C interface for verification purposes. In addition a parity error bit is supplied in bit 16 unless the memory load consists of processor data (program, block, or mission sensor loads). Following the memory load a checksum is downlinked via MDDATA to indicate the correctness of the load.

10.3 Digital EST Points

The software outputs the following EST information in the form of an EST status word. The bits have the meaning shown. The information is available as EST points and also by sending a SPC Status Command (CMD017) which will cause a dump of the EST status word via MDDATA.

EST STATUS WORD BIT	EST POINT	DEFINITION
1	74	2^0
2	74	2^1 PSTATE
3	74	2^2
4	130	PROCESSOR STATUS WORD ERROR
5	129	MAC LOAD
6	116	BRDF RS D8 TS 0
7	116	BRDF RV D8 TS 1
8	116	SPARE D8 TS 2
9	116	SPARE D8 TS 3
10	116	SPARE D8 TS 4
11	116	SPARE D8 TS 5
12	116	SPARE D8 TS 6
13		SPARE
14		SPARE
15		SPARE
16		SPARE

10.4 Processor Status Word

The processor status word has been described in the section dealing with uplink memory. The error bits in the processor status word are repeated below:

E1 - memory checksum error

E2 - shed OLS power command

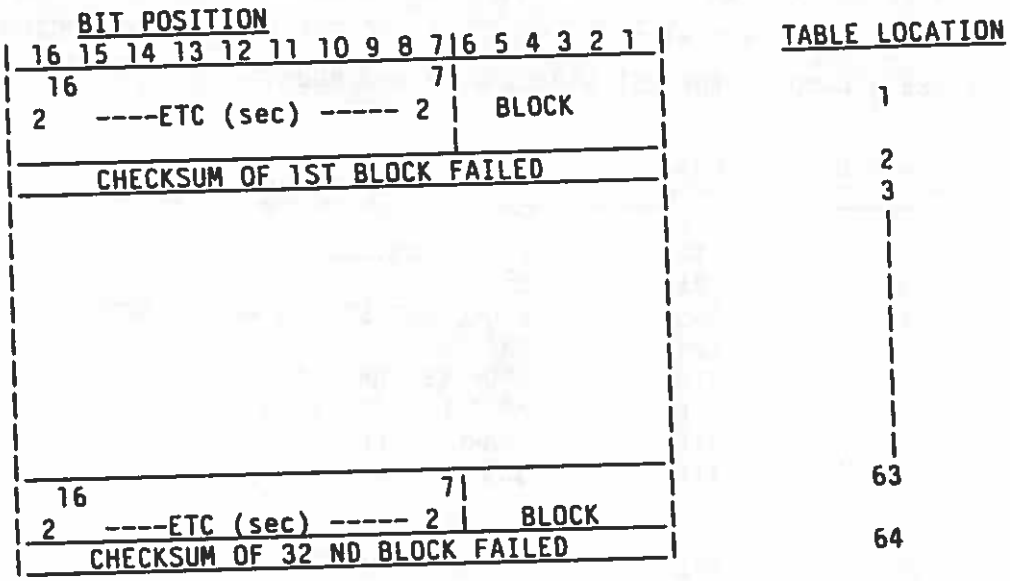
E3 - system error table entry

In addition the program version, revision, and initialization count are included in the processor status word. This count is the number of times the program was intialized since the last time memory has been powered down.

If the E1 bit is on, further information can be obtained by checking the checksum error table. If the E3 bit is on further information can be obtained by examining the system error table.

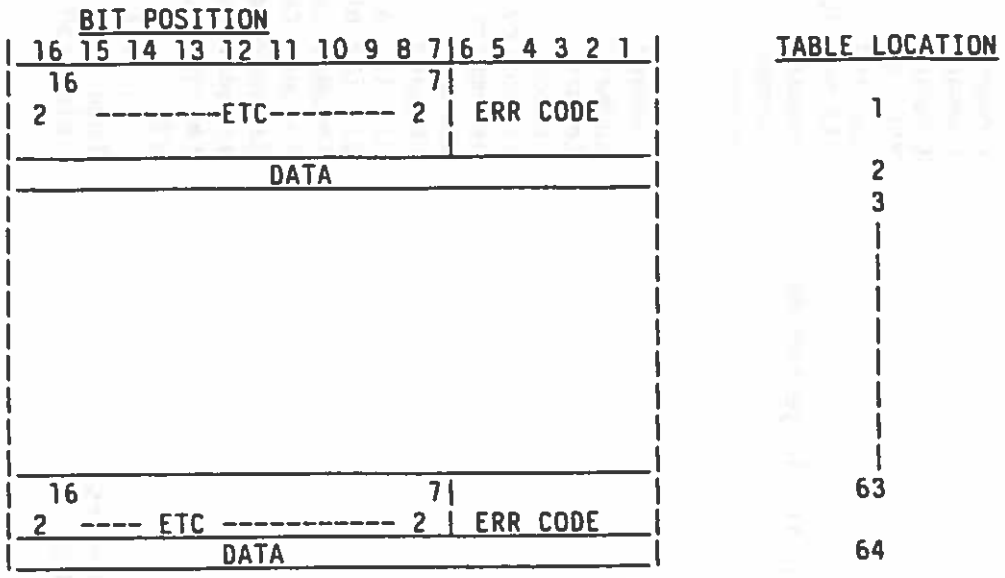
10.5 Checksum Error Table

When the processor status word indicates a checksum error, the memory block with the error is stored in the checksum error table along with the computed checksum and elapsed time count. When the table becomes full, new errors write over the last location. The errors remain in the table until the table is cleared with a SPC clear command (CMD017). The format of the checksum error table is shown below.



10.6 System Error Table

When the processor status word indicates a system error table entry, additional information about the error can be obtained by examining the system error table. When the table becomes full, new errors write over top of the last location. The errors remain in the table until the table is cleared with a SPC clear command (CMD017). The format of the system error table is shown below. The table can hold a total of 32 errors.



The error code specifies the type of error which has occured. The data is that data associated with the error. ETC is 10 bits of the elapsed time count when the error occurred (LSB = 2^7 sec).

CODE (OCTAL)	MEANING	DATA
0	Not Used	
1	Undefined Command	Command
2	Illegal S/C LOCDAT Command	Command
3	UPC on Command given with no Start Address	Command
4	UPC on Command Start Address out of limits	Command
5	Real Time AIS (J or SK) Command	Command
6	Missed MS Sampling Band	MSEC out of Band
7	Command Buffer Full	Command
010	Diagnostic Error	Diagnostic Segment
011	MAC Command with no Address or Count, or Count too large for MAC TEL	Command
012	RAM Overflow on Memory Load Expected	Command
013	Commanded Device Busy	Command
014	Commanding Error	
015	Uplink Parity Error Command Rejection	Command
016	Main Memory Standby CMD not from Main Memory	Command
017	Uplink Memory Parity Error OVERRIDE	Command
020	Bad Time Tag	Command
021	Illegal Command in Stored Command Memory	Command
022	Telemetry Data Ready Flag Failure	Telemetry Data
023	Telemetry Buffer Overflow	Telemetry Data
024	Uplink CV Buffer Overflow	Command
025	Channel to DT Interlock Violated	Command
026	Undefined Location Data from S/C	Z17-Z32 of Location Data
027	Location Data Ready Flag Failure	Z17-Z32 of Location Data
030	Real Time Clock 1 Overflow	Encoder Count
031	Real Time Clock 2 Overflow	Encoder Count
032	WD3 (S1SEGS) Flag Failure	Encoder Count
033	WD7 (S2SCOF) Flag Failure	Encoder Count
034	Erroneous Sensor Switch	Encoder Count
035	Scanner Upset	ETC
036	Scanner Amplitude Out of Limits	Scanner Amplitude
037	Violation of Minimum Time Between MS Byte Tranfers	Load Data
040	MS Load Calculated CKSM Not Equal to Block CKSM	Calc CKSM

TABLE OF ERROR DATA FORMATS

CODE (OCTAL)	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	CV						COMMAND									
2	MSB						COMMAND									
3	CV						COMMAND									
4	CV						COMMAND									
5	CV						COMMAND									
6	2^{15}						MSEC									2^{0}
7	CV						COMMAND									
010														2^{2}-SEG		2^{0}
011	CV						COMMAND									
012	CV						COMMAND									
013	CV						COMMAND									
014	CV						COMMAND									
015	CV						COMMAND									
016	CV						COMMAND									
017	CV						COMMAND									
020	CV						COMMAND									
021	CV						COMMAND									
022		T1	T2	T3	T4	T5	T6	T7	~~T1~~	~~T2~~	T3	T4	~~T5~~	T6	~~T7~~	
023		T1	T2	T3	T4	T5	T6	T7	~~T1~~	~~T2~~	T3	T4	~~T5~~	T6	~~T7~~	
024	CV						COMMAND									
025	CV						COMMAND									
026	Z^{17}					LOCATION DATA										Z^{32}
027	Z^{17}					LOCATION DATA										Z^{32}
030	S	2^{10}			ENCODER COUNT						2^{0}					+ZD
031	S	2^{10}			ENCODER COUNT						2^{0}					+ZD
032	S	2^{10}			ENCODER COUNT						2^{0}					+ZD
033	S	2^{10}			ENCODER COUNT						2^{0}					+ZD
034	S	2^{10}			ENCODER COUNT						2^{0}					+ZD
035	2^{16}						ETC									2^{1}
036	2^{11}					SCANNER AMPLITUDE										2^{-4}
037	MSB						LOAD DATA									
040	MSB						CALCULATED CKSM									

10.7 Access to Error Information

Access to the error information discussed above can be obtained via uplink commands. A MAC (CMD015) command can be used to dump any part of the memory for analysis however, specific addresses must be specified. A detailed knowledge of the operational program listing is required if that method is to be used.

The SPC command (CMD017) can be used to dump functional areas without the detailed knowledge of where these areas are actually located in memory. The areas or functions which can be dumped are:

Operational constants memory
GVVSSE table
Main Memory program
Oribt Memory program
DMDM Memroy
Mission Sensor Preferred State table
Autonomous Mode DMDM memory
Special Ancdat table
Memory block dump
Processor input word
Last state processor output word
Processor status word
Checksum Error Table
System Error table
Main Program Status
Orbit Program Status
Processor Status Error Time Code
Sampled Elapsed Time Clock
OLS Telemetry Address table

Most of the above items have already been described. A few require additional discussion.

GVVSSE Table - The exact dB values used can be obtained from the program listing.

Input/Output Words - The word and bit assignments along with their meaning can be obtained from the software specification.

Memory Block Dump - The program listing contains the exact values.

Main/Orbit Program Status - The address of the next command is in bits 1-13. The program on bit is in bit 16. The time tag test in progress bit is in bit 15. Main program standby bit is in bit 14.

Sampled Elapsed Time Clock - The LSB in bit 1 has a value of 2 seconds.

The Processor Status Error Time Code contains the 2^{-8} through 2^{7} second bits of the ETC when the first processor error occurred thus providing better resolution than obtained from the time code in the error table. When the status error is cleared with an SPC command, this value is reset to zero.

10.8 PSTATE

PSTATE is the analog EST #74 and is used to show the program state. The states are arranged according to priority. PSTATE 1 has the highest priority and PSTATE 7 has the lowest priority.

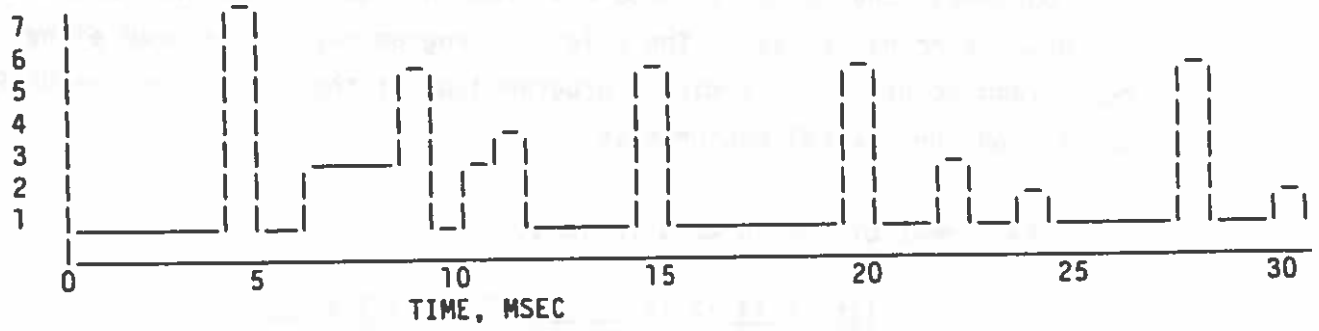
PSTATE 1 - Sensor switching
2 - Sensor calibration and segment selects
3 - Formatting pulses
4 - Initiate mission sensor sampling
5 - Stored Telemetry processing
6 - Real time command processing
7 - Location data processing
0 - Other processing as required.

PSTATE 0 is entered if none of the priority states 1-7 demand attention.

PSTATE 0 performs the following functions:

Orbit clock updating
Orbit memory control
Main memory control
Along scan gain control
Direct mode data processing
Command timing
EST processing and CPU telemetry
Checksum calculation
Processor diagnostic
Command verification
Scanner amplitude calculation

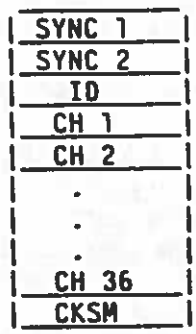
A typical PSTATE representation is shown below. Time 0 represents the peak of the -Z overscan.



10.9 OLS CPU Telemetry

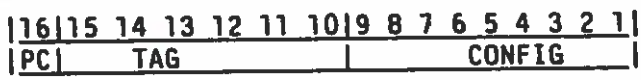
A 40-word OLS CPU telemetry frame is continuously output over MDDATA except when interrupted by a memory dump or memory/program load. After interruption the telemetry output is reset to the beginning of the frame. Sync words differentiate between telemetry and dump/load data. In addition, an ID word following the sync further indicates the type of load/dump, identifies the processor performing the function and presents configuration information which is ground programmable.

The telemetry frame format is shown below:



The format of the data is shown in table 10.9.1. CKSM is a checksum of the telemetry frame addresses and will be constant for an OLSP program load. The channel assignments are programmable and if changed will result in a different CKSM along with different data content (table 10.9.1 will not apply). The ID word has a field available for ground programming which can be used to indicate a different telemetry format configuration. If the table is re-programmed, the formatted data will remain fixed to the new format even if the OLSP is reinitialized. The original program may be restored either by reprogramming or by performing a program load of the portion of the OLSP containing the channel assignments.

The format of the ID word follows:



CONFIG = ground programmable field

TAG = see table 10.9.2

PC = processor (1=D, 0=C)

Table 10.9.2 defines sync words and tags for telemetry, load, and dump modes.

DATA FORMAT

E4ØTEL	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	CH	FUNCTION
+E4SYNC	1	0	1	0	0	1	1	1	0	0	1	0	1	1	1	0	-	SYNC=123456
+E4SYNC	1	0	1	0	0	1	1	1	0	0	1	0	1	1	1	0	-	SYNC=123456
+E4ID	PC		TAG							CONFIGURATION							-	ID
+E6STATUS	0	INIT COUNT					VERSION				REVISION				E3	E2	E1	1	OLSP STATUS WORD
+M1ØN	WAIT															ØN	TTT	2	MAIN MEMORY STATUS
+M1ADR							2^{10}			ADDRESS							2^{0}	3	MAIN MEMORY ADDRESS
+M4ETC	2^{16}								SECONDS								2^{1}	4	MAIN MEMORY CLOCK
+M2ØN																ØN	TTT	5	ORBIT MEMORY STATUS
+M2ADR							2^{10}			ADDRESS							2^{0}	6	ORBIT MEMORY ADDRESS
+M4OC	2^{14}								SECONDS								2^{-1}	7	ORBIT MEMORY CLOCK
+S1PT	2^{15}								CLK*T -2^{17}								2^{0}	8	SCANNER PERIOD
+E2EM	2^{11}								ENCODER COUNT								2^{-4}	9	SCANNER AMPLITUDE
+V1CMD	CV				SUB-SUB						SUB					CMD		10	LAST EXECUTED CMD
+F2RRQ	R	ON	ONP	INT	CV				B	A	SOURCE/ DEST.	PR-SUB			PR			11	PRO STATUS
+F2RRQ+5																		12	PR5 STATUS
+F3RLOC	S	2^{12}					FEET FROM BOT										2^{-2}	13	PR1 LOCATION
+F3RLØC+1																		14	PR2 LOCATION
+F3RLØC+2																		15	PR3 LOCATION
+F3RLOC+3																		16	PR4 LOCATION
+NOTCHA	2^{3} TR GAIN 2^{0}						2^{3} TL GAIN 2^{0}				2^{3} T LEVEL 2^{0}							17	T GAIN/LEVEL
+S1PAB	2^{15}						CLK*T										2^{0}	18	+Z TIME
+S1PBC	2^{15}						CLK*T -2^{16}										2^{0}	19	DOS 0 TIME
+S1PCD	2^{15}						CLK*T										2^{0}	20	-Z TIME
+S1PDA	2^{15}						CLK*T -2^{16}										2^{0}	21	DOS 1 TIME
+C6LØCK	F5W	C6W	C6R										DT4	DT3	DT2	DT1		22	DT INTERLOCK
+G2BIAS	S	2^{7}					BIAS										2^{-7}	23	BIAS
+G2MODE							MODE											24	GAIN MODE
+S4CSAZ	S	2^{-1}					COSINE SOL AZIMUTH										2^{-15}	25	COSINE SOLAR AZIMUTH
+S4ELVT	S	2^{7}					SOL ELEVATION										2^{-7}	26	SOLAR ELEVATION
+S4RRH1	S	2^{0}					(R+h)/R										2^{-14}	27	1 + ALT/EARTH RADIUS
+S4LONG	S	2^{-1}					LOCDAT LONGITUDE										2^{-15}	28	LONGITUDE
+S4LAT	S	2^{-1}					LOCDAT LATITUDE										2^{-15}	29	LATITUDE
+F1ZBFA+9	S	2^{-1}					COS LUN AZIMUTH	2^{-7}	S	2^{6}							2^{0}	30	LUNAR Z1 - Z16

DATA FORMAT

E4ØTEL	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	CH	FUNCTION
+F1ZBFFA+8	2^{-1}	LUN	EL		2^{-5}	2^{7}	LABS	(LUN TR	PHASE) TM	TL	HR	HM	2^{0} HL	1 PR	0 PM	1 PL	31	LUNAR Z17-Z32
+NOMSK3																	32	SEGMENT OVERRIDE
+V3ØWO1	2^{5}						DB									2^{-10}	33	VDGA BASE @ SOAD
+S4CMD	SUB-SUB									SUB			CMD				34	S/C LOCDAT CMD
+S1ØS	S	2^{10}				ENCODER COUNT										2^{-4}	35	SCANNER OFFSET
+S1SWØS	S	2^{10}				ENCODER COUNT										2^{-4}	36	OLSP OFFSET
+E4CKSM	2^{15}				E4ØTEL ADDRESS TABLE CHECKSUM											2^{0}	-	TABLE CHECKSUM

B	A	
LF	TF	SDF RCD
LOW		
SPD	C/E	PBK

PR-SUB	
0	OFF
1	RCD
2	PBK
3	FFD

SOURCE/DEST	RCD	PBK
0	SDF	CH1
1	SDS	CH2
2		CH3
3		CH4

C6RQ - CMDO6 REQUEST
C6WU - CMDO6 DT WARMUP
C/E - CLEAR/ENCRYPT

MODE	
0	PGC
+1	ASGC
-1	ATGC

SENSOR	
1	HRD
2	PMT1/9
3	PMT LO
4	PMT HI

CV - COMMAND VERIFICATION BIT
F5W - CMDO1 (RTO) OR CMDO3 (PBK) DT WARMUP
C6W - CMDO6 (TBC) DT WARM-UP
C6R - CMDO6 REQUEST ACTIVE
TTT - TIME TAG TEST IN PROGRESS
R - REQUEST BIT

E1 - CHECKSUM ERROR TABLE ENTRY
E2 - SHED OLS POWER
E3 - SYSTEM ERROR TABLE ENTRY

CLK = 1064960 Hz

ØNP - PR HAS JUST BEEN TURNED ON
INT - PR 5 SEC INTERLOCK
S - SIGN BIT (2's COMP)

TABLE 10.9.2

FUNCTION	SYNC 1	SYNC 2	TAG
OLS TEL	123456	123456	0
PROG LOAD	137465	137465	77
MAC L PAGE	137465	137465	1
BLK			3
TEL			5
MS			7
MSPS			11
AMDMDM			13
SANCDAT			15
MAC D PAGE	137465	137465	2
BLK			4
TEL			6
MSPS			12
AMDMDM			14
SANCDAT			16
SPC D CONST	137465	137465	40
GVVSSE			41
MP			42
ØP			43
DMDM			44
MSPS			45
AMDMDM			46
SANCDAT			47
SPC D PSW	137465	137465	20
CKET			21
SET			22
MS			23
ØS			24
ETC			25
ERT			26
TEL			27
SPC D IW	137465	137465	30
ØW			31
BLK			32

Program loads, commandable loads, and commandable dumps will disable OLS telemetry, output sync 1, sync 2, ID per table, output the load/dump data, output load checksum if applicable, then reset OLS telemetry to start of frame to re-enable OLS telemetry.

10.10 Special Ancillary Data

The SDF ancillary data frames can be commanded to special ancillary data with the PSC command. This provides a convenient method of placing information in primary data which is synchronous with the scanner and occurs every scan line.

The special ancillary data is determined from a programmable six word table of addresses. The data can be changed by loading in addresses of the desired data with the MAC command. The default table contains the addresses of the scanner parameters shown below. Only the lower 14 bits of the first five data words and the lower 12 bits of the last data word are formatted by the SDF formatter. The formats of the Special Ancillary Data table and the primary data ancillary data frame are shown below.

Special Ancillary Data Table

SANCDAT TABLE	default addresses
F1ADAT (0)	+S1PBC
F1ADAT (1)	+S1PCD
F1ADAT (2)	+S1PDA
F1ADAT (3)	+S1PAB
F1ADAT (4)	+E2EM
FIADAT (5)	+S1OS

Data (i = 1 = LSB, i = 16 = MSB)

$Ai = CLK*t_1 - 2^{16}$, DOS 0 active time

$Bi = CLK*t_2$, -Z overscan time

$Ci = CLK*t_3 - 2^{16}$, DOS1 active time

$Di = CLK*t_4$, +Z overscan time

Fi = scanner amplitude $*2^4$

Gi = scanner offset $*2^4$

$CLK = 1.06496 *10^6$Hz

Ancillary Data (Subsync) SDF Frame

SPECIAL

-	-	A1	A2	A3	A4
A5	A6	A7	A8	A9	A10
A11	A12	A13	A14	B1	B2
B3	B4	B5	B6	B7	B8
B9	B10	B11	B12	B13	B14
C1	C2	C3	C4	C5	C6
C7	C8	C9	C10	C11	C12
C13	C14	D1	D2	D3	D4
D5	D6	D7	D8	D9	D10
D11	D12	D13	D14	F1	F2
F3	F4	F5	F6	F7	F8
F9	F10	F11	F12	F13	F14
G1	G2	G3	G4	G5	G6
G7	G8	G9	G10	G11	G12
E27	E26	E25	E24	E23	E22
E21	E20	E19	E18	E17	E16

NORMAL

-	-	Z32	Z31	Z30	Z29
Z28	Z27	Z26	Z25	Z24	Z23
Z22	Z21	Z20	Z19	Z18	Z17
Z16	Z15	Z14	Z13	Z12	Z11
Z10	Z9	Z8	Z7	Z6	Z5
Z4	Z3	Z2	Z1	C8	C7
C6	C5	C4	C3	C2	C1
C0	-	Y4	Y3	Y2	Y1
H8	H7	H6	H5	H4	H3
H2	H1	H0	-	I4	I3
I2	I1	P8	P7	P6	P5
P4	P3	P2	P1	U	M4
M3	M2	M1	G9	G8	G7
G6	G5	G4	G3	G2	G1
E27	E26	E25	E24	E23	E22
E21	E20	E19	E18	E17	E16

Ei = elapsed time count

The bit designators in the normal frame are from the OLS-S/C interface spec. Those in the special frame are as defined in this section.

APPENDIX A

UPLINK COMMAND FORMATS

UPLINK COMMAND LIST

CMD CODE	MNEMONIC	DESCRIPTION
0 0	GNC	Gain Control
0 1	RTR	Real Time Readout
0 2		
0 3	SDC	Stored Data Control
0 4	RLC	Recorder Location Counter
0 5		
0 6	TBC	Transmitter/BBT Control
0 7	PSC	Primary Sensor Control
1 0	LDC	Location Data Command
1 1	SSC	Mission Sensor Control
1 2	SGN	System Generator
1 3	ØCP	Orbit Clock Preset
1 4	UPC	Uplink Program Control
1 5	MAC	Memory Access Control
1 6	AIS	Auxiliary Instruction Set
1 7	SPC	Special Purpose Commands

NOTE: Formats of the form A/B refer to when the bit is in the 1/0 position.

CMD 00 - GAIN CONTROL (GNC)

16	15 14 13 12	11 10	9	8 7 6 5	4 3 2 1	
P	2^3 -T GAIN- 2^0	0 0	0	0 0 0 0	0 0 0 0	T Channel Gain
	2^3 -T LEVEL- 2^0	0 0	1			T Channel Level Shift
		0 1	0			Spare
	R M L A	0 1	1			T SEG SEL
	R M L A	1 0	0			HRD SEG SEL
	R M L A	1 0	1			PMT SEG SEL
	2^3 -TL GAIN- 2^0	1 1	0			T Left Channel Gain
	2^3 -TR GAIN- 2^0	1 1	1			T Right Channel Gain
			LO / LI	0 0 0 1		ASGC Mode
				0 0 1 0		ATGC Mode
				0 0 1 1		Spare
	2^5 ___GAIN___ 2^0		LO /	0 1 0 0		HRD PGC Mode
			/	0 1 0 1		PMT 1/9 PGC Mode
			LI	0 1 1 0		PMT LO PGC Mode
				0 1 1 1		PMT HI PGC Mode
	S 2^3 _____ 2^{-1}		0	1 0 0 0		GVVSSE Bias Adjust
	S 2^{-2} _____ 2^{-6}		1			GVVSSE Slope Adjust
		Rv Rs		1 0 0 1		BRDF Enable
				1 0 1 0		Spare
				1 0 1 1		Spare
				1 1 0 0		Spare
				1 1 0 1		Spare
				1 1 1 0		Spare
				1 1 1 1		Spare

A = Automatic Segment Select
L = Left Segment
M = Mid Segment
R = Right Segment
S = Sign Bit (two's comp. neg. numbers)
T LEVEL = 1.02°K shifts at 210°K (initialized to = 1000)
T GAIN = 0.16 dB steps for OLS 8-10 (initialized to = 0101)
= 0.24 dB steps for OLS 7, 11-16 (initialized to = 0101)

BRDF Enable initialized Rs and Rv on.
Rs = Specular component
Rv = Diffuse component
GVVSSE Slope adjust is Spare for OLSP Rev K and up.

CMD 01 - REAL TIME READOUT (RTR)

16	15	14	13	12	11 10	9	8	7 6 5	4 3 2 1	
P		DM DM	TF LS	CL / / ENC	CH		ON / / OFF	0 0 0	0 0 0 1	RTD
								0 0 1		Spare
								0 1 0		Spare
								0 1 1		Spare
								1 0 0		Spare
								1 0 1		Spare
								1 1 0		Spare
								1 1 1		Spare

11 10	
0 0	Channel 1
0 1	Channel 2
1 0	Channel 3
1 1	Channel 4

- Consecutive ON CMDS will be executed as long as the specified channel is available.
- A channel is unavailable if it is connected to one of the recorders.
- The RTD formatter may be connected to any number of channels.

CMD 02 - SPARE

CMD 03 - STORED DATA CONTROL (SDC)

16	15 14	13 12	11 10	9 8	7 6 5	4 3 2 1	
P		B A	SOURCE / / DEST	SUB CMD	0 0 0	0 0 1 1	PR 0 (Test)
					0 0 1		PR 1
					0 1 0		PR 2
					0 1 1		PR 3
					1 0 0		PR 4
					1 0 1		PR 5 (Test)
					1 1 0		N/A
					1 1 1		N/A

SUB CMD	MODE
0 0	OFF
0 1	RECORD
1 0	PLAYBACK
1 1	FAST FORWARD

SOURCE /DEST	RCD	PBK
0 0	SDF	CH 1
0 1	SDS	CH 2
1 0	SPARE	CH 3
1 1	SPARE	CH 4

B	A	
LF	TF	SDF RCD
LO/HI SPD	CLR/ ENC	PLAYBACK

- o PR test used with OFF and RECORD mode only.
- o SDC CMDS (except SDC OFF) will be rejected if the selected PR or channel is in use. An active formatter will not reject the CMD; however, the formatter will be reconfigured per the CMD.
- o One formatter may drive all PR's at once. One PR may drive only one channel.
- o A PR test CMD will set up the specified formatter without affecting PR1-4. If a previous PR test CMD is active the CMD will be rejected.

CMD 04 - RECORDER LOCATION COUNTER (RLC)

16	15 14 13	12 11 10 9 8 7 6 5	4 3 2 1
P	PR #	2^{10} Location (ft) 2^{3}	0 1 0 0

PR # = Primary Recorder Number (1-4)
Location = Feet from BOT. Range 0-2040 in steps of 8 ft.

CMD 05 - SPARE

CMD 06 - TRANSMITTER/BBT CONTROL (TBC)

16	15 14	13 12	11 10	9 8	7 6 5	4 3 2 1	
P	DT4 CH*	DT3 CH*	DT2 CH*	DT1 CH*	0 0 0	0 1 1 0	Channel - DT Select
				ON	0 0 1		DT Power
			DT*	/	0 1 0		DT Interlock
			BBT*	/	0 1 1		BBT Power
				OFF	1 0 0		Spare
					1 0 1		Spare
					1 1 0		Spare
					1 1 1		Spare

* CH/ DT/ BBT	
0 0	DT, CH, BBT 1
0 1	DT, CH, BBT 2
1 0	DT, CH, BBT 3
1 1	DT, CH, BBT 4

- The interlock CMD also turns OFF the DT.
- The normal and intialized state of the CH-DT select logic is CH1-DT1, CH2-DT2, CH3-DT3, CH4-DT4.
- One channel can be connected to only one DT.

CMD 07 - PRIMARY SENSOR CONTROL (PSC)

16	15	14	13	12	11	10	9	8	7 6 5	4 3 2 1	
P		SB	I		T	P	SA	ON	0 0 0	0 1 1 1	SENSOR CONTROLS
							F	/	0 0 1		ENCODER SIMULATO
								/	0 1 0		Spare
		2^5 DELEM					2^0	OFF	0 1 1		SCANNER PROTECT
				S4	S3	S2	S1		1 0 0		SPU CONTROLS
									1 0 1		Spare
									1 1 0		Spare
									1 1 1		SPECIAL ANCDAT

P PMT Power Enable - Initialized to Disable
T T Channel Heater Enable - Initialized to Disable
SA Scanner Enable A - Initialized to Disable
SB Scanner Enable B - Initialized to Disable

I IMC Enable - Initialized to Enable
F Encoder Pulse Simulator Free Run - (0 = LOCKED)

DELEM = Scanner amplitude limit minus 1024.5

Scanner Protect initialized ON with limit of 1050.5 (DELEM = 26)

S1-S3 Spare SPU control bits
S4 Solenoid Mechanism activate - initialized off

CMD 10 - Location Data Command (LDC)

16	15 14 13 12 11 10 9 8	7 6 5	4 3 2 1	
P	0 1 0 0 0 1 1 0	0 0 0	1 0 0 0	Phase 2 Load St
		0 0 1		Spare
	0 0 0 0 1 1 1 1	0 1 0		Phase 1 Load St
	0 1 1 1 0 1 0 1			Autonomous Mode
		0 1 1		Spare
		1 0 0		Spare
		1 0 1		Spare
		1 1 0		Spare
		1 1 1		Spare

CMD 11 - MISSION SENSOR CONTROL (SSC)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
P			Sensor ID*					On/Off	0	0	0	1	0	0	1	Power
									0	0	1					Mode 1 Select
									0	1	0					Mode 2 Select
									0	1	1					XMIT Control Word
	MSB		CONTROL WORD					LSB	1	0	0					Take Control Word
									1	0	1					SPARE
									1	1	0					SPARE
									1	1	1					SPARE

Mode 1/2 Select

0, OFF or HOLD (+5v)

1, ON (OV) or ADVANCE (OV pulse)

*SENSOR ID (DECIMAL)

0 = None Selected

1 - Sensor A

12 = Sensor L

13 - 15 = Spare

CMD 12 - SYSTEM GENERATOR (SGN)

16	15 14	13 12 11 10	9	8	7 6 5	4 3 2 1	
P		SELECT		On/Off	0 0 0	1 0 1 0	Redundant Funct Control
					0 0 1		Spare
					0 1 0		Spare
					0 1 1		Spare
					1 0 0		Spare
					1 0 1		Spare
					1 1 0		Spare
					1 1 1		Spare

SELECT	REDUNDANT FUNCTION
0	Clock Driver Y
1	Sensor Control Y
2	Gain Control Y
3	WOW Flutter Y
4	FID & AUX Encoder Backup (mirrors)
5	Vacuum
6	Spare
7	Spare

SELECT	REDUNDANT FUNCTION
010	Output Data MUX Y
011	SSP FMT H
012	RTD FMT H
013	SDF FMT H
014	SDS FMT H
015	L' Video Filters
016	T' Video Filters
017	HRD AUX Post Amp

NOTE: Select 5 (vacuum) is used in test only to modify the DME for operating in air o vacuum. Select 5 off sets DME for air. Select 5 on sets DME for vacuum. This discrete is initialized to vacuum.

CMD 13 - ORBIT CLOCK PRESET (OCP)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
P									0	0	0	1	0	1	1	Zero Preset
	2^7 — ADR — 2^0								0	0	1					Preset OTC Indirect
	2^6 — SEC — 2^{-1}								0	1	0					Preset OTC Direct
	S 2^5 — SEC — 2^{-1}								0	1	1					OTC SEC ADJ
	S 2^6 — MIN — 2^0								1	0	0					OTC MIN ADJ
									1	0	1					
									1	1	0					
									1	1	1					

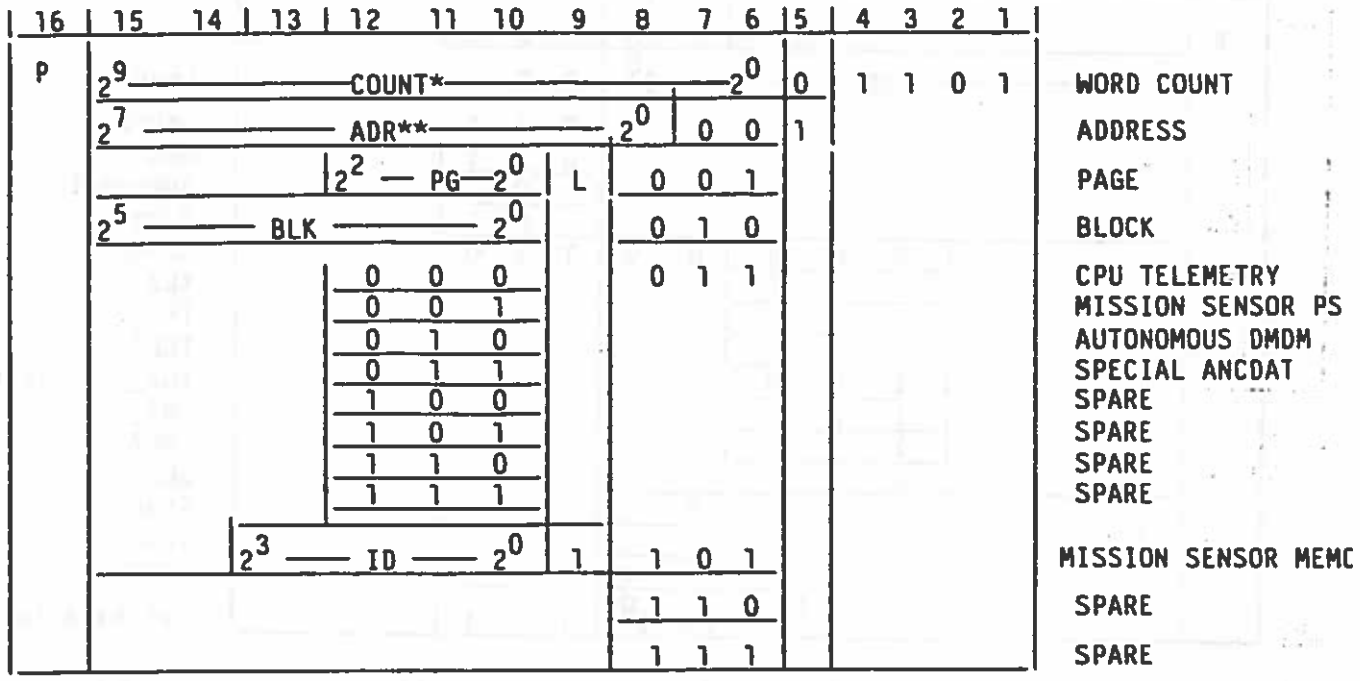
- o ADR is the address (0 - 0377) in page 0 of the uplink memory where the preset values can be found
- o Preset values of 0.0 up to 127.5 seconds can be specified directly in the preset direct SUB-CMD.

CMD 14 - UPLINK PROGRAM CONTROL (UPC)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
P							0	M	0	0	0	1	1	0	0	Main/Orbit Memory OFF
	2^7 — ADR — 2^0								0	0	1					Set Starting Address within Page
						2^2	PG	2^0	0	1	0					Set Starting Page and Turn ON
									0	1	1					Main Memory Standby
									1	0	0					Spare
									1	0	1					Spare
									1	1	0					Spare
									1	1	1					Spare

PG = Uplink Memory Page Number

CMD 15 - MEMORY ACCESS CONTROL (MAC)



PG = Uplink Memory Page Number (0 - 7)

BLK = Processor Memory Block Number (0 - 077)

ID = Mission Sensor Number (1 - 12)

PS = Preferred State Table (Mission Sensors)

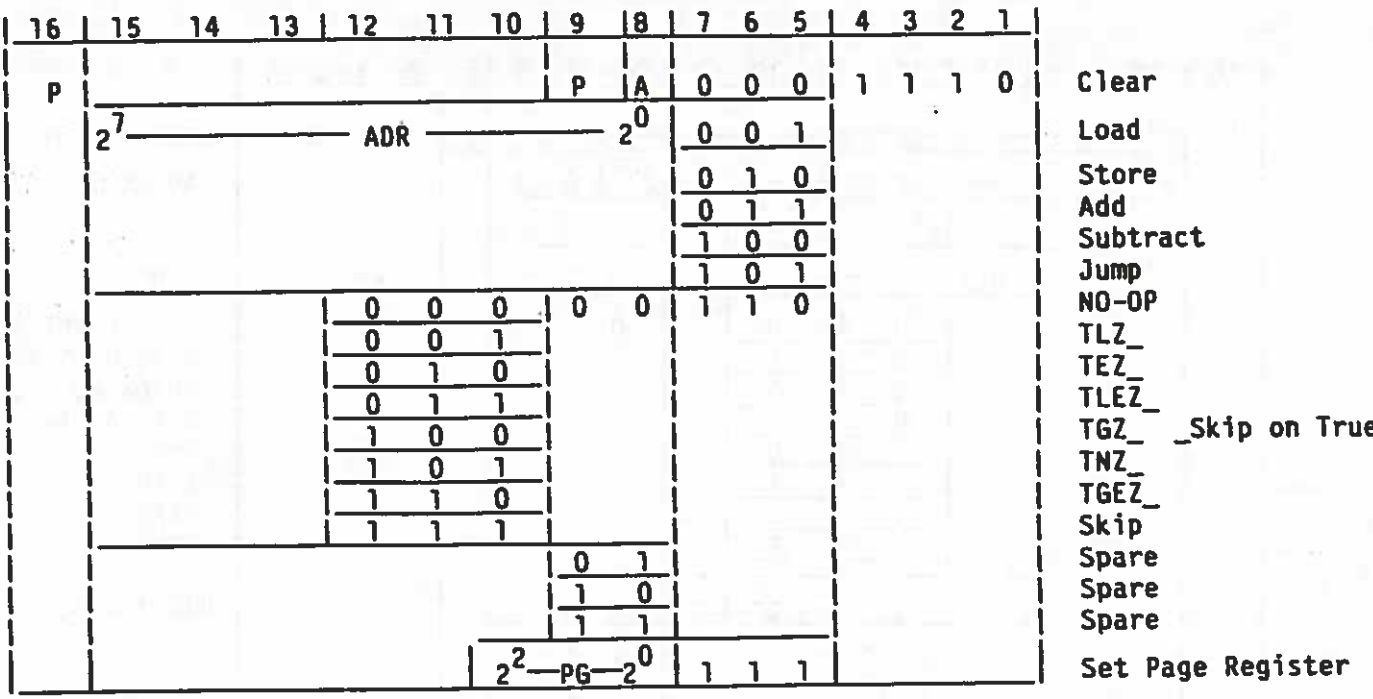
L = 1, Load
0, Dump (not available for mission sensor)

* For Page and Block, loads and dumps, a word count of 0 specifies 1024 words, thus 4 complete pages (blocks) can be loaded or dumped at c time.

**

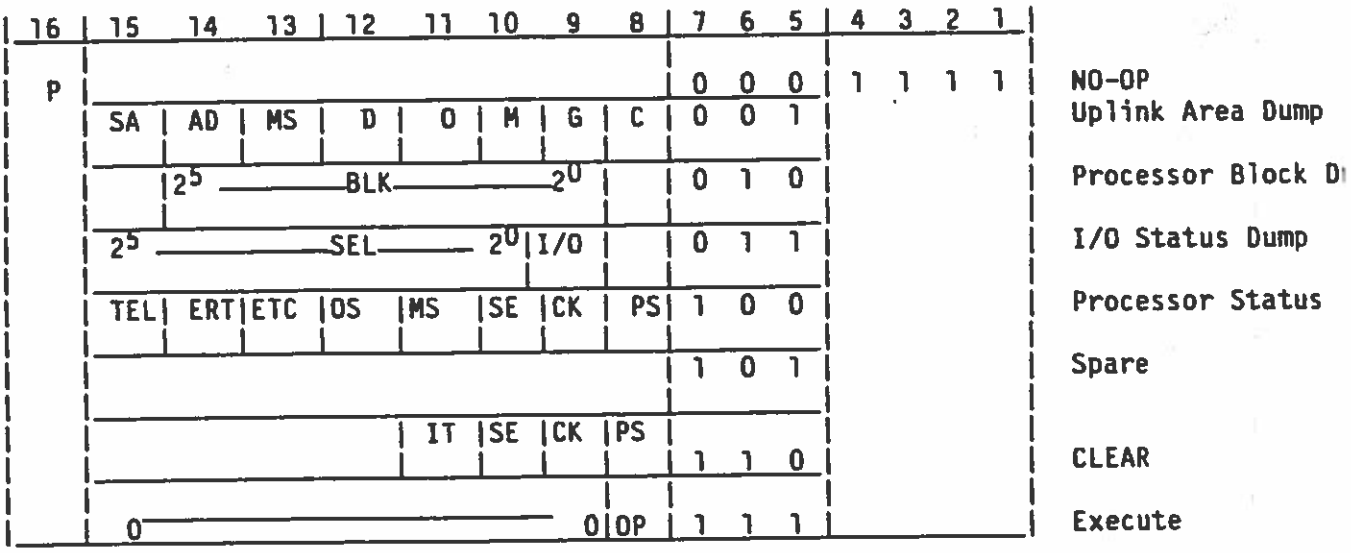
LOAD/DUMP TYPE	MEANING OF ADR	RANGE
PAGE	Address in Page	0 - 255
BLOCK	Address in Block	0 - 255
CPUTLM	CPU TLM Channel Number	1 - 36
MSPS	Address in table	0 - 49
AMDMDM	Address in table	0 - 45
SANCDAT	Address in table	0 - 5
MS MEM LD	Count of 1K (1024) words	0 - 31

CMD 16 - AUXILIARY INSTRUCTION SET (AIS)



- Operations are performed on a 15-bit accumulator (A). Two's complement arithmethic will be used with bit 15 as the sign bit.
- Memory is referenced by a page number and an address within the page. The page register must be set to the page in which the memory operand lies.
- The page register retains its value until another set page or clear page command is executed.
- The clear command sets the page and/or accumulator to zero.
- The jump command will always jump to a location within the page in which the jump command resides.
- The skip command will skip over the next command if the test is true. Skipping may occur across page boundaries.
- The AIS commands can be simultaneously programmed in both main and orbit memories since there are separate Page & Accumulaters for each.

CMD 17 - SPECIAL PURPOSE COMMANDS (SPC)



C	Operational Constants
G	GVVSSE Table
M	Main Program
O	Orbit program
D	DMDM Memory
MS	Mission Sensor Preferred State Table
AD	Autonomous Mode DMDM Memory
SA	Special Ancillary Data Table
I/O	1 = Input select, 0 = output select
SEL	I/O Select Code

PS	Processor Status Word (CLEAR PS Clears Error Bits Only)
CK	Checksum Error Table
SE	System Error Table
MS	Main Program Address Counter and Status
OS	Orbit Program Address Counter and Status
ETC	Sampled Elapsed Time Count
ERT	Processor Status Error Time Code (LSB = 2^{-8} sec)
TEL	OLS TEL Table

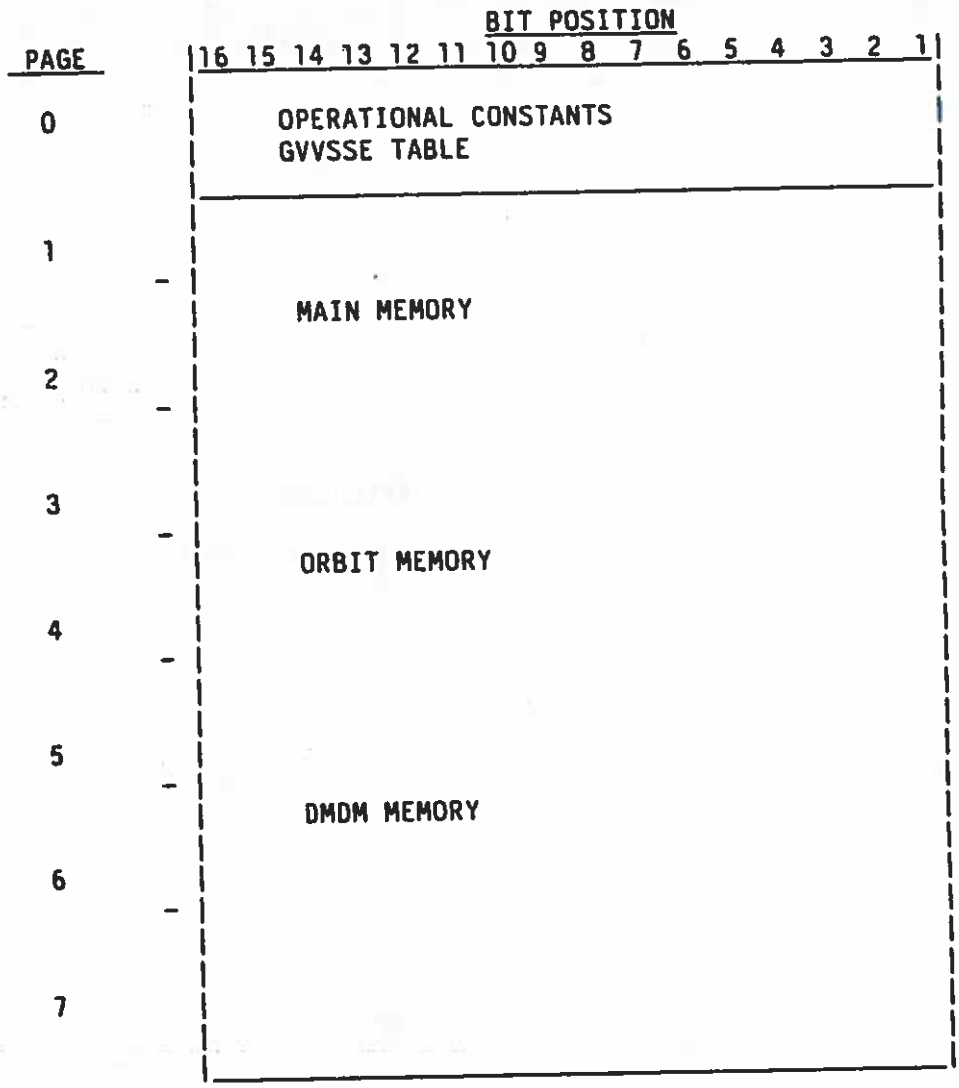
OP	Override Parity
IT	Init Count in Processor Status Word

PRIORITY OF DUMPING MULTIPLE DUMPS STARTS WITH BIT 8.

APPENDIX B

UPLINK MEMORY FORMATS

UPLINK MEMORY ALLOCATION

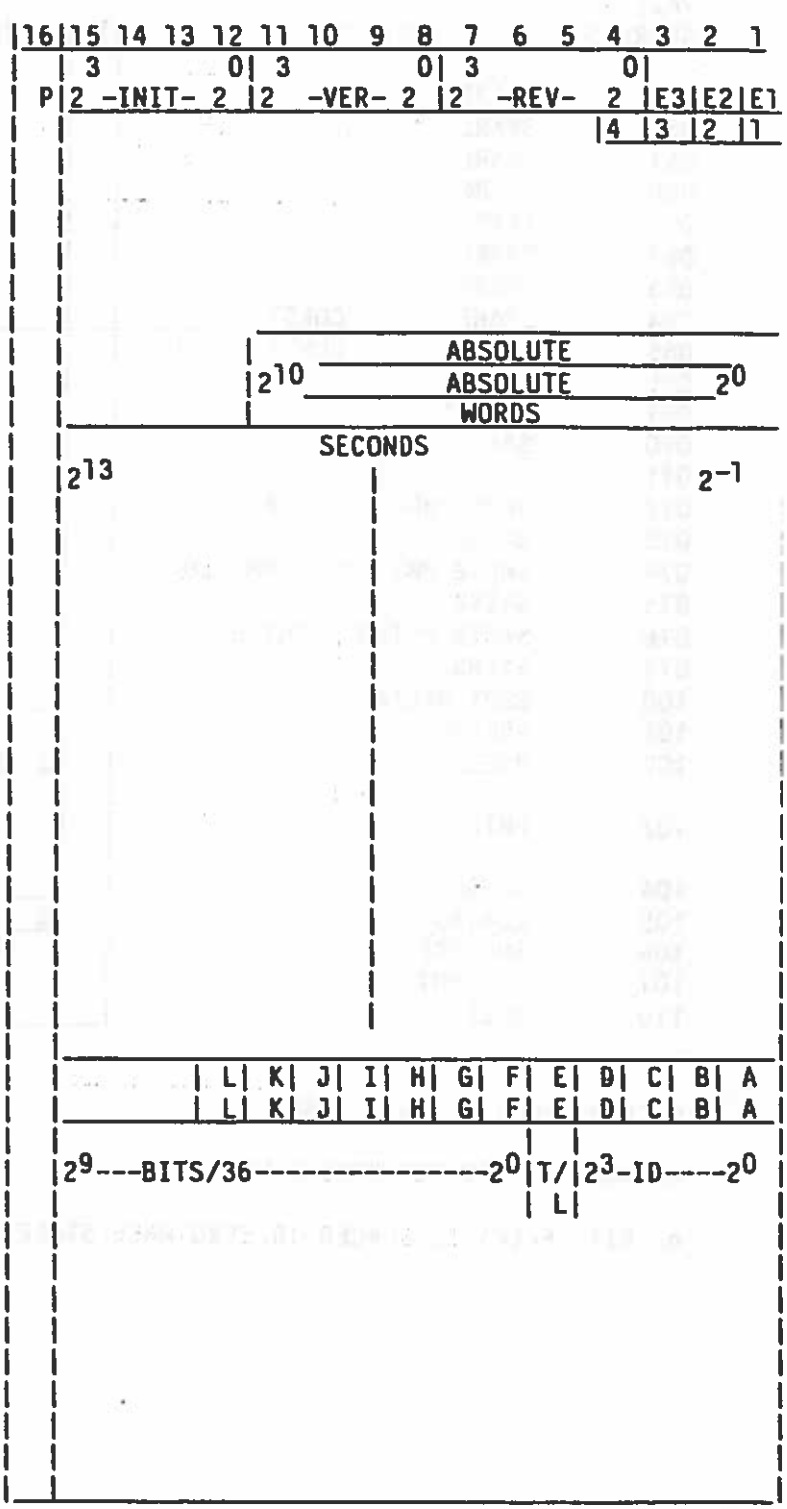


- 2K MEMORY BROKEN INTO 8 PAGES OF 256 WORDS EACH.
- 1792 LOCATIONS AVAILABLE FOR UPLINK PROGRAMS (896 CMDS).

OPERATIONAL CONSTANTS ALLOCATION

PAGE 0

ADDRESS	CONTENTS
000	PSW
001	BADPR
002	SPARE
003	SPARE
004	SPARE
005	SPARE
006	SPARE
007	SPARE
010	ORBIT MEM. START ADR.
011	DMDM MEM. START ADR.
012	DMDM MEM. LENGTH
013	OTC PRESET VALUE #1
014	OTC PRESET VALUE #2
015	OTC PRESET VALUE #3
016	OTC PRESET VALUE #4
017	OTC PRESET VALUE #5
020	OTC PRESET VALUE #6
021	OTC PRESET VALUE #7
022	OTC PRESET VALUE #8
023	OTC PRESET VALUE #9
024	OTC PRESET VALUE #10
025	OTC PRESET VALUE #11
026	OTC PRESET VALUE #12
027	OTC PRESET VALUE #13
030	OTC PRESET VALUE #14
031	OTC PRESET VALUE #15
032	OTC PRESET VALUE #16
033	OTC PRESET VALUE #17
034	OTC PRESET VALUE #18
035	OTC PRESET VALUE #19
036	OTC PRESET VALUE #20
037	MSMD1 TYPE
040	MSMD2 TYPE
041	MS FMT WD #1
042	MS FMT WD #2
043	MS FMT WD #3
044	MS FMT WD #4
045	MS FMT WD #5
046	MS FMT WD #6
047	MS FMT WD #7
050	MS FMT WD #8
051	MS FMT WD #9
052	MS FMT WD #10
053	MS FMT WD #11
054	MS FMT WD #12



REV R

OPERATIONAL CONSTANTS ALLOCATION

PAGE 0

ADDRESS	CONTENTS	16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
055	SPARE		
056	SPARE		
057	SPARE		
060	SPARE		
061	SPARE		
062	SPARE		
063	SPARE		
064	SPARE CONST I		
065	SPARE CONST II		
066	INHOFS		I
067	VEHDAT		2^3 ID 2^0 D
070	SPARE		
071	HRD OFFSET		5 -3
072	SWPT1 HRD-PMT 1/9		2 VDGA DB 2
073	GAIN1		
074	SWPT2 PMT 1/9 - PMT LO		
075	GAIN2		
076	SWPT3 PMTLO - PMT HI		
077	GAIN3		
100	SWPT DELTA		2^2 DB 2^{-3}
101	PDELBS		14 1
102	PDELSP		S 2 CLOCKS* 2
103	PMTCG		5 -3 2 VDGA DB 2
104	BCMAX		7 -6 2 GVVSSE DB 2
105	LGBIAS		S 2^3 DB 2^{-10}
106	BRDFHRD		2^3 2^{-10}
107	BRDFPMT		2^3 2^{-10}
110	BRDFX2		2^3 2^{-10}

- o ADR 0-064 FOR DMCC USE
- o ADR 065-110 FOR DMCC & PSCC USE
- o BIT 16 (P) IS FORCED TO ZERO WHEN STORED.

* 1 CLOCK = 1/1.064960 uSec

GVVSSE MEMORY ALLOCATION

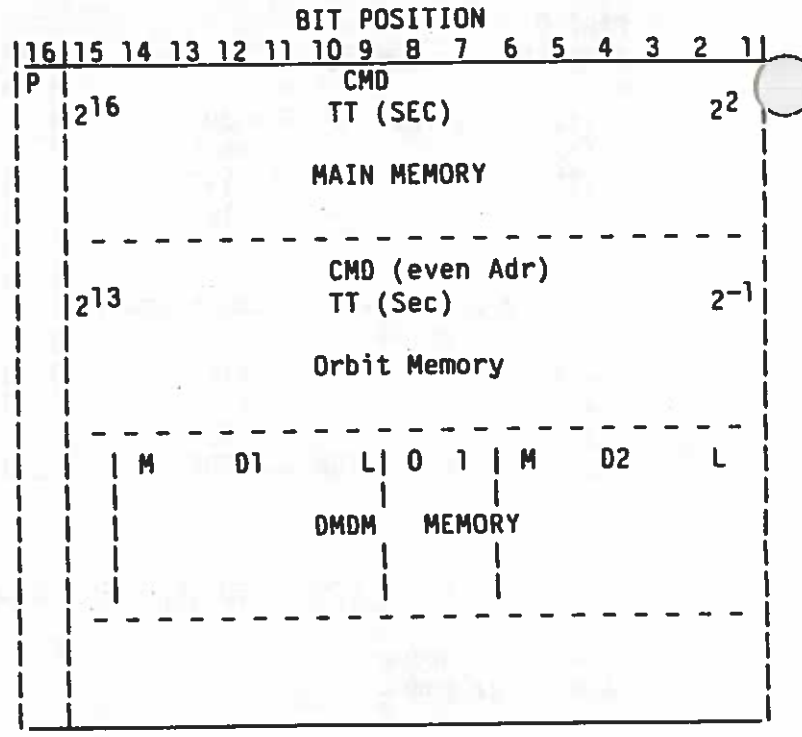
PAGE 0 ADDRESS	CONTENTS	BIT POSITION 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
			8 -6
111	GVVSLE FOR GL=+80°	P	2 DB 2
112	+80°		
113	+79°		
114	+78°		
237	GVVSLE GL=-5°, GVVSSE GS=-15°		
374	+78°		
375	+79°		
376	+80°		
377	GVVSSE FOR GS=+80°		

o BIT 16 (P) IS FORCED TO ZERO WHEN STORED.

GS = Solar gamma
GL = Lunar gamma

UPLINK PROGRAMS AND DMDM ALLOCATION

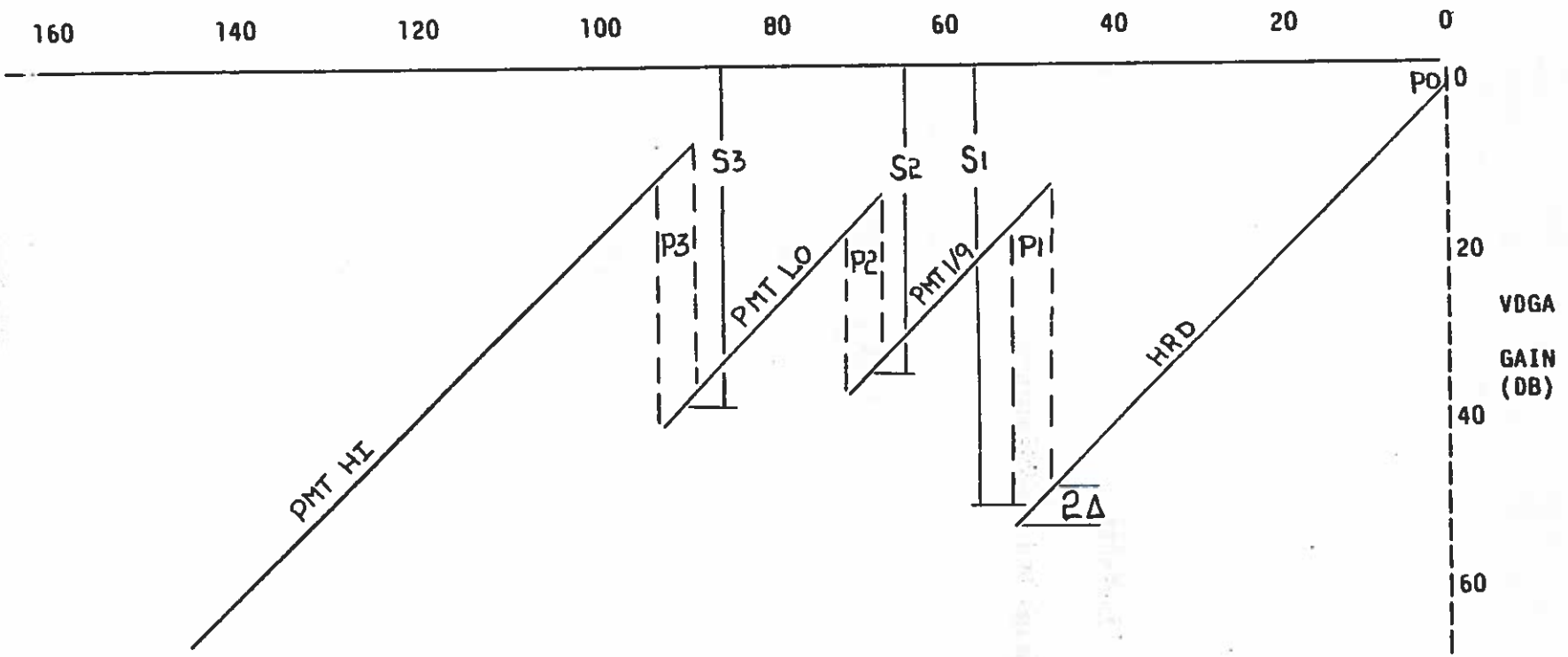
PAGE	PAGE ADDRESS	ABSOLUTE ADDRESS
1	000	0400
	|	|
	377	0777
2	000	1000
	|	|
	377	1377
3	000	1400
	|	|
	377	1777
4	000	2000
	|	|
	377	2377
5	000	2400
	|	|
	377	2777
6	000	3000
	|	|
	377	3377
7	000	3400
	|	|
	377	3777



- o BOUNDARIES ARE FLEXIBLE, HOWEVER, ORBIT MEMORY MUST START IN AN EVEN ADDRESS
- o BIT 16 (P) REFLECTS THE PARITY CORRECTNESS OF THE WORD WHEN IT WAS UPLINKED (ie. 0, CORRECT PARITY; 1, INCORRECT PARITY)

APPENDIX C

SENSOR GAINS AND SWITCH POINTS



TYPICAL VALUES

2Δ = 3 DB		SWITCH POINT DELTA x2
P(0) = 3 DB		HRD OFFSET (SENSOR 1)
P(1) = 36 DB		PMT 1/9 GAIN (SENSOR 2)
P(2) = 19 DB		PMT LO GAIN (SENSOR 3)
P(3) = 30 DB		PMT HI GAIN (SENSOR 4)
S(1) = 52 DB		SENSOR 1-2 SWITCH POINT
S(2) = 36 DB		SENSOR 2-3 SWITCH POINT
S(3) = 39 DB		SENSOR 3-4 SWITCH POINT

FOR +Z DIRECTION SWITCH POINT = S(X-1)-P(X-1)+Δ

FOR -Z DIRECTION SWITCH POINT = S(X)-Δ

SENSOR GAINS AND SWITCH POINTS

APPENDIX D

LIST OF ABBREVIATIONS

APPENDIX D

LIST OF ABBREVIATIONS

AIS	Auxilary Instruction Set
ASGC	Along Scan Gain Control
ATGC	Along Track Gain Control
BBT	Black Box Transmitter
CAP	Command Access Period
CKSM	Checksum
COMDAT	Command Data
CVDATA	Command Verification Data
C/V	Command Verification
DMCC	Data Management and Control Computer
DMDM	Direct Mode Data Message
DOS	Direction of Scan
DT	Data Transmitter
EOS	End of Scan
ERT	Processor Status Error Time Code
EST	Equipment Status Telemetry
ETC	Elapsed Time Clock
GNC	Gain Control
GVVSSE	Gain Value VS Scene Solar Elevation
HRD	High Resolution Diode
I/O	Input/Output
L	Light Data
LF	Light Fine Data
LS	Light Smooth Data
LSB	Least Significant Bit
MAC	Memory Access Control
MDDATA	Memory Dump Data
MS	Mission Sensors
MSB	Most Significant Bit
OC	Orbit Clock
OCP	Orbit Clock Preset
OLS	Operational Linescan System
OLSP	Operational Program
PGC	Preset Gain Control
PMT	Photo Multiplier Tube
PR	Primary Recorder
PSC	Primary Sensor Control
PSCC	Primary Sensor Control Computer
ROM	Real Only Memory
RLC	Recorder Location Counter
RTD	Real Time Data
RTDF	Real Time Data Formatter
RTR	Real Time Readout
SDC	Stored Data Control
SDF	Stored Data Fine
SDFL	Stored Data Fine Light data
SDFT	Stored Data Fine Thermal data
SDS	Stored Data Smooth
SGN	System Generator
SPC	Special Purpose Commands
SPU	Special Processing Unit

SSC	Mission Sensor Control
SSS	Scanner Sub System
S/C	Spacecraft
T	Thermal data
TBC	Transmitter/BBT Control
TF	Thermal Fine data
TS	Thermal Smooth data
TTG	Time Tag
UPC	Uplink Program Control
VDGA	Variable Digital Gain Amplifier

APPENDIX II

DETERMINATION OF SCAN ANGLE OF VIDEO DATA SAMPLES IN OLS DATA

1.0 INTRODUCTION

The stored data is corrected in the OLS so that data samples correspond to fixed scan angles. These data samples would occur linearly versus time if the scanner motion were nominal. When scanner motion differs from nominal, the correction places the data samples at the same scan angles as a nominal scanner motion would place them. The nominal scanner motion is defined by a ROM in the OLS to be a cosine wave with the following characteristics:

$$\phi = \phi_p \cos(2\pi f t)$$

where:

ϕ_p = 57.85° peak scan amplitude
f = 5.94 Hz scan frequency
t = time from positive peak scan angle.

The data sampling for nominal motion occurs at a sampling frequency, f_s, of 102.4 kHz in Stored Data Fine (SDF) and 20.48 kHz in Stored Data Smoothed (SDS). Data samples are only taken over the central "active data" portion of the scan of $\pm(996/1024.5)*57.85° = \pm 56.240703°$. The number of data sampling periods, S_T, in the active data region is determined as follows:

$$S_T = f_s * \left| (t_{-996} - t_{+996}) \right|$$

$$= f_s * 71.505654E\text{-}3$$

$$= 7322.179 \text{ for SDF}$$

$$= 1464.436 \text{ for SDS}$$

where t_{+996} and t_{-996} are the times from the positive peak scan angle to delphi +996, which is 6.3347 msec, and to delphi -996, which is 77.8403 msec.

Since samples are taken at the start of the sampling period the total samples available will be one more than the total number of sampling periods available. The variation from these nominal sampling periods has been determined by a simulation of the wow-flutter (w/f) loop with the following worst case inputs:

Scan amplitude = 57.85° ± 0.1%
Scan Frequency = 5.94 Hz ± 1.0%
Encoder inaccuracy at facet to facet period = .05 mr
Distortion of the waveform = .02% (2nd harmonic)
.03% (3rd harmonic)
.01% (5th harmonic)
Wow-flutter clock frequency, $f_{w/f}$ = 512 kHz
Loop gain = lowest permitted by component tolerance.

The results of the simulation show that at the end of active data (Delphi 996) the maximum loop error is ±4 counts of the 512 kHz wow-flutter clock VCO. When this is added to a ±1 count clock retiming variation in the active data period, a total ±5 count variation is possible. A ±5 count variation is equal to $\pm 5/f_{w/f}$ = 9.7656 μsec.

The variation from nominal sampling periods are:

$\pm 5 * (fs/f_{w/f})$ = ±1 for SDF
= ±.2 for SDS

2.0 5D3 OLS SAMPLING

The taking of data samples in the active data portion of the scan is delayed to compensate for the difference between the nominal group delay of the analog filter which determines channel bandwidth and the delay of the encoder processing which determines when a given Delphi pulse has occurred. The signal at the output of the analog filter represents a scan angle other than ± 56.240703° at the time the Delphi ± 996 is through encoder processing. Thus taking of the first sample must be delayed from receipt by the Processor of the Delphi ± 996 pulse so that this first sample represents data from a scan angle of ± 56.240703°. This compensation causes the whole active data sampling region between Delphis ± 996 to be shifted toward +Z in DOS 1 and toward -Z in DOS 0 by C_F in fine and C_S in smoothed. Both C_F and C_S, in their respective modes, cause video sampling to be delayed beyond the start of active data (SOAD) and the end of active data (EOAD) so that the total time during the active data region does not change.

In addition, the T SDS active data region is shifted approximately one-half sample toward +Z to allow the sample-hold and A/D converter to be shared by both L and T data.

The OLS samples are centered around nadir and corresponding samples in each DOS represent the same scan angle. The SDF samples are

delayed by increasing the compensation C_F by $C_F' = 1.179/2$ sample times. This eliminates the line to line jitter and places SDF nadir at sample number 3661.5 in both DOS's. C_F' delays taking of the samples within the already compensated active data region. The SDS DOS 1 sampling is delayed within the compensated active data region by D_S. This assures 1465 samples on each line and places SDS nadir nominally at sample number 733 for L data and at sample number 733.5 for T data. The SD3 design incorporates a D_S equal to 5 wow-flutter clock times . This is the closest number of wow-flutter clock times to the desired $D_S^* = (.436/2)/fs = 10.64$ µsec. The following table shows the resulting nominal SD-3 stored data sampling:

		1st Sample at	Total Samples
	SDF DOS 1	(Delphi -996)+C_F+C_F'	7323.179±1
	SDF DOS 0	(Delphi +996)+C_F+C_F'	7323.179±1
L data	SDS DOS 1	(Delphi -966)+C_S+D_S	1465.436±.2
T data	SDS DOS 1	(Delphi -996)+C_S+D_S+T_S	1465.436±.2
L data	SDS DOS 0	(Delphi +996)+C_S+D_S'	1465.436±.2
T data	SDS DOS 0	(Delphi +996)+C_S-W_S	1465.436±.2

The compensation parameter values and the values used to center data samples about nadir are:

SDF C_F = 13 µsec

$C_F' = (1.179/2)/fs = 6$ µsec

SDS C_S = 68 µsec

$D_S = 5/f_{w/f} = 9.77$ µsec

$D_S' = 2D_S^* - D_S = 11.52$ µsec

$T_S = 13/f_{w/f} = 25.39$ µsec

W_S = wow-flutter clock counts from (Delphi +996)+C_S to the last T sample on previous DOS 1.

= nominally $T_S - D_S' = 13.87$ µsec

The following chart shows the timing between encoder pulses (Delphi ±996) and sampling for T and L stored data smoothed (SDS). Note that the numbering of samples is based on DOS 0.

Sample Period = P_S = 48.83 µsec

Encoder to Video Delay = C_S = 68 µsec

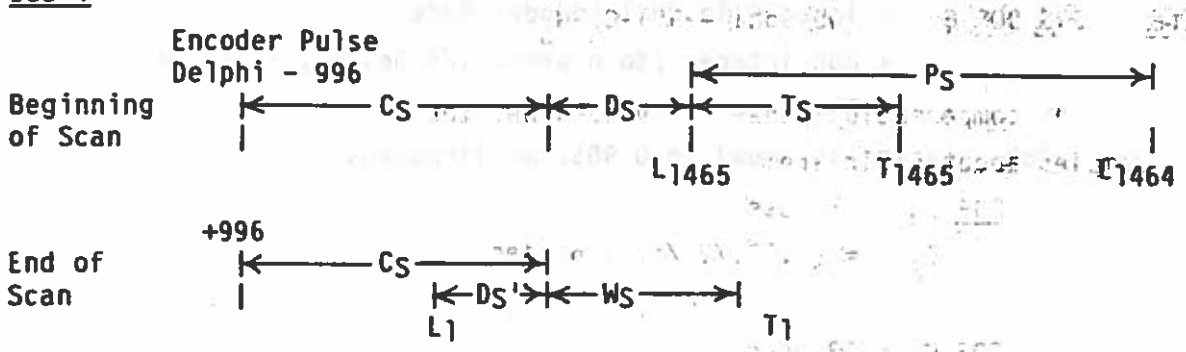
L to T DOS 1 delay = T_S = 25.39 µsec

Centering delay DOS 1 = D_S = 9.77 µsec actual

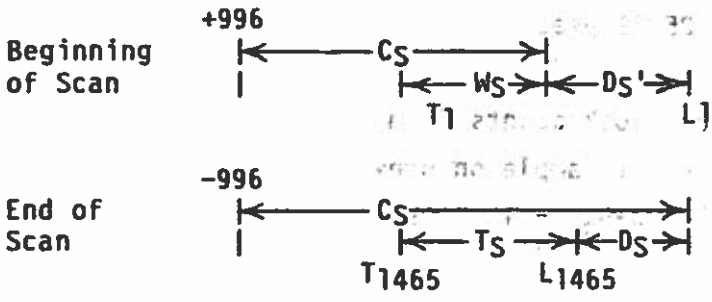
D_S* = 10.64 µsec desired

D_S = 11.52 µsec nominal

DOS 1



DOS 0



3.0 EFFECT OF SCANNER OFFSET

The OLS has provisions for handling what is called "scanner offset". If the center of the sinusoidal scan shifts with respect to scan angles as defined by the optical encoder, the processor shifts its angular reference to maintain data sampling with respect to the sinusoidal waveform. The number of encoder pulses of shift that is current in the processor is transmitted in the data stream as "scanner offset."

The net effect of scanner offset is the same as a spacecraft roll error. Therefore the scan angle relative to the +X primary reference axis becomes:

$$\Phi_{PRI} = \phi - N * 0.0009855 \text{ radians}$$

where:

ϕ = scan angle without offset correction.

N = signed value of scanner offset from subsync frame of data stream.

= integer in Real Encoder Mode

= non-integer (to nearest 1/4 Delphi) in Encoder Simulator Locked Mode.

One delphi spacing is equal to 0.9855 milliradians.

4.0 SCAN ANGLE OF VIDEO DATA SAMPLES - SDF

The SDF video data is corrected in the OLS so that data samples correspond to fixed scan angles. The SDF data sampling occurs at a varying sampling frequency of nominally 102.4 kHz. These data samples would occur linearly versus time if the scanner motion were nominal. When scanner motion differs from nominal, the correction places the data samples at the same angles as a nominal scanner motion would place them.

The scan angle, ϕ, for a given sample number, S_i, is defined as follows:

$$\phi = (-1)^D * \phi_p * \cos\left(\frac{(Si-1)}{S_T} * M + B\right) - N*K$$

where:

D = 0 for SDF DOS 0
  = 1 for SDF DOS 1

ϕp = peak scan angle = 57.85° = 1.00967 radians

Si = sample number in order received by the tape recorder (SOAD = 1, EOAD = 7322)

S_T = nominal total sample periods = 7322.179

M = total active scan = $2\pi f * |(t_{-996} - t_{+996})|$
  = 2.66874 radians

B = start of active scan
  = $2\pi f * (t_{+996} + C_F')$
  = 0.23665 radians

N = signed value of scanner offset from subsync frame of data stream.

K = 0.00099 radians.

5.0 SCAN ANGLE OF VIDEO DATA SAMPLES - SDS

The SDS video is corrected in the OLS so that data samples correspond to fixed scan angles. The data sampling occurs at a varying sampling frequency of nominally 20.48 kHz. These data samples would occur linearly versus time if the scanner motion were nominal. When scanner motion differs from nominal, the correction places the data samples at the same scan angles as a nominal scanner motion would place them.

The T SDS data is shifted approximately one-half sample toward +Z to allow the sample-hold and A/D converter to be shared by both L and T data.

The scan angle, ϕ, for a given sample number, Si, is defined as follows:

$$\phi = \phi_p * \cos\left(\frac{(Si-1)}{S_T} * M + B\right) - N*K$$

where:

ϕ_p = peak scan angle = 57.85° = 1.00967 radians

Si = sample number in order received by the tape recorder (SOAD = 1, EOAD = 1465)

S_T = nominal total sample periods = 1464.436

M = total active scan = $2\pi f^*|(t_{+996} - t_{-996})|$
= 2.66874 radians

B = start of active scan
= $2\pi f^*(t_{+996} + D_S')$ for L data
= $2\pi f^*(t_{+996} - W_S)$ for T data
= 0.23686 radians for L data
= 0.23591 radians for T data

N = signed value of scanner offset from subsync frame of data stream

K = 0.00099 radians

6.0 SCAN ANGLE OF VIDEO DATA SAMPLES - RTD

The RTD video data is not corrected in the DLS so that data samples do not correspond to fixed scan angles. The data sampling occurs at a fixed sampling frequency of 102.4 kHz. Ground correction of video data sample placement to eliminate the effects of scanner motion deviations from nominal is possible using the wow-flutter information. The wow-flutter clock frequency is deviated from its nominal 6023.53 Hz as a direct function of scanner motion deviation from a nominal sine wave of frequency 5.94 Hz and amplitude 57.85 degrees.

The scan angle, ϕ, for any video data sample is defined as follows:

$$\phi = (-1)^{D} * \phi_p * \cos (W*M+B) - N*K$$

where:

D = 0 for RTD DOS 0
= 1 for RTD DOS 1

ϕ_p = peak scan angle = 57.85° = 1.00967 radians

W = number of W/F periods (including fractional periods) between line sync, Delphi 999, and the video data sample of interest

M = one nominal W/F interval = $2\pi f*(1/6023.53\ Hz)$
= 0.0061961 radians

B = start of sampling process corrected for differential signal delay
= $2\pi f*(t_{+999} - D_R)$
= 0.22310 radians for fine data
= 0.22104 radians for smoothed data

N = signed value of scanner offset from subsync frame of data stream.

K = 0.00099 radians

The data sampling process is enabled at Delphi 999. The differential time delay, D_R, between video and W/F sync signals is 13 μsec for fine data and 68 μsec for smoothed data.